

2016 e-Manufacturing and Design Collaboration Symposium (eMDC 2016)

**Hsinchu, Taiwan
9 September 2016**



**IEEE Catalog Number: CFP1696T-POD
ISBN: 978-1-5090-0711-0**

**Copyright © 2016, Taiwan Semiconductor Industry Association (TSIA)
All Rights Reserved**

******This publication is a representation of what appears in the IEEE Digital Libraries. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP1696T-POD
ISBN (Print-On-Demand):	978-1-5090-0711-0
ISBN (Online):	978-986-91715-2-6

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

e-Manufacturing & Design Collaboration Symposium2016

Table of Contents

	Topic	Authors	Association
N1	Prioritization of Key In-Line Process Parameters for Electrical Characteristic Optimization of 16-nm High-k Metal Gate Bulk FinFET Devices 1	Ping-Husn Su and Yiming Li	NCTU
N2	Fundamentals of side isolation LDMOS device with 0.35um CMOS compatible process 5	R.Deivasigamani, Gene Sheu, Shao Ming Yang, S. Krishna Sai, S. Selvendran Chirag Aryadeep, Po-An Chen	Asia University
N3	IPD Robustness Test Methodology for InFO 9	Tang-Jung Chiu, Yen-Cheng Lin, Yi-Chen Wang, Chi-Che Wu, Hung-Chih Lin, and Min-Jer Wang	TSMC
N4	Advance Technique for Automatic Optical Inspection Process Optimization 13	Wiljelm Carl Olalia	ON Semiconductor
N5	Eliminating undercut profile of through silicon via by using nitrided fluorocarbon passivation in rapid alternating process 17	Leonard Hsu, Wei Lai, Jisoo Kim, Eldon Cheng, Paul Lin	Lam Research
N6	Novel InFO Wafer-Level-Chip-Scale-Package N-Leak Test and Stress 20	Hao Chen, Hung-Chih Lin, Ching-Nen Peng, and Min-Jer Wang	TSMC
N7	Improvement of MIM Capacitor Early Breakdown by Metal Deposition Process Optimization and Ar Sputter Etch Implementation 24	Chin-tsan Yeh, Szu-Ming Chu, Yi-Hao Yeh, Wen-Chi Ting, Chih-Yuan Lu	Macronix
N8	Wet Clean Study on Cobalt Silicide and Contact Processes 28	Shih-Ping Lee, Jin-Liang Lin, Chia-Hsien Kuo, Chien-Hui Lu, Chia-Hsin Tsai	Powerchip Technology
N9	The Role of Models in Semiconductor Smart Manufacturing 31	Alan Weber	Cimetrix
N10	Opportunity for Improving Fab Effectiveness by Predictive Overall Equipment Effectiveness (POEE) in Industry 4.0 34	Yu-Ting Kao ¹ , Shi-Chung Chang ¹ , Stéphane Dauzère-Pérès ² , and Jakey	National Taiwan University ¹ , Ecole des Mines de Saint-

		Blue ²	Etienne, Centre Microélectronique de Provence ²
N11	Heuristic Methods for Q-time Bottleneck Dispatching 38	Ching-Lung Chang, Han-Yu Wu, Chao-Kai Chen	Winbond
N12	Capacity Simulation by Cellular Automation in Endura Platform 42	Tung-He Chou, Yu-Chih Chang, Binglung Yu, Chun- Fu Chen, Yung-Tai Hung, Tuung Luoh, Ling-Wuu Yang, Tahone Yang, Kuang- Chao Chen	Macronix
N13	Virtual Metrology for 3D Vertical Stacking Processes in Semiconductor Manufacturing 46	Syueren Wu, Chun-Fu Chen, Tuung Luoh, Ling- Wuu Yang, Tahone Yang, Kuang-Chao Chen	Macronix
N14	New Process Variation Modeling Method of 3-D Capacitances for Advanced Nanometer CMOS Nodes Nodes 49	Kuo-Fu Lee, Hsiao-Han Liu, Ping-Hung Yuh, Ho-Che Yu, Wen-Cheng Huang, Victor C.Y. Chang, Keh-Jeng Chang	TSMC
N15	Research on Ion Implanter Transferring from Spot Beam to Ribbon Beam 51	Yu-An Chen, Shih-Ping Lee, Chien-Hui Lu , Chia-Hsin Tsai	Powerchip Technology