

# **3rd Annual International Wafer-Level Packaging Conference (IWLPC 2006)**

San Jose, California, USA  
1 - 3 November 2006

ISBN: 978-1-5108-3302-9

**Printed from e-media with permission by:**

Curran Associates, Inc.  
57 Morehouse Lane  
Red Hook, NY 12571



**Some format issues inherent in the e-media version may also appear in this print version.**

Copyright© (2006) by Surface Mount Technology Association (SMTA)  
All rights reserved.

Printed by Curran Associates, Inc. (2017)

For permission requests, please contact Surface Mount Technology Association (SMTA)  
at the address below.

Surface Mount Technology Association (SMTA)  
6600 City West Parkway  
Eden Prairie, MN 55344  
USA

Phone: (952) 920-7682  
Fax: (952) 926-1819

[smta@smta.org](mailto:smta@smta.org)

**Additional copies of this publication are available from:**

Curran Associates, Inc.  
57 Morehouse Lane  
Red Hook, NY 12571 USA  
Phone: 845-758-0400  
Fax: 845-758-2633  
Email: [curran@proceedings.com](mailto:curran@proceedings.com)  
Web: [www.proceedings.com](http://www.proceedings.com)

# TABLE OF CONTENTS

## Opening Session: Business and Marketing Issues of Wafer-Level and IC Packaging

### [The Expansion of Wafer-Level Packaging: Challenges and Opportunities.....1](#)

E. Jan Vardaman, *TechSearch International, Inc.*

### [The IC Packaging World and Its Latest Developments.....3](#)

Sandra L. Winkler, *Electronic Trend Publications*

## WAFER-LEVEL PACKAGING AND PROCESS MATERIALS TRACK

### Session 1

#### [RF Crosstalk Suppression Based on Wafer-Level Packaging Concept.....5](#)

S.M. Sinaga, A. Polyakov, M. Bartek, and J.N. Burghartz, *Delft Institute of Microelectronics and Submicron Technology*

#### [Wafer Level Stacking of 8 to 10 Dice per mm for Consumer Products – Wireless Die-on-Die “WDoD”.....10](#)

Christian Val, Ph.D. and Pascal Couderc, Ph.D., *3D PLUS*

#### [Squeegee Influence on Bump Metrics for Stencil Printed Wafers.....16](#)

Jeff Schake, *DEK USA Inc.* and Guy Burgess, *Flip Chip International, LLC*

### Session 3

#### [Fabrication of Tapered Through-Vias on \(100\) Silicon for Wafer-Level Packaging.....22](#)

Huang Shuang Wu and Chia Yong Poo, *Micron Semiconductor Asia Pte Ltd.*

#### [Lithography-Grade Controlled Expansion Substrates for Wafer Level Packaging.....28](#)

Greg Rudd and Bob Cronk, *SMI (Spectra-Mat, Inc.)*

### Session 5

#### [Su-8 Bonding for Transparent Packaging.....32](#)

C. Brubaker, T. Matthias and M. Wimplinger, *EV Group*

#### [Metrology for Ultra-Thin Wafer and Die Strength Characterization and Related Edge Damage and Modeling Challenges .....39](#)

David Liu, Anwei Liu, Michael I. Current, Wojtek J. Walecki, and Ann Koo, *Frontier Semiconductor*

#### [Utilization of Die Attach Adhesives in Wafer Level Assembly of Cavity Packages for Image Sensors.....42](#)

G. Humpston and M. Nystrom, *Tessera Inc.*; S. Kanagavel, M. Previti, and M. Wilson, *Cookson Electronics Inc.*

### Session 7

#### [BCB Wafer Bonding with Electrical Interconnects.....48](#)

Praveen Pandojirao-S, Rachita Dewan, Dan O. Popa, and J.-C. Chiao, *Automation & Robotics Research Institute, University of Texas at Arlington*

#### [Wafer-to-Wafer and Chip-to-Wafer Integration Schemes for Systems-in-a-Package and 3D Interconnects.....54](#)

Thorsten Matthias, Stefan Pargfrieder, Herwig Kirchberger, Markus Wimplinger, and Paul Lindner, *EV Group*

#### [Pattern Effects on Electroplated Copper Pillars.....61](#)

Arthur Keigler, Bill Wu, Jim Zhang, and Zhenqiu Liu, *NEXX Systems, Inc.*

## Session 9

### **C4NP – Data for Fine Pitch to CSP Flip Chip Solder Bumping.....65**

Eric Laine and Klaus Ruhmer, *SUSS MicroTec, Inc.*; Luc Belanger and Michel Turgeon, *IBM Canada Ltd.*; Eric Perfecto, Hai Longworth, and David Hawken, *IBM Microelectronics*

### **An Integrated Deep Silicon Etch/Directional Physical Vapor Deposition Process for Through-Wafer Via Applications.....72**

G. Reynolds, C. Constantine, S. Lai, K. Mackenzie, R. Westerman, D. Johnson, C. Johnson, and R. Benz, *Oerlikon USA, Inc.*; J-B Chevrier, *Oerlikon France*; J. Weichart, S. Kadlec, M. Elghazzali, H. Hirscher, and H. Auer, *OC Oerlikon Balzers Limited*

### **Study of Ni-P/Pd/Au as a Final Finish for Wafer.....78**

Kazuki Yoshikawa, Toshiaki Shibata, Masayuki Kiso, and Shigeo Hashimoto, *C. Uyemura & Company, Ltd.*; Don Gudczauskas, *Uyemura International Corporation*

## Session 11

### **Advanced Plasma Processing Techniques for Improving Descum and Other WLP Process Performance.....82**

Scott D. Szymanski, *March Plasma Systems*

### **Using the 2D Macro CD Metrology Package to Measure CD Lines.....87**

Rajiv Roy, Matt Wilson, and Chris Hawes, *Rudolph Technologies*

### **Surface Cleaning Flip Chip Wafers for Test and Assembly Improvements.....91**

Terence Collier, *CVInc.*

### **Non Lithographic Microcell Plating for Integrated Passives and RDL.....98**

P. Möller and M. Fredenberg, *Replisaurus Technologies AB*; P. Leisner, *Acreo AB*; M. Ostling, *Royal Institute of Technology, IMIT*

## 3D, STACKED AND NOVEL DIE PACKAGING TRACK

## Session 2

### **Assembling Optical Devices Utilizing Wafer Level Technology and Chip on Board Process to Enable Higher Yields and Reduced Costs.....102**

Yehudit Dagan, Giles Humpston, and Michael J. Nystrom, *Tessera Inc.*

### **Hybrid Wafer-Level Packaging for RF-MEMS Applications.....106**

J. Iannacci, R. Gaddi, and A. Gnudi, *ARCES-DEIS Università di Bologna*; J. Iannacci, M. Bartek, J. Tian, S. Sosin, and A. Akhnoukh, *HiTeC-DIMES, Delft University of Technology*

### **UTCP: 60µm Thick Bendable Chip Package.....114**

W. Christiaens, B. Vandeveld, E. Bosman, and J. Vanfleteren, *IMEC/TFCG Microsystems*

### **Copper Panel Fabrication and Stacking Concept for VLP FB DIMMS.....120**

Peter Salmon, *Peter C. Salmon, LLC*

## Session 4

### **Single Wafer Bumping.....128**

Yixiang Xie, Qiang Fu, and Solomon Basame, *Surfact Technologies, Inc.*

### **SiP – Identifying Issues for Stacked (3D) Multichip Packaging Adoption.....131**

Larry Gilg, *Die Products Consortium*

### **Challenges in Flip Chip Die Sorting, Handling and Inspection.....135**

Gerald Steinwasser, *Mühlbauer, Inc.*

#### Session 6

**Overview of MEMS Wafer Level Processes and Patents.....140**

Ken Gilleo, Ph.D., *ET-Trends LLC*

**Effects of Plasma Pretreatment on Flip Chip and CSP Substrate Level Assembly Yield and Reliability.....147**

Daniel Baldwin, Ph.D., *Georgia Institute of Technology*; Paul Houston and Brian Lewis, *Engent, Inc.*

**Embedded IC Polyimide Multi-Layer Substrate.....157**

M. Okamoto, S. Ito, S. Okude, T. Suzuki, O. Nakao, T. Ito, and R. Yamauchi, Ph.D., *Fujikura Ltd.*

**Stair-Step IC Packages for Low Cost and High Performance.....161**

Joseph Fjelstad, *SiliconPipe, Inc.*

#### Session 8

**Advanced Package Prototyping Using Nano-Particle Silver Printed Interconnects.....167**

Sungchul Joo and Daniel F. Baldwin, Ph.D., *Georgia Institute of Technology*

**DRIE with High Rate and Uniformity for MEMS and WLP.....174**

Leslie Lea, *Surface Technology Systems plc*

**Aerosol-Jet Printing for 3-D Interconnects, Flexible Substrates and Embedded Passives.....179**

Martin Hedges, *Neotech Services MTP*; Mike Kardos, Bruce King, and Mike Renn, *Optomec Inc.*

#### Session 10

**Study on Adhesion of Dicing Die Attach Two-in-One Film for 3-D Stack Packaging.....184**

Shijian Luo, Ph.D. and Tom Jiang, Ph.D., *Micron Technology Inc.*

**Placing Wafer Level Devices in a High Speed Workflow.....189**

Gheorghe Pascariu, *Hover-Davis Inc.*

#### Session 12

**Methodology for Stacking of Power Semiconductors for the Harsh Automotive Environment.....193**

Todd P. Oman, *Delphi Corporation*

**White Ring Defect Formation in Lead-Free Wafer Level Packaging.....199**

Kimberly D. Pollard, Ph.D., Raymond Chan, Ph.D., and Diane Scheele, *Dynaloy, LLC*

**Formation of Lead-Free Microbumps by Electroplating for Flip-Chip and WLP Applications.....203**

R. Kiumi, F. Kuriyama, and N. Saito, *Precision Machinery Co., Ebara Corp.*

#### Poster Session

**Wafer-Level Packaging: Effective Cost Reduction with Wafer Bonding.....210**

Thorsten Matthias, Markus Wimplinger, and Paul Lindner, *EV Group*