## 12th Annual International Wafer-Level Packaging Conference (IWLPC 2015)

Interconnecting WLP, MEMS & 2.5/3D Integration

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	Session	ns at a Glance: Tuesday, Od	ctober 13		
7:00 AM	Pagistration Opens				
	WLP TRACK   MONTEREY ROOM Session 1: Fan Out WLP Technologies and Applications	3D TRACK   SAN CARLOS ROOM Session 2 - TSV Processing Considerations	MEMS TRACK   SANTA CLARA Session 3 - MEMS and Sensor Packaging Solutions		
8:30 AM	Fan-Out Wafer Level Packaging: Market and Technology TrendsN/A Thibault Buisson, Yole Développement	A Study of Microbump Metrology and Defectivity at 20um Pitch and Below for 3D TSV Stacking12 Maarten Liebens, IMEC	Full Hermetic 3D Wafer-Level-Packaging for LED and Sensor ModulesN/A Martin Wilke, P.Eng., Fraunhofer IZM		
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	Low Stress And Volatile-Free Spin-On Dielectric Silicone Solution For Wafer-Level Packaging Applications1 Byung Hwang Ph.D., Dow Corning Europe S.A	Methods for Assembly of TSV Products20 Tom Strothmann, Kulicke & Soffa	SiP's for Internet of Things (lot)– 3D CIS/IC and MEMS/IC IntegrationN/A John Lau, Ph.D., ASM		
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10:30 AM	Refreshment Break Exhibit Hall				
11:10 AM	Welcome Comments - Steven Xu, Ph.D., Qualcomm, Conference Chair				
11:20 AM	Keynote Address: Rama Alapati, Director of GLOBALFOUNDRIES - Package Architecture & Customer Technology (PACT) High Density Fan-Out:  Evolution or Revolution OAK BALLROOM (2ND FLOOR)  Lunch Break				
12:15 PM					
	WLP TRACK   MONTEREY ROOM Session 4 - Fan-Out WLCSP	3D TRACK   SAN CARLOS ROOM Session 5 – 3D and TSV Metrology Methodologies	MEMS TRACK   SANTA CLARA Session 6 - MEMS Process Technologies		
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3:15 PM	Refreshment Break Exhibit Hall				
4:00 PM	Panel Discussion: Fan-Out WLP Panel Processing OAK BALLROOM (2nd FLOOR)				
	Moderator: Jan Vardaman, President, TechSearch International, Inc. Panelists: Jose Campos, NANIUM, S.A. Bill Chen, ASE Tim Olson, Deca Technologies Beth Keser, Ph.D., Qualcomm Thomas Uhrmann, EV Group				
5:30pm -	Exhibitor Reception Exhibit Hall				

	Sessio	ns at a Glance: Wednesday, Oc	tober 14		
7:00 AM	Registration Opens Bayshore Foyer				
8:30 AM	Keynote Address: Sitaram Arkalgud, VP of Invensas - 2.5D/3D IC,Examining Low Cost Alternatives OAK BALLROOM (2ND FLOOR)				
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3:15 PM	Refreshment Break Exhibit Hall				
	WLP TRACK   MONTEREY ROOM	3D TRACK   SAN CARLOS ROOM	WLP TRACK   SANTA CLARA		
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