
Advanced Gate Stack, Source/Drain, and Channel Engineering for Si-Based CMOS 5: New Materials, Processes, and Equipment

Editors:

V. Narayanan

IBM T.J. Watson Research Center
Yorktown Heights, New York, USA

D-L. Kwong

Institute of Microelectronics
Singapore

E. P. Gusev

Qualcomm MEMS Technologies
San Jose, California, USA

F. Roozeboom

NXP Semiconductors Research
and University of Technology
Eindhoven, The Netherlands

H. Iwai

Tokyo Institute of Technology
Yokohama, Japan

P. J. Timans

Mattson Technology Inc.
Fremont, California, USA

Sponsoring Divisions:



Electronics and Photonics



Dielectric Science & Technology



High Temperature Materials



Published by

The Electrochemical Society

65 South Main Street, Building D
Pennington, NJ 08534-2839, USA

tel 609 737 1902

fax 609 737 2743

www.electrochem.org

ecstransactions™

Vol. 19 No. 1

Copyright 2009 by The Electrochemical Society.
All rights reserved.

This book has been registered with Copyright Clearance Center.
For further information, please contact the Copyright Clearance Center,
Salem, Massachusetts.

Published by:

The Electrochemical Society
65 South Main Street
Pennington, New Jersey 08534-2839, USA

Telephone 609.737.1902
Fax 609.737.2743
e-mail: ecs@electrochem.org
Web: www.electrochem.org

ISSN 1938-6737 (online)
ISSN 1938-5862 (print)

ISBN 978-1-56677-709-4 (Hardcover)
ISBN 978-1-60768-059-8 (PDF)

Printed in the United States of America.

ECS Transactions, Volume 19, Issue 1
Advanced Gate Stack, Source/Drain, and Channel Engineering for Si-Based CMOS 5:
New Materials, Processes, and Equipment

Table of Contents

Preface *iii*

Chapter 1
Keynote Address

Revolutionary Nanoelectronic Devices and Processes for Post 32nm CMOS Era 3
Y. Nishi

Chapter 2
Technologies for Advanced Electronics

Light up the Future of Silicon Microprocessors * 17
J. Liu, M. Beals, J. Michel and L. Kimerling

High-k Dielectrics and Metal Gates for Future Generation Memory Devices * 29
*J. A. Kittl, K. Opsomer, M. Popovici, N. Menou, B. Kaczer, X. P. Wang,
C. Adelman, M. A. Pawlak, K. Tomida, A. Rothschild, B. Govoreanu,
R. Degraeve, M. Schaekers, M. Zahid, A. Delabie, J. Meersschaut, W. Polspoel,
S. Clima, G. Pourtois, W. Knaepen, C. Detavernier, V. Afanas'ev, T. Blomberg,
D. Pierreux, J. Swerts, P. Fischer, J. W. Maes, D. Manger, W. Vandervorst,
T. Conrad, A. Franquet, P. Favia, H. Bender, B. Brijs, S. Van Elshocht,
M. Jurczak, J. Van Houdt and D. J. Wouters*

Temperature Influence on Nanocrystals Embedded High-k Nonvolatile Memory 41
Characteristics
C. Yang, Y. Kuo, C. Lin and W. Kuo

Nanoelectromechanical Logic and Memory Devices * 49
K. Akarvardar and H. Wong

Chapter 3

Short-Time Annealing - Dopant Activation & Diffusion

Millisecond Annealing Junctions for Near-Scaling-Limit Bulk CMOS Using Raised Source/Drain Extensions *	63
<i>M. Hane</i>	
Boron Diffusion Behavior During the Formation of Shallow p ⁺ /n Junction Using the Combination of Ge Pre-amorphization Implantation, Pre-Annealing RTA and Post-Annealing Non-Melt Excimer Laser(NLA) Processes	71
<i>S. Aid, S. Matsumoto, T. Suzuki, G. Fuse and T. Nakazawa</i>	
Flash Lamp Activation of n- and p-type Dopants in Strained and Unstrained SOI and HOI	79
<i>R. A. Minamisava, D. Buca, W. Heiermann, F. Lanzerath, S. Mantl, W. Skorupa, J. Hartmann, B. Ghyselen, N. Kernevez and U. Breuer</i>	
Ultra-Shallow Junction Formation by Plasma doping and Excimer Laser Annealing	87
<i>L. Jung, S. Do, J. Kim, S. Kong, K. Nam and Y. Lee</i>	
High Temperature Ion Implantation: a Solution for n-Type Junctions in Strained Silicon	95
<i>W. Heiermann, D. Buca, H. Trinkaus, B. Holländer, U. Breuer, N. Kernevez, B. Ghyselen and S. Mantl</i>	
Atomic Layer Deposition of Antimony Oxide on Hydrogen-terminated Silicon Substrates	105
<i>B. Kalkofen, S. Matichyn and E. Burté</i>	

Chapter 4

Shallow Junction Metrology

Dopant and Carrier Concentration Profiling with Atomic Resolution by Scanning Tunneling Microscopy *	117
<i>T. Kanayama, M. Nishizawa and L. Bolotov</i>	
Characterization of Annealing Effects in Ultra-Shallow Boron-Implanted Si Wafers using Raman Scattering	127
<i>M. Fukumoto, H. Minami, N. Hasuike, H. Harima, M. Yoshimoto and W. Yoo</i>	
The Evaluation of State-of-the-Art Front-End Structures by the Differential Hall Effect Continuous Anodic Oxidation Technique	135
<i>S. A. Prussin and J. Reyes</i>	

Photoluminescence Study on Ion Implanted Silicon after Rapid Thermal Annealing	147
<i>S. Takashima, M. Yoshimoto and W. Yoo</i>	

Chapter 5 Novel Channel Engineering

Opportunities and Challenges for Germanium and Silicon-Germanium Channel p-FETs *	155
<i>S. W. Bedell, N. Daval, K. Fogel, K. Shimizu, J. Ott, J. Newbury and D. Sadana</i>	
Ge/GeO ₂ Interface Control with High Pressure Oxidation for Improving Electrical Characteristics	165
<i>C. Lee, T. Tabata, T. Nishimura, K. Nagashio, K. Kita and A. Toriumi</i>	
RF Sputtered Er ₂ O ₃ Thin Films as High-k Gate Dielectrics for Germanium MOS Devices	175
<i>G. C. Deepak and N. Bhat</i>	
The Influence of the Epitaxial Growth Process Parameters on Layer Characteristics and Device Performance in Si-passivated Ge pMOSFETs *	183
<i>M. R. Caymax, F. Leys, J. Mitard, K. Martens, L. Yang, G. Pourtois, W. Vandervorst, M. Meuris and R. Loo</i>	
Defects, Junction Leakage and Electrical Performance of Ge pFET Devices *	195
<i>G. Eneman, E. Simoen, R. Yang, B. De Jaeger, G. Wang, J. Mitard, G. Hellings, D. Brunco, R. Loo, K. De Meyer, M. R. Caymax, C. Claeys, M. Meuris and M. Heyns</i>	
Fabrication of Suspended Ge-rich Nanowires by Ge Enrichment Technique for Multi-channel Devices	207
<i>E. D. Saracco, J. Damlencourt, D. Lafond, S. Bernasconi, V. Benevent, P. Rivallin, Y. Morand, J. Hartmann, P. Gautier, C. Vizioz, T. Ernst, C. Bonafos and P. Fazzini</i>	
Influence of Interfacial Oxygen and Carbon on Misfit Dislocation Generation in SiGe Epitaxial Layers	213
<i>M. Fukuda, Y. Shimamune, K. Tanahashi, K. Ikeda, M. Nishikawa, H. Maekawa, N. Tamura, T. Mori, A. Shimizu and M. Kase</i>	
The Challenges in Introducing PMOS Dual Channel in CMOS Processing *	223
<i>H. R. Harris, P. Majhi, P. D. Kirsch, P. Sivasubramani, J. Oh and S. Song</i>	

The Effect of NH₃ on the Interface of HfO₂ and Al₂O₃ Films on GaAs (100) Surfaces 233

D. Suh, Y. Cho, D. Ko, K. Chung, M. Cho and Y. Lee

Chapter 6 Advanced Gate Stacks

On the Origin of Anomalous V_{TH} Shift in high-k MOSFETs * 243

A. Toriumi and K. Kita

Engineering Band-Edge High- κ /Metal Gate n-MOSFETs with Cap Layers Containing Group IIA and IIIB Elements by Atomic Layer Deposition 253

H. Jagannathan, L. F. Edge, P. Jamison, R. Iijima, V. Narayanan, V. Paruchuri, R. Clark, S. Consiglio, C. Wajda and G. Leusink

Electrical and Materials Characterization of Reactive and Co-Sputtered Tantalum Carbide Metal Electrodes for High-K Gate Applications 263

L. F. Edge, T. Vo, A. Kellock, B. Linder, J. Bruley, Y. Zhu, P. DeHaven, V. Paruchuri, T. Tsunoda, A. Venkateshan and S. Shinde

Dipole Model Explaining High-k/Metal Gate Threshold Voltage Tuning * 269

P. D. Kirsch, P. Sivasubramani, J. Huang, C. D. Young, C. S. Park, K. Freeman, M. M. Hussain, G. Bersuker, H. R. Harris, P. Majhi, P. Lysaght, H. Tseng, B. H. Lee and R. Jammy

Modeling the Influence of Defects on the Electrical Response of Multi-Dielectric Gate-Stack Structures 277

H. P. Hjalmarson and R. Devine

Low Voltage SILC Analysis for High-k/metal Gate Dielectrics 283

N. Rahim and D. Misra

Hafnium Oxide Etching Using Hydrogen Chloride Gas 289

H. Habuka, Y. Kobori, M. Yamaji, S. Horii and Y. Kunii

Chapter 7 Contacts

Three-Dimensional Atom-Probe Tomographic Studies of Nickel Monosilicide/Silicon Interfaces on a Subnanometer Scale *	303
<i>P. Adusumilli, C. E. Murray, L. J. Lauhon, O. Avayu, Y. Rosenwaks and D. N. Seidman</i>	
Electrical and Wafer Surface Profile Characterization of NiSi Formation Process using a Four Point Probe and Optical Surface Profilometer	315
<i>W. Yoo, T. Ueda, T. Ishigaki and K. Kang</i>	
Integration of Al Segregated NiSiGe/SiGe Source/Drain Contact Technology in p-FinFETs for Drive Current Enhancement	323
<i>M. Sinha, R. Lee, S. Devi, G. Lo, E. Chor and Y. Yeo</i>	
Properties of ErSi(2-x) Contacts Formed on Si(1-x)C(x) Epitaxial Layers	331
<i>E. Alptekin, M. Ozturk, V. Misra, Y. Cho, Y. Kim and S. Chopra</i>	
UHV Fabrication of the Ytterbium Silicide as Potential Low Schottky Barrier S/D Contact Material for N-Type MOSFET	339
<i>D. A. Yarekha, G. Larrieu, N. Breil, E. Dubois, S. Godey, X. Wallart, C. Soyer, D. Remiens, N. Reckinger, X. Tang, A. Laszcz, J. Ratajczak and A. Halimaoui</i>	
Enhancement of Carrier Ballistic Transport in Schottky S/D MOSFETs	345
<i>W. Wang, H. Tsuchiya and M. Ogawa</i>	
Author Index	351

* invited paper