

# **2016 International Symposium on Rapid System Prototyping (RSP 2016)**

**Pittsburgh, Pennsylvania, USA  
6-7 October 2016**



**IEEE Catalog Number: CFP16047-POD  
ISBN: 978-1-5090-3926-5**

**Copyright © 2016, The Association for Computing Machinery (ACM)  
All Rights Reserved**

***\*\*\* This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

|                         |                   |
|-------------------------|-------------------|
| IEEE Catalog Number:    | CFP16047-POD      |
| ISBN (Print-On-Demand): | 978-1-5090-3926-5 |
| ISBN (Online):          | 978-1-4503-4535-4 |
| ISSN:                   | 2150-5500         |

**Additional Copies of This Publication Are Available From:**

Curran Associates, Inc  
57 Morehouse Lane  
Red Hook, NY 12571 USA  
Phone: (845) 758-0400  
Fax: (845) 758-2633  
E-mail: [curran@proceedings.com](mailto:curran@proceedings.com)  
Web: [www.proceedings.com](http://www.proceedings.com)

CURRAN ASSOCIATES INC.  
**proceedings**  
.com

# Table of Contents

|                                                                                                         |     |
|---------------------------------------------------------------------------------------------------------|-----|
| Conference Committees.....                                                                              | iii |
| <hr/>                                                                                                   |     |
| <b>Session 1 – Keynote</b>                                                                              |     |
| <hr/>                                                                                                   |     |
| <b>Keynote:</b> Rethinking Memory System Design.....                                                    | 1   |
| <i>Onur Mutlu, ETH Zurich and Carnegie Mellon University</i>                                            |     |
| <hr/>                                                                                                   |     |
| <b>Session 2 – Virtualization and Visualization</b>                                                     |     |
| <hr/>                                                                                                   |     |
| <b>Invited paper:</b> Embedded Virtualization for the Design of Secure IoT Applications.....            | 2   |
| <i>Carlos Moratelli, Sergio Johann Filho, Marcelo Neves and Fabiano Hessel</i>                          |     |
| <b>Invited paper:</b> MORPh: Mobile OLED Power Friendly Camera System.....                              | 7   |
| <i>Xiang Chen, Jiachen Mao, Jiafei Gao, Kent Nixon, and Yiran Chen</i>                                  |     |
| <hr/>                                                                                                   |     |
| <b>Session 3 – Embedded Systems for Medical Applications</b>                                            |     |
| <hr/>                                                                                                   |     |
| A HW/SW Embedded System for Accelerating Diagnosis of Glaucoma From Eye Fundus Images .....             | 12  |
| <i>Paulo Cezar Dantas Junior, Andrea Sarmento and Adriano Sarmento</i>                                  |     |
| EEGu2: An Embedded Device for Brain/Body Signal Acquisition and Processing .....                        | 19  |
| <i>Shen Feng, Mian Tang, Fernando Quivira, Tim Dyson, Filip Cuckov and Gunar Schirner</i>               |     |
| <hr/>                                                                                                   |     |
| <b>Session 4 – Performance and Prototyping with FPGAs</b>                                               |     |
| <hr/>                                                                                                   |     |
| Automatic Detection and Elision of Reset Sub-Circuits.....                                              | 26  |
| <i>Panagiotis Patros and Kenneth Kent</i>                                                               |     |
| Architectural Performance Analysis of FPGA Synthesized LEON Processors.....                             | 33  |
| <i>Corentin Damman, Gregory Edison, Fabrice Guet, Eric Noulard, Luca Santinelli and Jérôme Hugues</i>   |     |
| On-Board Non-Regression Test of HLS Tools Targeting FPGA .....                                          | 41  |
| <i>Arief Wicaksana, Adrien Prost-Boucle, Olivier Muller, Arif Sasongko and Frédéric Rousseau</i>        |     |
| <hr/>                                                                                                   |     |
| <b>Session 5 – Real-time</b>                                                                            |     |
| <hr/>                                                                                                   |     |
| <b>Invited paper:</b> On platforms for CPS - adaptive, predictable and efficient.....                   | 48  |
| <i>Lothar Thiele, Felix Sutton, Romain Jacob, Reto da Forno and Jan Beutel</i>                          |     |
| Overloads in Compositional Embedded Real-Time Control Systems .....                                     | 51  |
| <i>Akramul Azim</i>                                                                                     |     |
| Efficient Parallel Multi-Objective Optimization for Real-time Systems Software Design Exploration ..... | 58  |
| <i>Rahma Bouaziz, Laurent Lemarchand, Frank Singhoff, Bechir Zalila and Mohamed Jmaiel</i>              |     |
| Design of an Expandable Real-time Simulation (eRTS) Platform for Multi-level Rapid Prototyping.....     | 65  |
| <i>Ankurkumar Patel, Troy Silloway, Fnu Qinggele and Yong-Kyu Jung</i>                                  |     |
| Architecture Exploration of Intelligent Robot System using ROS-compliant FPGA Component .....           | 72  |
| <i>Takeshi Ohkawa, Kazushi Yamashina, Takuya Matsumoto, Kanemitsu Ootsu and Takashi Yokota</i>          |     |
| <hr/>                                                                                                   |     |
| <b>Session 6 – System-on-Chip Prototyping and Simulation</b>                                            |     |
| <hr/>                                                                                                   |     |
| Rapid SoC Prototyping Utilizing Quilt Packaging Technology For Modular Functional IC Partitioning ..... | 79  |
| <i>Tian Lu, Jason Kulick, Carlos Ortega, Gary H. Bernstein, Scott Ardisson and Rob Engelhardt</i>       |     |

|                                                              |    |
|--------------------------------------------------------------|----|
| RapidSoC: Short Turnaround Creation of FPGA Based SoCs ..... | 86 |
| <i>Jakob Wenzel and Christian Hochberger</i>                 |    |

---

## Session 7 – Exploration and Design of Systems

---

|                                                                                                              |     |
|--------------------------------------------------------------------------------------------------------------|-----|
| Simulation driven insertion of data prefetching instructions for early software-on-SoC optimization .....    | 93  |
| <i>Perrin Njoyah Ntafam, Eric Paire, Alain Clouard and Frédéric Petrot</i>                                   |     |
| HAMEX: Heterogeneous Architecture and Memory Exploration framework .....                                     | 100 |
| <i>Kasra Moazzemi, Roger Chen-Ying Hsieh and Nikil Dutt</i>                                                  |     |
| Inter-FPGA Routing Environment for Performance Exploration of Multi-FPGA Systems .....                       | 107 |
| <i>Umer Farooq, Roselyne Chotin-Avot, Moazzam Azeem, Maminionja Ravoson and Habib Mehrez</i>                 |     |
| Model-driven Design & Synthesis of the SHA-256 Cryptographic Hash Function in ReWire .....                   | 114 |
| <i>William Harrison, Adam Procter and Gerard Allwein</i>                                                     |     |
| Schedulability-Guided Exploration of Multi-core Systems .....                                                | 121 |
| <i>Rabeh Ayari, Imane Hafnaoui, Giovanni Beltrame and Gabriela Nicolescu</i>                                 |     |
| Transforming VHDL Descriptions into Formal Component-based Models .....                                      | 128 |
| <i>Ayoub Nouri, Rahma Benatitallah, Anca Molnos, Christian Fabre, Frederic Heitzmann and Olivier Debicki</i> |     |