

2017 IEEE 35th VLSI Test Symposium (VTS 2017)

**Las Vegas, Nevada, USA
9-12 April 2017**



**IEEE Catalog Number: CFP17029-POD
ISBN: 978-1-5090-4483-2**

**Copyright © 2017 by the Institute of Electrical and Electronics Engineers, Inc
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP17029-POD
ISBN (Print-On-Demand):	978-1-5090-4483-2
ISBN (Online):	978-1-5090-4482-5
ISSN:	1093-0167

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

TABLE OF CONTENTS

A TECHNIQUE FOR DYNAMIC RANGE IMPROVEMENT OF INTERMODULATION DISTORTION PRODUCTS FOR AN INTERPOLATING DAC-BASED ARBITRARY WAVEFORM GENERATOR USING A PHASE SWITCHING ALGORITHM.....	1
<i>Peter Sarson ; Shohei Shibuya ; Tomonori Yanagida ; Haruo Kobayashi</i>	
ACCURATE JITTER DECOMPOSITION IN HIGH-SPEED LINKS	7
<i>Yan Duan ; Degang Chen</i>	
ADAPTIVE TEST FLOW FOR MIXED-SIGNAL ICS	13
<i>Haralampos-G. Stratigopoulos ; Christian Streitwieser</i>	
A NEW DELAY TESTING SIGNAL SCHEME ROBUST TO POWER DISTRIBUTION NETWORK IMPEDANCE VARIATION	19
<i>Claude Thibeault ; Ali Louati</i>	
AGING MONITOR REUSE FOR SMALL DELAY FAULT TESTING.....	25
<i>Chang Liu ; Michael A. Kochte ; Hans-Joachim Wunderlich</i>	
AN OPTIMISED SDD ATPG AND SDQL COMPUTATION METHOD ACROSS DIFFERENT PATTERN SETS	31
<i>Wilson Pradeep ; Prakash Narayanan ; Rubin Parekhji</i>	
INNOVATIVE PRACTICES SESSION 1C SCREENING FOR LAYOUT SENSITIVE DEFECTS.....	37
<i>Arani Sinha ; Nitin Chaudhary</i>	
FAIL DATA REDUCTION FOR DIAGNOSIS OF SCAN CHAIN FAULTS UNDER TRANSPARENT-SCAN	38
<i>Irith Pomeranz</i>	
METHODOLOGY OF GENERATING DUAL-CELL-AWARE TESTS.....	44
<i>Yu-Hao Huang ; Ching-Ho Lu ; Tse-Wei Wu ; Yu-Teng Nien ; Ying-Yen Chen ; Max Wu ; Jih-Nung Lee ; Mango C. -T. Chao</i>	
TEST-SET REORDERING FOR IMPROVING DIAGNOSABILITY	50
<i>Cheng Xue ; R. D. Blanton</i>	
INNOVATIVE PRACTICES SESSION 2C: “HOW IS INDUSTRY SIMPLIFYING ANALOG TEST”	56
<i>Rubin A. Parekhji ; Srinivas Modekurty</i>	
FAST WAT TEST STRUCTURE FOR MEASURING VT VARIANCE BASED ON LATCH-BASED COMPARATORS	57
<i>Kao-Chi Lee ; Kai-Chiang Wu ; Chih-Ying Tsai ; Mango Chia-Tso Chao</i>	
FLIP-FLOP CLUSTERING BASED TRACE SIGNAL SELECTION FOR POST-SILICON DEBUG	63
<i>Yun Cheng ; Huawei Li ; Ying Wang ; Yingke Gao ; Bo Liu ; Xiaowei Li</i>	
HLDTL: HIGH-PERFORMANCE, LOW-COST, AND DOUBLE NODE UPSET TOLERANT LATCH DESIGN.....	69
<i>Aibin Yan ; Zhengfeng Huang ; Maoxiang Yi ; Jie Cui ; Huaguo Liang</i>	
INNOVATIVE PRACTICES SESSION 3C HARDWARE SECURITY.....	75
<i>Jv Rajendran ; Peilin Song ; Suriya Natarajan</i>	
INNOVATIVE PRACTICES SESSION 4A VARIATION-TOLERANT DESIGN OF CIRCUITS/SYSTEMS	76
<i>Arijit Raychowdhury</i>	
SPECIAL SESSION ON EARLY LIFE FAILURES	77
<i>Jyotirmoy Deshmukh ; Wolfgang Kunz ; Hans-Joachim Wunderlich ; Sybille Hellebrand</i>	
INNOVATIVE PRACTICES SESSION 4C DATA ANALYTICS IN TEST	78
<i>Suriya Natarajan ; Abhijit Sathaye</i>	
A METHODOLOGY FOR ESTIMATING MEMORY LIFETIME USING A SYSTEM-LEVEL ACCELERATED LIFE TEST AND ERROR-CORRECTING CODES	79
<i>Dae-Hyun Kim ; Linda Milor</i>	
AT-SPEED CAPTURE GLOBAL NOISE REDUCTION & LOW-POWER MEMORY TEST ARCHITECTURE.....	85
<i>Bonita Bhaskaran ; Sailendra Chadavada ; Shantanu Sarangi ; Nithin Valentine ; Venkat Abilash Reddy Nerallapally ; Ayub Abdollahian</i>	
LEVERAGING SYSTEMATIC UNIDIRECTIONAL ERROR-DETECTING CODES FOR FAST STT-MRAM CACHE.....	91
<i>Nour Sayed ; Fabian Oboril ; Rajendra Bishnoi ; Mehdi B. Tahoori</i>	

AN ANALYTICAL MODEL FOR PREDICTING THE RESIDUAL LIFE OF AN IC AND DESIGN OF RESIDUAL-LIFE METER.....	97
<i>Md Nazmul Islam ; Sandip Kundu</i>	
LEARNING THE PROCESS FOR CORRELATION ANALYSIS	103
<i>Sebastian Siatkowski ; Li-C. Wang ; Nik Sumikawa ; Leroy Winemberg</i>	
PERFORMANCE-AWARE RELIABILITY ASSESSMENT OF HETEROGENEOUS CHIPS	109
<i>Athanasios Chatzidimitriou ; Manolis Kaliorakis ; Sotiris Tselonis ; Dimitris Gizopoulos</i>	
INNOVATIVE PRACTICES SESSION 5C AUTOMOTIVE TEST SOLUTIONS.....	115
<i>Pete Sarson ; Stefano Di Carlo</i>	
A FRAMEWORK FOR FAST TEST GENERATION AT THE RTL	116
<i>Kelson Gent ; Akash Agrawal ; Michael S. Hsiao</i>	
EFFICIENT SAT-BASED GENERATION OF HAZARD-ACTIVATED TSOE TESTS	122
<i>Jan Burchard ; Dominik Erb ; Sudhakar M. Reddy ; Adit D. Singh ; Bernd Becker</i>	
USING PIECEWISE-FUNCTIONAL BROADSIDE TESTS FOR FUNCTIONAL BROADSIDE TEST COMPACTION	128
<i>Irith Pomeranz</i>	
INNOVATIVE PRACTICES SESSION 6C DFT FOR FUNCTIONAL SAFETY.....	134
<i>Prashant Goteti ; Sreejit Chakravarty</i>	
A NOVEL DESIGN-FOR-SECURITY (DFS) ARCHITECTURE TO PREVENT UNAUTHORIZED IC OVERPRODUCTION	135
<i>Ujjwal Guin ; Ziqi Zhou ; Adit Singh</i>	
DYNAMICALLY OBFUSCATED SCAN FOR PROTECTING IPS AGAINST SCAN-BASED ATTACKS THROUGHOUT SUPPLY CHAIN	141
<i>Dongrong Zhang ; Miao He ; Xiaoxiao Wang ; Mark Tehranipoor</i>	
FISCAL: FIRMWARE IDENTIFICATION USING SIDE-CHANNEL POWER ANALYSIS.....	147
<i>Deepak Krishnankutty ; Ryan Robucci ; Nilanjan Banerjee ; Chintan Patel</i>	
INNOVATIVE PRACTICES SESSION 7C AUTOMOTIVE QUALITY ASSURANCE	153
<i>Pete Sarson</i>	
A LOW-COST METHOD FOR SEPARATION AND ACCURATE ESTIMATION OF ADC NOISE, APERTURE JITTER, AND CLOCK JITTER.....	154
<i>Shravan Chaganti ; Li Xu ; Degang Chen</i>	
ANALYSIS OF AN EFFICIENT ON-CHIP SERVO-LOOP TECHNIQUE FOR REDUCED-CODE STATIC LINEARITY TEST OF PIPELINE ADCS.....	160
<i>Guillaume Renaud ; Marc Margalef-Rovira ; Manuel J. Barragan ; Salvador Mir</i>	
KNOB NON-IDEALITIES IN LEARNING-BASED POST-PRODUCTION TUNING OF ANALOG/RF ICs: IMPACT & REMEDIES.....	166
<i>Yichuan Lu ; Georgios Volanis ; Kiruba S. Subramani ; Angelos Antonopoulos ; Yiorgos Makris</i>	
INNOVATIVE PRACTICES SESSION 9B INNOVATIVE PRACTICES IN ASIA-1: FROM QUALITY PERSPECTIVE.....	172
<i>Kazumi Hatayama ; Masahiro Ishida</i>	
INNOVATIVE PRACTICES SESSION 9C DFT AND DATA FOR DIAGNOSTICS	173
<i>Kun Young Chung ; Stefano Di Carlo</i>	
STRUCTURED SCAN PATTERNS RETARGETING FOR DYNAMIC INSTRUMENTS ACCESS.....	174
<i>Ahmed Ibrahim ; Hans G. Kerkhoff</i>	
TEST-COST OPTIMIZATION IN A SCAN-COMPRESSOR ARCHITECTURE USING SUPPORT-VECTOR REGRESSION	180
<i>Zipeng Li ; Jonathon E. Colburn ; Vinod Pagalone ; Kaushik Narayanun ; Krishnendu Chakrabarty</i>	
INNOVATIVE PRACTICES SESSION 10B INNOVATIVE PRACTICES IN ASIA-2: FROM COST PERSPECTIVE	186
<i>Kazumi Hatayama ; Masahiro Ishida</i>	
INNOVATIVE PRACTICES SESSION 10C FORMAL VERIFICATION PRACTICES IN INDUSTRY	187
<i>Huawei Li ; Xiaowei Li</i>	
ASYMMETRIC SIZING: AN EFFECTIVE DESIGN APPROACH FOR SRAM CELLS AGAINST BTI AGING.....	188
<i>Xuan Zuo ; Sandeep K. Gupta</i>	
COMPREHENSIVE INVESTIGATION OF GATE OXIDE SHORT IN FINFETS.....	194
<i>Roya Dibaj ; Dhamin Al-Khalili ; Maitham Shams</i>	
ON-LINE DIAGNOSIS AND COMPENSATION FOR PARAMETRIC FAILURES IN LINEAR STATE VARIABLE CIRCUITS AND SYSTEMS USING TIME-DOMAIN CHECKSUM OBSERVERS.....	200
<i>Md Imran Momtaz ; Suvadeep Banerjee ; Abhijit Chatterjee</i>	

INNOVATIVE PRACTICES SESSION 11C SOC TESTING 206
 Yu Huang
Author Index