

2017 Design, Automation & Test in Europe Conference & Exhibition (DATE 2017)

**Lausanne, Switzerland
27-31 March 2017**

Pages 1-605



**IEEE Catalog Number: CFP17162-POD
ISBN: 978-1-5090-5826-6**

**Copyright © 2017, European Design and Automation Association (EDAA)
All Rights Reserved**

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP17162-POD
ISBN (Print-On-Demand):	978-1-5090-5826-6
ISBN (Online):	978-3-9815370-8-6
ISSN:	1530-1591

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

Technical Program

Monday, 28 March 2017											
1.1	2.2	2.3	2.4	2.5	2.6	2.7	3.0	3.1	3.2	3.3	3.4
3.5	3.6	3.7	3.9	IP1	4.1	4.2	4.3	4.4	4.5	4.6	4.7
Tuesday, 29 March 2017											
5.1	5.2	5.3	5.4	5.5	5.6	5.7	IP2	6.1	6.3	6.4	6.5
6.6	6.7	7.0	7.1	7.2	7.3	7.4	7.5	7.6	7.7	IP3	8.1
8.2	8.3	8.4	8.5	8.6	8.7						
Wednesday, 30 March 2017											
9.1	9.2	9.3	9.4	9.5	9.6	9.7	IP4	10.1	10.2	10.3	10.4
10.5	10.6	10.7	11.0	11.1	11.2	11.3	11.4	11.5	11.6	11.7	11.8
IP5	12.2	12.3	12.4	12.5	12.6	12.7	12.8				

Session	Opening Session: Plenary, Awards Ceremony & Keynote Addresses
Session Code / Room	1.1 / SwissTech, Auditorium
Date / Time	Tuesday, March 28, 2017 / 08:30 – 10:30
Chair	David Atienza, EPFL, CH,
Co-Chair	Giorgio Di Natale, LIRMM, FR,

1.1.1 08:30 – 08:45	WELCOME ADDRESSES.....viii <i>David Atienza and Giorgio Di Natale</i>
1.1.2 08:45 – 09:15	Presentation of Distinguished Awards
1.1.3 09:15 – 09:45	Keynote: Design Automation in the Era of Ai and Iot: Challenges and Pitfalls.....xxxiv <i>Arvind Krishna</i>
1.1.4 09:45 – 10:30	Keynote: A New Era of Hardware Microservices in the Cloud.....xxxv <i>Doug Burger</i>

Session Title	Stochastic, Approximate and Neural Computing
Session Code / Room	2. 2 / 4BC
Date / Time	Tuesday, March 28, 2017 / 11:30 – 13:00
Chair	Lukas Sekanina, Lukas Sekanina,
Co-Chair	Andy Tyrrell, University of York, GB,

2.2.1 11:30 – 12:00	Framework for Quantifying and Managing Accuracy in Stochastic Circuit Design.....1 <i>Florian Neugebauer, Ilia Polian and John P. Hayes</i>
2.2.2 12:00 – 12:30	Energy-Efficient Approximate Multiplier Design using Bit Significance-Driven Logic Compression.....7 <i>Issa Qiqieh, Rishad Shafik, Ghaith Tarawneh, Danil Sokolov and Alex Yakovlev</i>
2.2.3 12:30 – 12:45	Energy-Efficient Hybrid Stochastic-Binary Neural Networks for Near-Sensor Computing.....13 <i>Vincent T. Lee, Armin Alaghi, John P. Hayes, Visvesh Sathe and Luis Ceze</i>

2.2.4
12:45 – 13:00 Accelerator-friendly Neural-network Training: Learning Variations and Defects in RRAM Crossbar.....19
Lerong Chen, Jiawen Li, Yiran Chen, Qiuping Deng, Jiyuan Shen, Xiaoyao Liang and Li Jiang

Session Title	ACache memory management for performance and reliability
Session Code / Room	2.3 / 2BC
Date / Time	Tuesday, 15 March 2017 / 11:30 – 13:00
Chair	Dionisios Pnevmatikatos, Technical University of Crete, GR
Co-Chair	Cristina Silvano, Politecnico di Milano, IT

2.3.1
11:30 – 12:00 Shared Last-level Cache Management for GPGPUs with Hybrid Main Memory.....25
Guan Wang, Xiaojun Cai, Lei Ju, Chuanqi Zang, Mengying Zhao and Zhiping Jia

2.3.2
12:00 – 12:30 Effective Cache Bank Placement for GPUs.....31
Mohammad Sadrosadati, Amirhossein Mirhosseini, Shahin Roozkhosh, Hazhir Bakhishi and Hamid Sarbazi-Azad,

2.3.3
12:30 – 13:00 Soft Error-Aware Architectural Exploration for Designing Reliability Adaptive Cache Hierarchies in Multi-Cores.....37
Arun Subramaniyan, Semeen Rehman, Muhammad Shafique, Akash Kumar and Jörg Henkel

Session Title	Performance and Power Analysis
Session Code / Room	2.4 /3A
Date / Time	Tuesday, March 28, 2017 / 11:30 – 13:00
Chair	Gianluca Palermo, politecnico di Milano, IT
Co-Chair	Ingo Sander, KTH Royal Institute of Technology

2.4.1
11:30 – 12:00 GATSim: Abstract Timing Simulation of GPUs.....43
Kishore Punniyamurthy, Behzad Boroujerdian and Andreas Gerstlauer

2.4.2
12:00 – 12:30 MeSAP: A Fast Analytic Power Model for DRAM Memories.....49
Sandeep Poddar, Rik Jongerius, Leandro Fiorin, Giovanni Mariani, Gero Dittmann, Andreea Anghel and Henk Corporaal

2.4.3
12:30 – 13:00 AFEC: An Analytical Framework for Evaluating Cache Performance in Out-of-Order Processors.....55
Kecheng Ji, Ming Ling, Qin Wang, Longxing Shi and Jianping Pan

Session Title	Reliability and Energy-Efficiency: Two Pillars of NoC Design
Session Code / Room	2.5 / 3C
Date / Time	Tuesday, March 28, 2017 / 11:30 – 13:00
Chair	Sebastien Le Beux, Ecole Central du Lyon, FR,
Co-Chair	Tushar Krishna, Georgia Institute of Technology, US,

2.5.1
11:30 – 12:00 Reliability Assessment of Fault Tolerant Routing Algorithms in Networks-on-Chip: An Analytic Approach.....61
Sadia Moriam and Gerhard P. Fettweis

2.5.2
12:00 – 12:30 Online Monitoring and Adaptive Routing for Aging Mitigation in NoCs.....67
Zana Ghaderi, Ayed Alqahtani and Nader Bagherzadeh

2.5.3 eBSP: Managing NoC Traffic for BSP Workloads on the 16-Core Adapteva Epiphany-
12:30 – 13:00 III Processor.....73
Siddhartha and Nachiket Kapre

Session Title	Advancing Test for Mixed-Signal and Microfluidic Circuits and Systems
Session Code / Room	2.6 / 5A
Date / Time	Tuesday, March 28, 2017 / 11:30 – 13:00
Chair	Andre Ivanov, Univ. BC, CA,
Co-Chair	Marie-Minerve Louerat, Univ. Pierre et Marie Curie, FR,

2.6.1 On the Limits of Machine Learning-Based Test: A Calibrated Mixed-Signal System
11:30 – 12:00 Case Study.....79

Manuel J. Barragan, G. Leger, A. Gines, E. Peralias and A. Rueda

2.6.2 An Extension of Cohn's Sensitivity Theorem to Mismatch Analysis of 1-Port Resistor
12:00 – 12:30 Networks.....85

Sébastien Cliquennois

2.6.3 Testing Microfluidic Fully Programmable Valve Arrays (FPVAs).....91

12:30 – 13:00 *Chunfeng Liu, Bing Li, Bhargab B. Bhattacharya, Krishnendu Chakrabarty, Tsung-Yi Ho and Ulf Schlichtmann*

Session Title	EU Project Special Session: from Secure Clouds to reliable and variable HPC
Session Code / Room	2.7 / 3B
Date / Time	Tuesday, March 28, 2017 / 11:30 – 13:00
Chair	Lorena Anghel, TIMA Laboratory, FR,

2.7.1 HARPA: Tackling Physically Induced Performance Variability.....97

11:30 – 12:00

Nikolaos Zompakis, Michail Noltsis, Lorena Ndreu, Zacharias Hadjilambrou, Panagiotis Englezakis, Panagiota Nikolaou, Antoni Portero, Simone Libutti, Giuseppe Massari, Federico Sassi, Alessandro Bacchini, Chrysostomos Nicopoulos, Yiannakis Sazeides, Radim Vavrik, Martin Golasowski, Jiri Sevcik, Vit Vondrak, Francky Catthoor, William Fornaciari and Dimitrios Soudris

2.7.2 Dynamic Software Randomisation: Lessons Learned From an Aerospace Case Study.....103

12:00 – 12:15

Fabrice Cros, Leonidas Kosmidis, Franck Wartel, David Morales, Jaume Abella, Ian Broster and Francisco J. Cazorla

2.7.3 READEX: Linking Two Ends of the Computing Continuum to Improve Energy-
12:15 – 12:30 efficiency in Dynamic Applications.....109

Per Gunnar Kjeldsberg, Andreas Gocht, Michael Gerndt, Lubomir Riha, Joseph Schuchart and Umbreen Sabir Mian

2.7.4 BASTION: Board and SoC Test Instrumentation for Ageing and No Failure Found.....115

12:30 – 12:45

Artur Jutman, Christophe Lotz, Erik Larsson, Matteo Sonza Reorda, Maksim Jenihhin, Jaan Raik, Hans Kerkhoff, Rene Krenz-Baath and Piet Engelke

2.7.5 RETHINK Big: European Roadmap for Hardware and Networking Optimizations for
12:45 – 13:00 Big Data.....121

Gina Alioto, Paul Carpenter, Adrián Cristal, Osman Unsal, Marcus Leich and Christophe Avare

Session Title	LUNCH TIME KEYNOTE SESSION: Precision Medicine: Where Engineering and Life Science meet
Session Code / Room	3.0 / Garden Foyer
Date / Time	Tuesday, March 28, 2017 / 13:50 - 14:20
chair	David Atienza, EPFL, CH

3.0.1
13:50 – 14:20 Precision Medicine: Where Engineering and Life Science Meet.....xxxvi
Giovanni De Micheli

Session Title	IT&A Session: Parallel Ultra-Low-Power Computing for the IoT: Applications, Platforms, Circuits
Session Code / Room	3.1 / 5BC
Date / Time	Tuesday, March 28, 2017 / 14:30 – 16:00
Organiser	Luca Benini, ETHZ, CH
chair	Luca Benini, ETHZ, CH
co-chair	Danilo Rossi, University of Bologna, IT,

3.1.3
14:30 – 15:00 Better than Worst Case Signoff Strategies for Low Power IoT Devices.....N/A
Jose Pineda de Gyvez, Jose Pineda and Hamed Fatemi

3.1.2
15:00 – 15:30 Gap: An Open-Source Pulp-Riscv Platform for Near-Sensor Analytics.....N/A
Eric Flamand

3.1.3
15:30 – 16:00 Energy-Quality Scalable Adaptive VLSI Circuits and Systems beyond Approximate Computing.....127
Massimo Alioto

Session Title	Hot Topic Session: New Benchmarking Vectors for Emerging Devices, Circuits, and Architectures: Energy, Delay, and ... Accuracy
Session Code / Room	3.2 / 4BC
Date / Time	Tuesday, March 28, 2017/ 14:30 – 16:00
Chair	Xiaobo Sharon Hu, University of Notre Dame, US,
Co-Chair	Pierre-Emmanuel Gaillardon, The University of Utah at Salt Lake City, US,

3.2.1
14:30 – 15:00 Beyond-CMOS Non-Boolean Logic Benchmarking: Insights and Future Directions.....133
Chenyun Pan and Azad Naeemi

3.2.2
15:00 – 15:30 Understanding the Design of IBM Neurosynaptic System and Its Tradeoffs: A User Perspective.....139
Hsin-Pai Cheng, Wei Wen, Chunpeng Wu, Sicheng Li, Hai (Helen) Li and Yiran Chen

3.2.3
15:30 – 16:00 Cellular Neural Network Friendly Convolutional Neural Networks -- CNNs with CNNs.....145
András Horváth, Michael Hillmer, Qiuwen Lou, X. Sharon Hu and Michael Niemier

Session Title	Hardware Trojans and Fault Attacks
Session Code / Room	3.3 /2BC
Date / Time	Tuesday, March 28, 2017 / 14:30 – 16:00
Chair	Ingrid Verbauwhede, KU Leuven, BE
Co-Chair	Ilia Polian, University of Passau, DE

- 3.3.1** Algebraic Fault Analysis of SHA-3.....151
14:30 – 15:00 *Pei Luo, Konstantinos Athanasiou, Yunsu Fei and Thomas Wahl*
- 3.3.2** Evaluating Coherence-exploiting Hardware Trojan.....157
15:00 – 15:30 *Minsu Kim, Sunhee Kong, Boeui Hong, Lei Xu, Weidong Shi and Taeweon Suh*
- 3.3.3** Hardware Trojan Detection Based on Correlated Path Delays in Defiance of Variations
with Spatial Correlations.....163
15:30 – 15:45 *Fatma Nur Esirci and Alp Arslan Bayrakci*
- 3.3.4** Malware Detection using Machine Learning Based Analysis of Virtual Memory Access
Patterns.....169
15:45 – 16:00 *Zhixing Xu, Sayak Ray, Pramod Subramanyan and Sharad Malik*

Session Title	AGuardbanding and Approximation
Session Code / Room	3.4 /3A
Date / Time	Tuesday, March 28, 2017 / 14:30 – 16:00
Chair	Michael Glass, Ulm University, DE,
Co-Chair	Yuko Hara-Azumi, Tokyo Institute of Technology, JP

- 3.4.1** Optimizing Temperature Guardbands.....175
14:30 – 15:00 *Hussam Amrouch, Behnam Khaleghi and Jörg Henkel*
- 3.4.2** The Hidden Cost of Functional Approximation Against Careful Data Sizing -- A Case
Study.....181
15:00 – 15:30 *Benjamin Barrois, Olivier Sentieys and Daniel Menard*
- 3.4.3** High-Level Synthesis of Approximate Hardware under Joint Precision and Voltage
Scaling.....187
15:30 – 16:00 *Seogoo Lee, Lizy K. John and Andreas Gerstlauer*

Session Title	Low-power brain inspired computing for embedded systems
Session Code / Room	3.5 /3C
Date / Time	Tuesday, March 28, 2017/ 14:30 – 16:00
Chair	Johanna Sepulveda, TU Munich, DE,
Co-Chair	Andrea Bartolini, Uniiversita' di Bologna - ETH Zurich, IT

- 3.5.1** Approximate Computing for Spiking Neural Networks.....193
14:30 – 15:00 *Sanchari Sen, Swagath Venkataramani and Anand Raghunathan*
- 3.5.2** Adaptive Weight Compression for Memory-Efficient Neural Networks.....199
15:00 – 15:30 *Jong Hwan Ko, Duckhwan Kim, Taesik Na, Jaeha Kung and Saibal Mukhopadhyay*
- 3.5.3** Real-Time Anomaly Detection for Streaming Data using Burst Code on a Neurosynaptic
Processor.....N/A
15:30 – 15:45 *Qiuwen Chen and Qinru Qiu*

3.5.4 Fast, Low Power Evaluation of Elementary Functions Using Radial Basis Function
15:45 – 16:00 Networks.....208
Parami Wijesinghe, Chamika M. Liyanagedera and Kaushik Roy

Session Title	Mechanisms for hardware fault testing, recovery and metastability management
Session Code / Room	3.6 / 5A
Date / Time	Tuesday, March 28, 2017 / 14:30 – 16:00
Chair	Jaume Abella , <i>Barcelona Supercomputing Center(BSC), ES,</i>
Co-Chair	Maria K. Michael , <i>University of Cyprus, CY,</i>

3.6.1 Charka: A Reliability-Aware Test Scheme for Diagnosis of Channel Shorts Beyond
14:30 – 15:00 Mesh NoCs.....214
Biswajit Bhowmik, Jantindra Kumar Deka and Santosh Biswas

3.6.2 Recovery-Aware Proactive TSV Repair for Electromigration in 3D ICs.....220
15:00 – 15:30 *Shengcheng Wang, Hongyang Zhao, Sheldon X.-D. Tan and Mehdi B. Tahoori*

3.6.3 Near-Optimal Metastability-Containing Sorting Networks.....226
15:30 – 16:00 *Johannes Bund, Christoph Lenzen and Moti Medina*

Session Title	Scheduling and Optimization
Session Code / Room	3.7 / 3B
Date / Time	Tuesday, March 28, 2017 / 14:30 – 16:00
Chair	Rolf Ernst , <i>TU Braunschweig, DE,</i>
Co-Chair	Kai Lampka , <i>Uppsala University, SE,</i>

3.7.1 The Concept of Unschedulability Core for Optimizing Priority Assignment in Real-Time
14:30 – 15:00 Systems.....232
Yecheng Zhao and Haibo Zeng

3.7.2 Utilization Difference Based Partitioned Scheduling of Mixed-Criticality Systems.....238
15:00 – 15:30 *Saravanan Ramanathan and Arvind Easwaran*

3.7.3 Schedulability Using Native Non-Preemptive Groups on an AUTOSAR/OSEK Platform
15:30 – 16:00 with Caches.....244
Leo Hatvani, Reinder J. Bril and Sebastian Altmeyer

Session Title	A tribute to Ralph Otten
Session Code / Room	3.9 / Auditorium
Date / Time	Tuesday, March 28, 2017 / 14:30 - 16:00
Chair	Michael Burstein , <i>CEO Billy.com, CA</i>
Co-Chair	Giovanni De Micheli , <i>EPFL, CH,</i>

3.9.1 Chip design-Physical and Philosophical.....N/A
14:50 – 14:45 *Dave Liu*

3.9.2 Automatic Floorplan Design.....N/A
14:45 – 15:00 *Martin Wong*

3.9.3 The Evolution of Floorplanning.....N/A
15:00 – 15:15 *Antun Domic*

3.9.4 15:15– 15:30	From Silicon Compiler to Physical Synthesis: Ralph Otten's Contributions to EDA.....N/A <i>Patrick Groeneweld</i>
3.9.5 15:30– 15:45	Dealing With Exploding Design Rule Numbers and Complexity.....N/A <i>Raul Camposano</i>
3.9.6 15:45– 16:00	In Memoriam of Ralph Otten: Breaking Down the Complexity of Layout Design Under Moore's Law.....N/A <i>Jochen Jess</i>

Session Title	Interactive Presentations
Session Code / Room	IP1
Date / Time	Tuesday, March 28, 2017 / 16:00 - 16:30
IP1-1	Structural Design Optimization for Deep Convolutional Neural Networks using Stochastic Computing.....250 <i>Zhe Li, Ao Ren, Ji Li, Qinru Qiu, Bo Yuan, Jeffrey Draper and Yanzhi Wang</i>
IP1-2	ApproxQA: A Unified Quality Assurance Framework for Approximate Computing.....254 <i>Ting Wang, Qian Zhang and Qiang Xu</i>
IP1-3	EvoApprox8b: Library of Approximate Adders and Multipliers for Circuit Design and Benchmarking of Approximation Methods.....258 <i>Vojtech Mrazek, Radek Hrbacek, Zdenek Vasicek and Lukas Sekanina</i>
IP1-4	Droop Mitigating Last Level Cache Architecture for STTRAM.....262 <i>Radha Krishna Aluru and Swaroop Ghosh</i>
IP1-5	Modeling Instruction Cache and Instruction Buffer for Performance Estimation of VLIW Architectures using Native Simulation.....266 <i>Omayma Matoussi and Frédéric Pétrot</i>
IP1-6	Analog Fault Testing Through Abstraction.....270 <i>Enrico Fraccaroli and Franco Fummi</i>
IP1-7	BISCC: Efficient Pre Through Post Silicon Validation of Mixed-Signal/RF Systems Using Built In State Consistency Checking.....274 <i>Sabyasachi Deyati, Barry Muldrey and Abhijit Chatterjee</i>
IP1-8	Computing with Nano-Crossbar Arrays: Logic Synthesis and Fault Tolerance.....278 <i>Mustafa Altun, Valentina Cirianni and Mehdi Tahoori</i>
IP1-9	SecureCloud: Secure Big Data Processing in Untrusted Clouds.....282 <i>Florian Kelbert, Franz Gregor, Rafael Pires, Stefan Köpsell, Marcelo Pasin, Aurélien Havet, Valerio Schiavoni, Pascal Felber, Christof Fetzner and Peter Pietzuch</i>
IP1-10	WCET-Aware Parallelization of Model-Based Applications for Multi-Cores: The ARGO Approach.....286 <i>Steven Derrien, Isabelle Puaut, Panayiotis Alefragis, Marcus Bednara, Harald Bucher, Clément David, Yann Debray, Umut Durak, Imen Fassi, Christian Ferdinand, Damien Hardy, Angeliki Kritikakou, Gerard Rauwerda, Simon Rederx, Martin Sicks, Timo Stripf, Kim Sunesen, Timon Ter Braak, Nikolaos Voros, Jürgen Becker</i>
IP1-11	Exploring the Unknown Through Successive Generations of Low Power and Low Resource Versatile Agents.....290 <i>Martin Andraud, Gonenc Berkol, Jaro De Roose, Santosh Gannavarapu, Haoming Xin, Eugenio Cantatore, Pieter J.A. Harpe, Marian Verhelst and Peter G.M. Baltus</i>
IP1-12	Power Profiling of Microcontroller's Instruction Set for Runtime Hardware Trojans Detection without Golden Circuit Models.....294 <i>Faiq Khalid Lodhi, Syed Rafay Hasan, Osman Hasan and Falah Awwadl</i>
IP1-13,	Accounting for Systematic Errors in Approximate Computing.....298 <i>Martin Bruestel and Akash Kumar</i>

IP1-14	Gaussian Mixture Error Estimation for Approximate Circuits.....302 <i>Amin Ghasemazar and Mieszko Lis</i>
IP1-15	Enhancing Symbolic System Synthesis through ASPmT with Partial Assignment Evaluation.....306 <i>Kai Neubauer, Philipp Wanko, Torsten Schaub and Christian Haubelt</i>
IP1-16,	3DFAR: A Three-Dimensional Fabric for Reliable Multi-Core Processors.....310 <i>Javad Bagherzadeh and Valeria Bertacco</i>
IP1-17	Evaluating Impact of Human Errors on the Availability of Data Storage Systems.....314 <i>Mostafa Kishani, Reza Eftekhari and Hossein Asadi</i>
IP1-18	GPUguard: Towards Supporting a Predictable Execution Model for Heterogeneous SoC.....318 <i>Björn Forsberg, Andrea Marongiu and Luca Benini</i>
IP1-19	A Non-Intrusive, Operating System Independent Spinlock Profiler for Embedded Multicore Systems.....322 <i>Lin Li, Philipp Wagner, Albrecht Mayer, Thomas Wild and Andreas Herkersdorf</i>

Session Title	IT&A Session: The Emergence of Silicon Photonics: From High Performance Computing to Data Centers and Quantum Computing
Session Code / Room	4.1 / 5BC
Date / Time	Tuesday, March 28, 2017 / 17:00 – 18:30
Organiser	Luca Carloni, Columbia University, US,

4.1.1 17:00 – 17:30	Energy-Performance Optimized Design of Silicon Photonic Interconnection Networks for High-Performance Computing.....326 <i>Meisam Bahadori, Sébastien Rumley, Robert Polster, Alexander Gazman, Matt Traverso, Mark Webster, Kaushik Patel and Keren Bergman</i>
4.1.2 17:30 – 18:00	Rapid Growth of IP Traffic Is Driving Adoption of Silicon Photonics in Data Centers.....332 <i>Kaushik Patel</i>
4.1.3 18:00 – 18:30	Generation of Complex Quantum States via Integrated Frequency Combs.....336 <i>Christian Reimer, Michael Kues, Piotr Roztock, Benjamin Wetzel, Brent E. Little, Sai T. Chu, Lucia Caspani, David J. Moss and Roberto Morandotti</i>

Session Title	Logic, Interconnects, Neurons: New Realizations
Session Code / Room	4.2 / Konferenz 6
Date / Time	Tuesday, March 28, 2017 / 17:00 – 18:30
Organisers	Jan ter Maten, University of Wuppertal, DE Caren Tischendorf, Humboldt University of Berlin, DE
Chair	Elena Gnani, University of Bologna, IT,
Co-Chair	Aida Todri-Sanial, CNRS-LIRMM, FR,

4.2.1 17:00 – 17:30	Exploiting Transistor-Level Reconfiguration to Optimize Combinational Circuits.....338 <i>Michael Raitza, Akash Kumar, Marcus Völz, Dennis Walter, Jens Trommer, Thomas Mikolajick and Walter M. Weber</i>
4.2.2 17:30 – 18:00	Automatic Place-and-Route of Emerging LED-Driven Wires within a Monolithically-Integrated CMOS+III-V Process.....344 <i>Tushar Krishna, Arya Balachandran, Siau Ben Chiah Li Zhang, Bing Wang, Cong Wang, Kenneth Lee Eng Kian, Jurgen Michel and Li-Shiuan Peh</i>

- 4.2.3** A Tunable Magnetic Skyrmion Neuron Cluster for Energy Efficient Artificial
18:00 – 18:30 Neural Network.....350
Zhezhi He and Deliang Fan

Session Title	Efficient memory design
Session Code / Room	4.3 / 2BC
Date / Time	Tuesday, March 28, 2017 / 17:00 – 18:30
Chair	Francisco Cazorla, CSIC and BSC, ES,
Co-Chair	Cristina Silvano, Politecnico di Milano, IT,

- 4.3.1** STAxCache: An Approximate, Energy Efficient STT-MRAM Cache.....356
17:00 – 17:30 *Ashish Ranjan, Swagath Venkataramani, Zoha Pajouhi, Rangharajan Venkatesan, Kaushik Roy and Anand Raghunathan*

- 4.3.2** Rethinking On-chip DRAM Cache for Simultaneous Performance and Energy
17:30 – 18:00 Optimization.....362
Fazal Hameed and Jeronimo Castrillon

- 4.3.3** An Energy-Efficient Memory Hierarchy for Multi-Issue Processors.....368
18:00 – 18:15 *Tiago Jost, Gabriel Nazar and Luigi Carro*

- 4.3.4** Mapping Granularity Adaptive FTL Based on Flash Page Re-programming.....374
18:15 – 18:30 *Yazhi Feng, Dan Feng, Chenye Yu, Wei Tongz and Jingning Liu*

Session Title	From functional validation to functional qualification
Session Code / Room	4.4 / 3A
Date / Time	Tuesday, March 28, 2017/ 17:00 – 18:30
Chair	Graziano Pravadelli, University of Verona, IT,
Co-Chair	Elena Ioana Vatajelu, TIMA, FR

- 4.4.1** Data Flow Testing for Virtual Prototypes.....380
17:00 – 17:30 *Muhammad Hassan, Vladimir Herdt, Hoang M. Le, Mingsong Chen, Daniel Große and Rolf Drechsler*

- 4.4.2** MINIME-Validator: Validating Hardware with Synthetic Parallel Testcases.....386
17:30 – 18:00 *Alper Sen, Etem Deniz and Brian Kahne*

- 4.4.3** Cost-Effective Analysis of Post-Silicon Functional Coverage Events.....392
18:00 – 18:30 *Farimah Farahmandi, Ronny Morad, Avi Ziv, Ziv Nevo and Prabhat Mishra*

Session Title	Hot Topic Session: On How to Design and Manage Exascale Computing System Technologies
Session Code / Room	4.5 / 3C
Date / Time	Tuesday, March 28, 2017/ 17:00 – 18:30
Chair	Donatella Sciuto, Politecnico di Milano, IT
Co-Chair	José L. Ayala, Universidad Complutense de Madrid, ES,

- 4.5.1** Towards Exascale Computing with Heterogeneous Architectures.....398
17:00 – 17:30 *Kenneth O'Brien, Lorenzo Di Tucci, Gianluca Durelli and Michaela Blott*

4.5.2 17:30 – 17:45	From exaflop to exaflow.....404 <i>Tobias Becker, Pavel Burovskiy, Anna Maria Nestorov, Hristina Palikareva, Enrico Reggiani and Georgi Gaydadjiev</i>
4.5.3 17:45 – 18:00	Heterogeneous Exascale Supercomputing: The Role of CAD in the exaFPGA Project.....410 <i>M. Rabozzi, G. Natale, E. Del Sozzo, A. Scolari, L. Stornaiuolo and M. D. Santambrogio</i>
4.5.4 18:00 – 18:30	An Open Reconfigurable Research Platform as Stepping Stone to Exascale High-Performance Computing.....416 <i>Dirk Stroobandt, Catalin Bogdan Ciobanu, Marco D. Santambrogio, Gabriël Figueiredo, Andreas Brokalakis, Dionisios Pnevmatikatos, Michael Huebner, Tobias Becker, Alex J. W. Thom</i>

Session Title	Fault modeling, test generation and diagnosis
Session Code / Room	4.6 / 5A
Date / Time	Tuesday, March 28, 2017 / 17:00 – 18:30
Chair	Stephan Eggersgluss, University of Bremen, DE,
Co-Chair	Martin Keim, Mentor, DE,

4.6.1 17:00 – 17:30	Fast and Waveform-Accurate Hazard-Aware SAT-Based TSOE ATPG.....422 <i>Jan Burchard, Dominik Erb, Adit D. Singh, Sudhakar M. Reddy and Bernd Becker</i>
4.6.2 17:30 – 18:00	Fault Diagnosis of Arbiter Physical Unclonable Function.....428 <i>Jing Ye, Qingli Guo, Yu Hu and Xiaowei Li</i>
4.6.3 18:00 – 18:30	FPGA-Based Failure Mode Testing and Analysis for MLC NAND Flash Memory.....434 <i>Meng Zhang, Fei Wu, He Huang, Qian Xia, Jian Zhou and Changsheng Xie</i>

Session Title	Process variation management for today's and tomorrow's computing
Session Code / Room	4.7 /3B
Date / Time	Tuesday, March 28, 2017 / 17:00 – 18:30
Chair	Mohamed Sabry, Stanford University, US,

4.7.1 17:00 – 17:30	Robust Neuromorphic Computing in the Presence of Process Variation.....440 <i>Ali BanaGozar, Mohammad Ali Maleki, Mehdi Kamal, Ali Afzali-Kusha and Massoud Pedram</i>
4.7.2 17:30 – 18:00	An On-Line Framework for Improving Reliability of Real-Time Systems on "Big-Little" Type MPSoCs.....446 <i>Yue Ma, Thidapat Chantem, Robert P. Dick, Shige Wang and X. Sharon Hu</i>
4.7.3 18:00 – 18:30	Application Performance Improvement By Exploiting Process Variability On FPGA Devices.....452 <i>Konstantinos Maragos, George Lentaris, Dimitrios Soudris, Kostas Siozios and Vasilis F. Pavlidis</i>

Session Title	IoT Day: IoT Perspectives
Session Code / Room	5.1 / 5BC
Date / Time	Wednesday, March 29, 2017/ 08:30 – 10:00
Organiser	Marilyn Wolf, <i>Georgia Tech, US,</i> Andreas Herkersdorf, <i>TU Muenchen, DE,</i>
Chair	Marilyn Wolf, <i>Georgia Tech, US</i>
Co-Chair	Andreas Herkersdorf, <i>TU Muenchen, DE</i>

- 5.1.1** Design for Iot.....N/A
8:30 – 9:15 *Lothar Thiele*
- 5.1.2** The internet of Things in the Cognitive ERA.....N/A
9:15–10:00 *Alessandro Curioni*

Session Title	Emerging Computer Paradigms
Session Code / Room	5.2 / 4BC
Date / Time	Wednesday, March 29, 2017 / 08:30 – 10:00
Chair	Jim Harkin, <i>Ulster University, GB,</i>

- 5.2.1** Make It Reversible: Efficient Embedding of Non-reversible Functions.....458
8:30 – 9:00 *Alwin Zulehner and Robert Wille*
- 5.2.2** QX: A High-Performance Quantum Computer Simulation Platform.....464
9:00 – 9:30 *N. Khammassi, I. Ashraf, X. Fu, C.G. Almudever and K. Bertels*
- 5.2.3** Design Automation and Design Space Exploration for Quantum Computers.....470
9:30 – 10:00 *Mathias Soeken, Martin Roetteler, Nathan Wiebe and Giovanni De Micheli*

Session Title	Hot Topic Session: I'm Gonna Make an Approximation IoT Can't Refuse - Approximate Computing for Improving Power Efficiency of IoT and HPC
Session Code / Room	5.3 / 2BC
Date / Time	Wednesday, March 29, 2017 / 08:30 – 10:00
Chair	Christian Enz, <i>EPFL, CH,</i>
Co-Chair	Anca Molnos, <i>CEA Leti, FR,</i>

- 5.3.1** Introduction.....N/A
8:30 – 8:45 *Christian Enz*
- 5.3.2** Pushing the Limits of Voltage Over-Scaling for Error-Resilient Applications.....476
8:45 – 9:00 *Rengarajan Ragavan, Benjamin Barrois, Cedric Killian and Olivier Sentieys*
- 5.3.3** Combining Structural and Timing Errors in Overclocked Inexact Speculative Adders.....482
9:00 – 9:15 *Xun Jiao, Vincent Camus, Mattia Cacciotti, Yu Jiang, Christian Enz and Rajesh K. Gupta*
- 5.3.4** DVAFS: Trading Computational Accuracy for Energy Through Dynamic-Voltage-Accuracy-Frequency-Scaling.....488
9:15 – 9:30 *Bert Moons, Roel Uytterhoeven, Wim Dehaene and Marian Verhelst*

- 5.3.5**
9:30 – 9:45 Exploiting Computation Skip to Reduce Energy Consumption by Approximate Computing, an HEVC Encoder Case Study.....494
Alexandre Mercat, Justine Bonnot, Maxime Pelcat, Wassim Hamidouche and Daniel Menard
- 5.3.6**
9:45 – 10:00 Location Detection for Navigation Using IMUs with a Map Through Coarse-Grained Machine Learning.....500
J. Jose Gonzalez E., Chen Luo, Anshumali Shrivastava, Krishna Palem, Yongshik Moon, Soonhyun Noh, Daedong Park and Seongsoo Hong

Session Title	Solutions for efficient simulation and validation
Session Code / Room	5.4 /3A
Date / Time	Wednesday, March 29, 2017/ 08:30 – 10:00
Chair	Daniel Grosse, University of Bremen, DE,
Co-Chair	Alper Sen, Bogazici University,TR

- 5.4.1**
8:30 – 9:00 Performance Impacts and Limitations of Hardware Memory Access Trace Collection.....506
Nicholas C. Doyle, Eric Matthews, Graham Holland, Alexandra Fedorova and Lesley Shannon
- 5.4.2**
9:00 – 9:30 Context-Sensitive Timing Automata for Fast Source Level Simulation.....512
Sebastian Ottlik, Christoph Gerum, Alexander Viehl, Wolfgang Rosenstiel and Oliver Bringmann
- 5.4.3**
9:30 – 9:45 MARS: A Flexible Real-Time Streaming Platform for Testing Automation Systems.....518
Raphael Eidenbenz, Alexandru Moga, Thanikesavan Sivanthi and Carsten Franke
- 5.4.4**
9:45 – 10:00 SERD: A Simulation Framework for Estimation of System Level Reliability Degradation.....524
Saurav Kumar Ghosh and Soumyajit Dey

Session Title	Hot Topic Session: Spintronics-based Computing
Session Code / Room	5.5 / 3C
Date / Time	Wednesday, March 29, 2017 / 08:30 – 10:00
Chair	Lionel Torres, LIRMM, CNRS/University of Montpellier, FR
Co-Chair	Weisheng Zhao, Beihang University, CN

- 5.5.1**
8:30 – 9:00 Magnetic Tunnel Junction Enabled All-Spin Stochastic Spiking Neural Network.....530
Gopalakrishnan Srinivasan, Abhronil Sengupta and Kaushik Roy
- 5.5.2**
9:00 – 9:15 Embedded Systems to High Performance Computing using STT-MRAM.....536
Sophiane Senni, Thibaud Delobelle, Odilia Coi, Pierre-Yves Peneau, Lionel Torres, Abdoulaye Gamatie, Pascal Benoit and Gilles Sassatelli
- 5.5.3**
9:15 – 9:30 Voltage-Controlled MRAM for Working Memory: Perspectives and Challenges.....542
Wang Kang, Liang Chang, Youguang Zhang and Weisheng Zhao
- 5.5.4**
9:30 – 9:45 Three-Terminal MTJ-Based Nonvolatile Logic Circuits with Self-Terminated Writing Mechanism for Ultra-Low-Power VLSI Processor.....548
Takahiro Hanyu, Daisuke Suzuki, Naoya Onizawa and Masanori Natsui
- 5.5.5**
9:45 – 10:00 Opportunistic Write for Fast and Reliable STT-MRAM.....554
Nour Sayed, Mojtaba Ebrahimi, Rajendra Bishnoi and Mehdi B. Tahoori

Session Title	Reuse and Integration of Test, Debug, and Reliability Infrastructure
Session Code / Room	5.6 / 5A
Date / Time	Wednesday, March 29, 2017 / 08:30 – 10:00
Chair	Paolo Bernardi, PdT, IT,
Co-Chair	Alberto Bosio, LIRMM, FR

- 5.6.1** Fault Clustering Technique for 3D Memory BISR.....560
8:30 – 9:00 *Tianjian Li, Yan Han, Xiaoyao Liang, Hsien-Hsin S. Lee and Li Jiang*
- 5.6.2** Architectural Evaluations on TSV Redundancy for Reliability Enhancement.....566
9:00 – 9:30 *Yen-Hao Chen, Chien-Pang Chiu, Russell Barnes and TingTing Hwang*
- 5.6.3** Reusing Trace Buffers to Enhance Cache Performance.....572
9:30 – 9:45 *Neetu Jindal, Preeti Ranjan Panda and Smruti R. Sarangi*
- 5.6.4** Optimization of Retargeting for IEEE 1149.1 TAP Controllers with Embedded Compression.....578
9:45 – 10:00 *Sebastian Huhn, Stephan Eggersglüß, Krishnendu Chakrabarty and Rolf Drechsler*

Session Title	Schedulability Analysis
Session Code / Room	5.7 /3B
Date / Time	Wednesday, March 29, 2017 / 08:30 – 10:00
Chair	Rodolfo Pellizzoni, University of Waterloo, CA
Co-Chair	Petru Eles, Linköpings universitet,

- 5.7.1** Bounding Deadline Misses in Weakly-Hard Real-Time Systems with Task Dependencies.....584
8:30 – 9:00 *Zain A. H. Hammadeh, Rolf Ernst, Sophie Quinton, Rafik Henia and Laurent Rioux*
- 5.7.2** Real-Time Communication Analysis for Networks-on-Chip with Backpressure.....590
9:00 – 9:30 *Sebastian Tobuschat and Rolf Ernst*
- 5.7.3** Probabilistic Schedulability Analysis for Fixed Priority Mixed Criticality Real-Time Systems.....596
9:30 – 10:00 *Yasmina Abdeddaïm and Dorin Maxim*

Session Title	Interactive Presentations
Session Code / Room	IP2
Date / Time	Wednesday, March 29, 2017 / 10:00 – 10:30

- IP2-1** Compact Modeling and Circuit-Level Simulation of Silicon Nanophotonic Interconnects.....602
Rui Wu, Yuyang Wang, Zeyu Zhang, Chong Zhang, Clint L. Schow, John E. Bowers and Kwang-Ting Cheng
- IP2-2** A True Random Number Generator based on Parallel STT-MTJs.....606
Yuanzhuo Qu, Jie Han, Bruce F. Cockburn, Witold Pedrycz, Yue Zhang and Weisheng Zhao
- IP2-3** Enabling Area Efficient RF ICs through Monolithic 3D Integration.....610
Panagiotis Chaourani, Per-Erik Hellström, Saul Rodriguez, Raul Onet and Ana Rusu
- IP2-4** Reconfigurable Threshold Logic Gates using Optoelectronic Capacitors.....614
Ragh Kuttappa, Lunal Khuon, Bahram Nabet and Baris Taskin

IP2-5	i-BEP: A Non-Redundant and High-Concurrency Memory Persistency Model.....618 <i>Yuanchao Xu, Zeyi Hou, Junfeng Yan, Lu Yang and Hu Wan</i>
IP2-6	SPMS: Strand based Persistent Memory System.....622 <i>Shuo Li, Peng Wang, Nong Xiao, Guangyu Sun and Fang Liu</i>
IP2-7	Architecting High-Speed Command Schedulers for Open-Row Real-Time SDRAM Controllers.....626 <i>Leonardo Ecco and Rolf Ernst</i>
IP2-8	Automatic Equivalence Checking for SystemC-TLM 2.0 Models Against their Formal Specifications.....630 <i>Mehran Goli, Jannis Stoppe and Rolf Drechsler</i>
IP2-9	Head-Mounted Sensors and Wearable Computing for Automatic Tunnel Vision Assessment.....634 <i>Yuchao Ma, Jon Clements, Roby Daquilante and Hassan Ghasemzadeh</i>
IP2-10	RetroDMR: Troubleshooting Non-Deterministic Faults with Retrospective DMR.....638 <i>Ting Wang, Yannan Liu, Qiang Xu, Zhaobo Zhang, Zhiyuan Wang and Xinli Gu</i>
IP2-11	Critical Path -- Oriented 38 Thermal Aware X-Filling for High Un-modeled Defect Coverage.....642 <i>Fotios Vartziotis and Xrysovalantis Kavousianos</i>
IP2-12	A Comprehensive Methodology for Stress Procedures Evaluation and Comparison for Burn-In of Automotive SoC.....646 <i>D. Appello, P. Bernardi, G. Giacomelli, A. Motta, A. Pagani, G. Pollaccia, C. Rabbi, M. Restifo, P. Ruberg, E. Sanchez, C.M. Villa and F. Venini</i>
IP2-13	Energy Efficient Stochastic Computing with Sobol Sequences.....650 <i>Siting Liu and Jie Han</i>
IP2-14	Logic Analysis and Verification of n-input Genetic Logic Circuits.....654 <i>Hasan Baig and Jan Madsen</i>
IP2-15	A Novel Way to Efficiently Simulate Complex Full Systems Incorporating Hardware Accelerators.....658 <i>Tampouratzis Nikolaos, Konstantinos Georgopoulos and Yannis Papaefstathiou</i>
IP2-16	Automatic Abstraction of Multi-Discipline Analog Models for Efficient Functional Simulation.....662 <i>Enrico Fraccaroli, Michele Lora and Franco Fummi</i>
IP2-17	Novel Magnetic Burn-In for Retention Testing of STTRAM.....666 <i>Mohammad Nasim Imtiaz Khan, Anirudh S. Iyengar and Swaroop Ghosh</i>
IP2-19	Automatic Construction of Models for Analytic System-Level Design Space Exploration Problems.....670 <i>Seyed-Hosein Attarzadeh-Niaki and Ingo Sander</i>

Session Title	IoT Day Hot Topic Session: IoT Enabling Technologies
Session Code / Room	6.1 / 5BC
Date / Time	Wednesday, March 29, 2017 / 11:00 – 12:30
Chair	Andreas Herkersdorf, , TU Muenchen, DE,

6.1.1 11:00 – 11:30	Ultra-Low-Power Circuits For IOT Applications.....N/A <i>Georges Gielen</i>
6.1.2 11:30 – 12:00	Structural Health Monitoring for Smart Cities: A HW/SW Codesign Perspective.....N/A <i>GJiang Xu</i>
6.1.3 12:00 – 12:30	Security in the Internet of Things: A Challenge of Scale.....674 <i>Patrick Schaumont</i>

Session Title	Security Primitives
Session Code / Room	6.3 / 2BC
Date / Time	Wednesday, March 29, 2017 / 11:00 – 12:30
Chair	Berndt Gammel, Infineon, DE
Co-Chair	Tim Güneysu, University of Bremen & DFKI, DE,

- 6.3.1**
11:00 – 11:30 Sensitized Path PUF: A Lightweight Embedded Physical Unclonable Function.....680
Matthias Sauer, Pascal Raiola, Linus Feiten, Bernd Becker, Ulrich Rührmair and Ilia Polian
- 6.3.2**
11:30 – 12:00 Temperature Aware Phase/Frequency Detector-Based RO-PUFs Exploiting Bulk-Controlled Oscillators.....686
Sha Tao and Elena Dubrova
- 6.3.3**
12:00 – 12:15 ChaCha20-Poly1305 Authenticated Encryption for High-Speed Embedded IoT Applications.....692
Fabrizio De Santis, Andreas Schauer and Georg Sigl,
- 6.3.4**
12:15 – 12:30 Towards Post-quantum Security for IoT Endpoints with NTRU.....698
Oscar M. Guillen, Thomas Pöppelmann, Jose M. Bermudo Mera, Elena Fuentes Bongenaar, Georg Sigl and Johanna Sepulveda

Session Title	High-performance Reconfigurable Computing
Session Code / Room	6.4 / 3A
Date / Time	Wednesday, March 29, 2017 / 11:00 – 12:30
Chair	Philip Brisk, University of California, Riverside, US,
Co-Chair	Mirjana Stojilovic, EPFL, CH

- 6.4.1**
11:00 – 11:30 Automating the Pipeline of Arithmetic Datapaths.....704
Matei Istoan and Florent de Dinechin
- 6.4.2**
11:30 – 12:00 Operand Size Reconfiguration for Big Data Processing in Memory.....710
Paulo C. Santos, Geraldo F. Oliveira, Diego G. Tomé, Marco A. Z. Alves, Eduardo C. Almeida and Luigi Carro
- 6.4.3**
12:00 – 12:30 Architectural Optimizations for High Performance and Energy Efficient Smith-Waterman Implementation on FPGAs using OpenCL.....716
Lorenzo Di Tucci, Kenneth O'Brien, Michaela Blott and Marco D. Santambrogio

Session Title	Hot Topic Session: Memristor for High Performance Computing: Myth or Reality?
Session Code / Room	6.5 / 3C
Date / Time	Wednesday, March 29, 2017 / 11:00 – 12:30
Chair	Henk Corporaal, Eindhoven University of Technology, NL,
Co-Chair	Koen Bertels, Delft University of Technology, NL,

- 6.5.1**
11:00 – 11:30 Memory-Intensive Architectures.....N/A
Shahar Kvatinsky
- 6.5.2**
11:30 – 12:00 Memristor For Computing: Myth or Reality?.....722
Said Hamdioui

6.5.3 Nanoscale Neuromorphic Silicon Learning Machines.....N/A
12:00 – 12:30 *Gert Cauwenberghs*

Session Title	Industrial Experiences & EU Projects
Session Code / Room	6.6 /5A
Date / Time	Wednesday, March 29, 2017 / 11:00 – 12:30
Chair	Mario Diaz Nava, ST Microelectronics, FR
Co-Chair	Eugenio Villar, University of Cantabria, ES

6.6.1 An Asynchronous NoC Router in a 14nm FinFET Library: Comparison to an Industrial
11:00 – 11:15 Synchronous Counterpart.....732
Weiwei Jiang, Davide Bertozzi, Gabriele Miorandi, Steven M. Nowick, Wayne Burleson and Greg Sadowski

6.6.2 An Advanced Embedded Architecture for Connected Component Analysis in Industrial
11:15 – 11:30 Applications.....734
Menbere Tekleyohannes, Mohammadsadegh Sadri, Christian Weis, Norbert Wehn, Martin Klein and Michael Siegrist

6.6.3 Workload Dependent Reliability Timing Analysis Flow.....736
11:30 – 11:45 *Ajith Sivadasan, Armelle Notin, Vincent Huard, Etienne Maurin, Souhir Mhira, Florian Cacho and Lorena Anghel*

6.6.4 Probabilistic Timing Analysis on Time-Randomized Platforms for the Space Domain.....738
11:45 – 12:00 *Mikel Fernandez, David Morales, Leonidas Kosmidis, Alen Bardizbanyan, Ian Broster, Carles Hernandez, Eduardo Quinones, Jaume Abella, Francisco Cazorla, Paulo Machado and Luca Fossati*

6.6.5 Cross-Layer Design of Reconfigurable Cyber-Physical Systems.....740
12:00 – 12:15 *M. Masin, F. Palumbo, H. Myrhaug, J. A. de Oliveira Filho, M. Pastena, M. Pelcat, L. Raffo, F. Regazzoni, A. A. Sanchez, A. Toffetti, E. de la Torre, K. Zedda*

6.6.6 INSPEX: Design and Integration of a Portable/Wearable Smart Spatial Exploration
12:15 – 12:30 System.....746
S. Lesecq, Julie Foucault, M. Correvo, P. Heck, J. Barrett, S. Rea, F. Birot, H. de Chaumont, R. Banach, J.-M. Van Gyseghe, C. Jackson, A. di Matteo, V. Di Palma, C. Ó'Murchú and A. Mathewson

Session Title	Model-Based Design and Verification of Real-Time Systems
Session Code / Room	6.7 /3B
Date / Time	Wednesday, March 29, 2017 / 11:00 – 12:30
Chair	Alain Girault, INRIA, FR,
Co-Chair	Amir Aminifar, IPFL Lausanne, CH,

6.7.1 Near-Optimal Deployment of Dataflow Applications on Many-Core Platforms with
11:00 – 11:30 Real-Time Guarantees.....752
Stefanos Skalistis and Alena Simalatsar

6.7.2 Simulating Preemptive Scheduling with Timing-aware Blocks in Simulink.....758
11:30 – 12:00 *ndreas Naderlinger*

6.7.3 Online Workload Monitoring with the Feedback of Actual Execution Time for Real-
12:00 – 12:30 Time Systems.....764
Biao Hu, Kai Huang, Gang Chen, Long Cheng and Alois Knoll

Session	LUNCH TIME KEYNOTE SESSION
Session Code / Room	7.0
Date / Time	Wednesday, March 29, 2017 / 13:50 - 14:20
Chair	David Atienza, EPFL, CH,

7.0.1 Internet Of Everything Is Our Opportunity.....xxxvii
13:50 – 14:20 *Keith Willett*

Session Title	IoT Day Hot Topic Session: IoT Deployment
Session Code / Room	7.1 / 5BC
Date / Time	Wednesday, March 29, 2017 / 14:30 – 16:00
Chair	Marilyn Wolf, Georgia Tech, US

7.1.1 Designing and Launching Great IOT Products.....N/A
14:30 – 15:00 *Adrian Caceres*

7.1.2 How ASIC Development Will Change for Future IOT MEMS Sensors.....N/A
15:00 – 15:30 *Dirk Droste*

7.1.3 Distributed Wayside Architecture - IOT for Railway Infrastructure.....N/A
15:30 – 16:00 *Olivier Kaiser*

7.1.4 A Low-Power IOT Processor Integrating Voltage-Scalable Fully Digital Memories.....N/A
16:00 – 16:01 *Olivier Kaise*

7.1.5 A Simple, Stateless, Cost Effective Symmetric Encryption Strategy for Energy-Harvesting IOT Devices.....N/A
16:01 – 16:02 *Jan Madsen*

7.1.6 Reconfigurable Microcontroller For End Nodes in Internet of Things.....N/A
16:02 – 16:03 *Wai-Chung Matthew Tang*

7.1.7 FURTHER SIMPLIFICATION OF APPROXIMATE ADDERS USING INPUT DATA RANGES IN IOT.....N/A
16:03 – 16:20 *Jeong-A Lee*

Session Title	In-memory Computing and Security for Non-volatile Memory Technologies
Session Code / Room	7.2 / 4BC
Date / Time	Wednesday, March 29, 2017 / 14:30 – 16:00
Chair	Bastien Giraud, CEA-Leti, FR
Co-Chair	Pierre-Emmanuel Gaillardon, University of Utah, US,

7.2.1 Automated Synthesis of Compact Crossbars for Sneak-Path Based In-Memory Computing.....770
14:30 – 15:00 *Dwaipayan Chakraborty and Sumit Kumar Jha*

7.2.2 Hybrid Spiking-based Multi-layered Self-learning Neuromorphic System Based On Memristor Crossbar Arrays.....776
15:00 – 15:30 *Amr M. Hassan, Chaofei Yang, Chenchen Liu, Hai (Helen) Li and Yiran Chen*

7.2.3 ReVAMP : ReRAM based VLIW Architecture for in-Memory computing.....782
15:30 – 16:00 *Debjyoti Bhattacharjee, Rajeswari Devadoss and Anupam Chattopadhyay*

Session Title	Optimizing performance, energy and predictability via hardware/software codesign
Session Code / Room	7.3 / 2BC
Date / Time	Wednesday, March 29, 2017 / 14:30 – 16:00
Chair	Sasan Avesta, <i>George Mason University, US,</i>
Co-Chair	Ramon Canal, <i>UPC, ES</i>

- 7.3.1**
14:30 – 15:00 Accurate Private/Shared Classification of Memory Accesses: A Run-time Analysis System for the LEON3 Multi-core Processor.....788
Nam Ho, Ishraq Ibne Ashraf, Paul Kaufmann and Marco Platzner
- 7.3.2**
15:00 – 15:30 Design of a Low Power, Relative Timing Based Asynchronous MSP430 Microprocessor.....794
Dipanjan Bhadra and Kenneth S. Stevens
- 7.3.3**
15:30 – 15:45 A Coordinated Multi-Agent Reinforcement Learning Approach to Multi-Level Cache Co-partitioning.....800
Rahul Jain, Preeti Ranjan Panda and Sreenivas Subramoney
- 7.3.4**
15:45 – 16:00 GPIOCP: Timing-Accurate General Purpose I/O Controller for Many-core Real-time Systems.....806
Zhe Jiang and Neil C. Audsley

Session Title	Advances in Logic Synthesis
Session Code / Room	7.4 / 3A
Date / Time	Wednesday, March 29, 2017 / 14:30 – 16:00
Chair	Paolo Ienne, <i>EPFL, CH</i>
Co-Chair	Tsutomu Sasao, <i>Meiji University, JP,</i>

- 7.4.1**
14:30 – 15:00 An Algorithm to Find Optimum Support-Reducing Decompositions for Index Generation Functions.....812
Tsutomu Sasao, Kyu Matsuura and Yukihiro Iguchi
- 7.4.2**
15:00 – 15:30 Taking One-to-one Mappings for Granted: Advanced Logic Design of Encoder Circuits.....818
Alwin Zulehner and Robert Wille
- 7.4.3**
15:30 – 15:45 Analysis of Short-Circuit Conditions in Logic Circuits.....824
João Afonso and José Monteiro
- 7.4.4**
15:45 – 16:00 Busy Man's Synthesis: Combinational Delay Optimization With SAT.....830
Mathias Soeken, Giovanni De Micheli and Alan Mishchenko

Session Title	Hot Topic Session: The Engineering Challenges for Quantum Computing
Session Code / Room	7.5 /3C
Date / Time	Wednesday, March 29, 2017 / 14:30 – 16:00
Chair	Edoardo Charbon, <i>Delft University of Technology, NL</i>
Co-Chair	Said Hamdioui, <i>Delft University of Technology, NL,</i>

- 7.5.1**
14:30 – 15:00 What is Quantum Computing All About?.....N/A
Carmen G. Almudever and Koen Bertels
- 7.5.2**
15:00 – 15:30 Further Simplification of Approximate Adders Using Input Data Ranges in IOT.....N/A
Jeong-A Lee

7.5.3 Control Electronics for Quantum Computer.....N/A
15:30 – 16:00 *Hendrik Bluhm*

Session Title	Memory Reliability: Modeling and Mitigation
Session Code / Room	7.6 /5A
Date / Time	Wednesday, March 29, 2017 / 14:30 – 16:00
Chair	Jose Pineda De Gyvez, NXP, NL,
Co-Chair	Vikas Chandra, ARM, US,

7.6.1 MVP ECC : Manufacturing Process Variation Aware Unequal Protection ECC for
14:30 – 15:00 Memory Reliability.....846
Seungyeob Lee and Joon-Sung Yang

7.6.2 Analyzing the Effects of Peripheral Circuit Aging of Embedded SRAM Architectures.....852
15:00 – 15:30 *Josef Kinseher, Leonhard Heiß and Ilia Polian*

7.6.3 Mitigation of Sense Amplifier Degradation Using Input Switching.....858
15:30 – 16:00 *Daniël Kraak, Innocent Agbo, Mottaqiallah Taouil, Said Hamdioui, Pieter Weckx, Stefan Cosemans, Francky Catthoor and Wim Dehaene*

Session Title	Resource management and analysis for embedded architectures
Session Code / Room	7.7 / 3B
Date / Time	Wednesday, March 29, 2017 / 14:30 – 16:00
Chair	Akash Kumar, Technische Universitaet Dresden, DE,
Co-Chair	Orlando Moreira, Intel, NL

7.7.1 Scalable Probabilistic Power Budgeting for Many-Cores.....864
14:30 – 15:00 *Anuj Pathania, Heba Khdr, Muhammad Shafique, Tulika Mitra and Jörg Henkel*

7.7.2 Exploiting Sporadic Servers to provide Budget Scheduling for ARINC653 based Real-
15:00 – 15:30 Time Virtualization Environments.....870
Matthias Beckert, Kai Björn Gemlau and Rolf Ernst

7.7.3 Programming and Analysing Scenario-Aware Dataflow on a Multi-Processor Platform.....876
15:30 – 16:00 *Reinier van Kampenhout, Sander Stuijk and Kees Goossens*

Session Title	Interactive Presentations
Session Code / Room	IP3
Date / Time	Wednesday, March 29, 2017 / 16:00 – 16:30

IP3-1 Leveraging Aging Effect to Improve SRAM-based True Random Number Generators.....882
Saman Kiamehr, Mohammad Saber Golanbari and Mehdi B. Tahoori

IP3-2 Design Automation for Obfuscated Circuits with Multiple Viable Functions.....886
Shahrzad Keshavarz, Christof Paar and Daniel Holcomb

IP3-3 Double MAC: Doubling the Performance of Convolutional Neural Networks on Modern
 FPGAs.....890
Dong Nguyen, Daewoo Kim and Jongeun Lee

IP3-4 BITMAN: A Tool and API for FPGA Bitstream Manipulations.....894
Khoa Dang Pham, Edson Horta and Dirk Koch

IP3-5	A Generic Topology Selection Method for Analog Circuits with Embedded Circuit Sizing Demonstrated on the OTA Example.....898 <i>Andreas Gerlach, Juergen Scheible, Thoralf Rosahl and Frank-Thomas Eitrich</i>
IP3-6	Latency Analysis of Homogeneous Synchronous Dataflow Graphs Using Timed Automata.....902 <i>Guus Kuiper and Marco J.G. Bekooij</i>
IP3-7	COVERT: Counter Overflow Reduction for Efficient Encryption of NonVolatile Memories.....906 <i>Shivam Swami and Kartik Mohanram</i>
IP3-8	A Wear-Leveling-Aware Counter Mode for Data Encryption in Non-Volatile Memories.....910 <i>Fangting Huang, Dan Feng, Yu Hua and Wen Zhou</i>
IP3-9	Tunnel FET Based Refresh-Free-DRAM.....914 <i>Navneet Gupta, Adam Makosiej, Andrei Vladimirescu, Amara Amara and Costin Anghel</i>
IP3-10	A Hardware Implementation of the MCAS Synchronization Primitive.....918 <i>Srishty Patel, Rajshekar Kalayappan, Ishani Mahajan and Smruti R. Sarangi</i>
IP3-11	BandiTS: Dynamic Timing Speculation Using Multi-Armed Bandit Based Optimization.....922 <i>Jeff (Jun) Zhang and Siddharth Garg</i>
IP3-12	Design and Implementation of a Fair Credit-Based Bandwidth Sharing Scheme for Buses.....926 <i>Mladen Slijepcevic, Carles Hernandez, Jaume Abella and Francisco J. Cazorla</i>
IP3-13	Technology Mapping with All Spin Logic.....930 <i>Boyu Zhang and Azadeh Davoodi</i>
IP3-14	A New Method to Identify Threshold Logic Functions.....934 <i>Seyed Nima Mozaffari, Spyros Tragoudas and Themistoklis Haniotakis</i>
IP3-15	A Bridging Fault Model for Line Coverage in the Presence of Undetected Transition Faults.....938 <i>Irith Pomeranz</i>
IP3-16	CHRT: A Criticality- and Heterogeneity-Aware Runtime System for Task-Parallel Applications.....942 <i>Myeonggyun Han, Jinsu Park and Woongki Baek</i>
IP3-17	MobiXen: Porting Xen on Android Devices for Mobile Virtualization.....946 <i>Yaozu Dong, Jianguo Yao, Haibing Guan, Ananth Krishna and Yunhong Jiang</i>
IP3-18	Optimisation Opportunities and Evaluation for GPGPU applications on Low-End Mobile GPUs.....950 <i>Matina Maria Trompouki and Leonidas Kosmidis</i>

Session Title	IoT Day Hot Topic Session: Challenges and Potentials for IoT Rollout
Session Code / Room	8.1 / 5BC
Date / Time	Wednesday, March 29, 2017 / 17:00 – 18:30
Chair	Andreas Herkersdorf, TU Muenchen, DE,
8.1.1 17:00 – 17:30	Ultra-Low Power and Dependability for IoT Devices.....954 <i>Jörg Henkel, Santiago Pagani, Hussam Amrouch, Lars Bauer and Farzad Samie</i>
8.1.2 17:30 – 18:00	Smarter Spaces Through Local(IZED) Object Interactions.....N/A <i>Jean-Marie Bonnin and Frédéric Weis</i>
8.1.3 18:00 – 18:30	Deploying IOT for Instrumentation and Analysis of Manufacturing Systems.....N/A <i>Mohammad Al Faruque</i>

Session Title	Hot Topic Session: No Power? No Problem! Exploiting Non-Volatility in Energy Constrained Environments
Session Code / Room	8.2 / 4BC
Date / Time	Wednesday, March 29, 2017 / 17:00 – 18:30
Chair	Michael Niemier, University of Notre Dame, US

- 8.2.1**
17:00 – 17:30 Energy-Driven Computing: Rethinking the Design of Energy Harvesting Systems.....960
Geoff V. Merrett and Bashir M. Al-Hashimi
- 8.2.2**
17:30 – 18:00 Nonvolatile Processors: Why Is It Trending?.....966
Fang Su, Kaisheng Ma, Xueqing Li, Tongda Wu, Yongpan Liu and Vijaykrishnan Narayanan
- 8.2.3**
18:00 – 18:30 Advanced Spintronic Memory and Logic For Non-Volatile Processors.....972
Robert Perricone, Ibrahim Ahmed, Zhaoxin Liang, Meghna G. Mankalale, X. Sharon Hu, Chris H. Kim, Michael Niemier, Sachin S. Sapatnekar and Jian-Ping Wang

Session Title	Secure Processor Components
Session Code / Room	8.3 / 2BC
Date / Time	Wednesday, March 29, 2017/ 17:00 – 18:30
Chair	Patrick Schaumont, Virginia Tech, US,
Co-Chair	José L. Ayala, Complutense University of Madrid, ES

- 8.3.1**
17:00 – 17:30 Automatic Generation of Formally-Proven Tamper-Resistant Galois-Field Multipliers Based on Generalized Masking Scheme.....978
Rei Ueno, Naofumi Homma, Sumio Morioka and Takafumi Aoki
- 8.3.2**
17:30 – 18:00 SCAM: Secured Content Addressable Memory Based on Homomorphic Encryption.....984
Song Bian, Masayuki Hiromoto and Takashi Sato
- 8.3.3**
18:00 – 18:30 SPARX - A Side-Channel Protected Processor for ARX-based Cryptography.....990
Florian Bache, Tobias Schneider, Amir Moradi and Tim Güneysu

Session Title	Advanced systems for healthcare and assistive technologies
Session Code / Room	8.4 / 3A
Date / Time	Wednesday, March 29, 2017 / 17:00 – 18:30
Chair	Ruben Braojos, EPFL, CH
Co-Chair	Luca Fanucci, University of Pisa, IT,

- 8.4.1**
17:00 – 17:30 Adaptive Compressed Sensing at the Fingertip of Internet-of-Things Sensors: An Ultra-Low Power Activity Recognition.....996
Ramin Fallahzadeh, Josue Pagan Ortiz and Hassan Ghasemzadeh
- 8.4.2**
17:30 – 18:00 A Zynq-Based Dynamically Reconfigurable High Density Myoelectric Prosthesis Controller.....1002
Alexander Boschmann, Georg Thombansen, Linus Witschen, Alex Wiens and Marco Platzner
- 8.4.3**
18:00 – 18:15 Microwatt End-to-End Digital Neural Signal Processing Systems for Motor Intention Decoding.....1008
Zhewei Jiang, Chisung Bae, Joonseong Kang, Sang Joon Kim and Mingoo Seok

8.4.4 An Embedded System Remotely Driving Mechanical Devices by P300 Brain Activity.....1014
18:15 – 18:30 *D. De Venuto, V. F. Annese and G. Mezzina*

Session Title	Learning and Resilience Techniques for Green Computing
Session Code / Room	8.5 / 3C
Date / Time	Wednesday, March 29, 2017/ 17:00 – 18:30
Chair	Muhammed Shafique , <i>Vienna University of Technology (TU-Wien), AT,</i>
Co-Chair	Andreas Burg , <i>EPFL, CH</i>

8.5.1 Revamping Timing Error Resilience to Tackle Choke Points at NTC Systems.....1020
17:00 – 17:30 *Aatreyi Bal, Shamik Saha, Sanghamitra Roy and Koushik Chakraborty*

8.5.2 Efficient Neural Network Acceleration on GPGPU using Content Addressable Memory.....1026
17:30 – 18:00 *Mohsen Imani, Daniel Peroni, Yeseong Kim, Abbas Rahimi and Tajana Rosing*

8.5.3 Chain-NN: An Energy-Efficient 1D Chain Architecture for Accelerating Deep
18:00 – 18:15 Convolutional Neural Networks.....1032
Shihao Wang, Dajiang Zhou, Xushen Han and Takeshi Yoshimura

8.5.4 Continuous Learning of HPC Infrastructure Models using Big Data Analytics and In-
18:15 – 18:30 Memory processing Tools.....1038
Francesco Beneventi, Andrea Bartolini, Carlo Cavazzoni and Luca Benini,

Session Title	Hot Topic Session: Self-aware Systems: Concepts and Applications
Session Code / Room	8.6 / 5A
Date / Time	Wednesday, March 29, 2017 / 17:00 – 18:30
Chair	Nikil Dutt , <i>UC Irvine, US</i>
Co-Chair	Amir Rahmani , <i>TU Wien, AT</i>

8.6.1 Self-Aware Computing Systems: From Psychology to Engineering.....1044
17:00 – 17:30 *Peter R. Lewis*

8.6.2 Self-Awareness in Autonomous Automotive Systems.....1050
17:30 – 18:00 *Johannes Schlatow, Mischa Möstl, Rolf Ernst, Marcus Nolte, Inga Jatzkowski, Markus Maurer, Christian Herber and Andreas Herkersdorf*

8.6.3 Self-Awareness in Remote Health Monitoring Systems using Wearable Electronics.....1056
18:00 – 18:30 *Arman Anzanpour, Iman Azimi, Maximilian Götzinger, Amir M. Rahmani, Nima TaheriNejad, Pasi Liljeberg, Axel Jantsch and Nikil Dutt*

Session Title	Instruction-level and thread-level parallelism in embedded systems
Session Code / Room	8.7 / 3B
Date / Time	Wednesday, March 29, 2017 / 17:00 – 18:30
Chair	Oliver Bringmann , <i>Universität Tübingen, DE</i>
co-Chair	Jürgen Teich , <i>Friedrich-Alexander-Universität Erlangen-Nürnberg, DE,</i>

8.7.1 Hardware-Accelerated Dynamic Binary Translation.....1062
17:00 – 17:30 *Simon Rokicki, Erven Rohou and Steven Derrien*

8.7.2 Superword Level Parallelism aware Word Length Optimization.....1068
17:30 – 18:00 *Ali Hassan El Moussawi and Steven Derrien*

8.7.3
18:00 – 18:30 Schedulability-Aware SPM Allocation for Preemptive Hard Real-Time Systems with Arbitrary Activation Patterns.....1074
Arno Luppold and Heiko Falk

Session Title	Wearable and Smart Medical Devices Day: New tools and devices for chronic and acute care
Session Code / Room	9.1 / 5BC
Date / Time	Thursday, March 30, 2017 / 08:30 – 10:00
Chair	José L. Ayala, <i>Universidad Complutense de Madrid, ES,</i>
Co-Chair	Chris Van Hoof, <i>IMEC, BE</i>

9.1.1
8:30 – 9:00 Wearable Robotics in Clinical Practice: Prospects.....N/A
José Luis Pons

9.1.2
9:00 – 9:30 Overcoming Hearing Loss Through New Implant Technologies.....N/A
Carl Van Himbeeck

9.1.3
9:30 – 10:00 Circuits and Systems as Enablers for Novel Healthcare Paradigms.....N/A
Mario Konijnenburg

Session Title	Emerging Schemes for Memory Management
Session Code / Room	9.2 / 4BC
Date / Time	Thursday, March 30, 2017/ 08:30 – 10:00
Chair	Arne Heittman, <i>RWTH, DE</i>
Co-Chair	Costin Anghel, <i>ISEP, FR</i>

9.2.1
8:30 – 9:00 A Log-aware Synergized Scheme for Page-Level FTL Design.....1080
Chu Li, Dan Feng, Yu Hua, Fang Wang, Chuntao Jiang and Wei Zhou

9.2.2
9:00 – 9:30 MALRU: Miss-Penalty Aware LRU-based Cache Replacement for Hybrid Memory Systems.....1086
Di Chen, Hai Jin, Xiaofei Liao, Haikun Liu, Rentong Guo and Dong Liu

9.2.3
9:30 – 9:45 Endurance Management for Resistive Logic-In-Memory Computing Architectures.....1092
Saeideh Shirinzadeh, Mathias Soeken, Pierre-Emmanuel Gaillardon, Giovanni De Micheli and Rolf Drechsler

9.2.4
9:45 – 10:00 Live Together or Die Alone: Block Cooperation to Extend Lifetime of Resistive Memories.....1098
Mohammad Khavari Tavana, Amir Kavyan Ziabari and David Kaeli

Session Title	Hot Topic Session: Security in Cyber-Physical Systems: Attacks All The Way
Session Code / Room	9.3 /2BC
Date / Time	Thursday, March 30, 2017 / 08:30 – 10:00
Chair	Muhammad Shafique, <i>CARE-Tech, TU Wien, AT</i>

9.3.1
8:30 – 8:45 Secure Cyber-Physical Systems: Current Trends, Tools and Open Research Problems.....1104
Anupam Chattopadhyay, Alok Prakash and Muhammad Shafique

9.3.2
8:45 – 9:00 Don't Fall into a Trap: Physical Side-Channel Analysis of ChaCha20-Poly1305.....1110
Bernhard Jungk and Shivam Bhasin

9.3.3
9:00 – 9:15 The RowHammer Problem and Other Issues We May Face as Memory Becomes Denser.....1116
Onur Mutlu

9.3.4	Compromising FPGA SoCs using Malicious Hardware Blocks.....1122
9:15 – 9:30	<i>Nisha Jacob, Carsten Rolfes, Andreas Zankl, Johann Heyszl and Georg Sigl,</i>
9.3.5	Inspiring Trust in Outsourced Integrated Circuit Fabrication.....1128
9:30 – 9:45	<i>Siddharth Garg</i>
9.3.6	Analyzing Security Breaches of Countermeasures Throughout the Refinement Process in
9:45 – 10:00	Hardware Design Flow.....1129
	<i>Jean-Luc Danger, Sylvain Guilley, Philippe Nguyen, Robert Nguyen and Youssef Souissi</i>

Session Title	Design Space Exploration
Session Code / Room	9.4 /3A
Date / Time	Thursday, March 30, 2017/ 08:30 – 10:00
Chair	Lars Bauer, KIT Karlsruhe,
Co-Chair	Alberto Del Barrio, Universidad Computense de Madrid, ES,

9.4.1	Automatic Operating Point Distillation for Hybrid Mapping Methodologies.....1135
8:30 – 9:00	<i>Behnaz Pourmohseni, Michael Glaß, Jürgen Teich</i>
9.4.2	Design Space Exploration of FPGA-Based Accelerators with Multi-Level Parallelism.....1141
9:00 – 9:30	<i>Guanwen Zhong, Alok Prakash, Siqi Wang, Yun Liang, Tulika Mitra and Smail Niar</i>
9.4.3	Design Space Exploration of FPGA Accelerators for Convolutional Neural Networks.....1147
9:30 – 9:45	<i>Atul Rahman, Sangyun Oh, Jongeun Lee and Kiyoung Choi</i>
9.4.4	A Slack-based Approach to Efficiently Deploy Radix 8 Booth Multipliers.....1153
9:45 – 10:00	<i>Alberto A. Del Barrio and Román Hermida</i>

Session Title	Modeling and optimization of Internet-of-things (IoT) devices
Session Code / Room	9.5 / 3C
Date / Time	Thursday, March 30, 2017 / 08:30 – 10:00
Chair	William Fornaciari, Politecnico di Milano, IT,
Co-Chair	Shusuke Yoshimoto, Osaka University, JP

9.5.1	Measurement and Validation of Energy Harvesting IoT Devices.....1159
8:30 – 9:00	<i>Lukas Sigrist, Andres Gomez, Roman Lim, Stefan Lippuner, Matthias Leubin and Lothar Thiele</i>
9.5.2	A Methodology for the Design of Dynamic Accuracy Operators by Runtime Back Bias.....1165
9:00 – 9:30	<i>Daniele Jahier Pagliari, Yves Durand, David Coriat, Anca Molnos, Edith Beigne, Enrico Macii and Massimo Poncino</i>
9.5.3	A Scan-Chain Based State Retention Methodology for IoT Processors Operating on
9:30 – 9:45	Intermittent Energy.....1171
	<i>Pascal Alexander Hager, Hamed Fatemi, Jose Pineda de Gyvez and Luca Benini</i>
9.5.4	A Circuit-Equivalent Battery Model Accounting for the Dependency on Load Frequency.....1177
9:45 – 10:00	<i>Yukai Chen, Enrico Macii and Massimo Poncino</i>

Session Title	Reliability and Optimization Techniques for Analog Circuits
Session Code / Room	9.6 /5A
Date / Time	Thursday, March 30, 2017 / 08:30 – 10:00
Chair	Manuel Barragan, TIMA, FR
Co-Chair	Said Hamdioui, TU Delft, NL

- 9.6.1**
8:30 – 9:00 SLoT: A Supervised Learning Model to Predict Dynamic Timing Errors of Functional Units.....1183
Xun Jiao, Yu Jiang, Abbas Rahimi and Rajesh K. Gupta
- 9.6.2**
9:00 – 9:15 Exploiting Data-Dependence and Flip-Flop Asymmetry for Zero-Overhead System Soft Error Mitigation.....1189
Liangzhen Lai and Vikas Chandra
- 9.6.3**
9:15 – 9:30 Subgradient Based Multiple-Starting-Point Algorithm for Non-Smooth Optimization of Analog Circuits.....1195
Wenlong Lv, Fan Yang, Changhao Yan, Dian Zhou and Xuan Zeng
- 9.6.4**
9:30 – 10:00 Efficient Yield Optimization Method using a Variable K-Means Algorithm for Analog IC Sizing.....1201
Antônio Canelas, Ricardo Martins, Ricardo Póvoa, Nuno Lourenço and Nuno Horta

Session Title	Front-row seats for Temperature and Variability
Session Code / Room	9.7 / 3B
Date / Time	Thursday, March 30, 2017 / 08:30 – 10:00
Chair	Marina Zapater Sancho, EPFL, CH,
Co-Chair	Giovanni Ansaloni,

- 9.7.1**
8:30 – 9:00 An Efficient Leakage-Aware Thermal Simulation Approach for 3D-ICs Using Corrected Linearized Model and Algebraic Multigrid.....1207
Chao Yan, Hengliang Zhu, Dian Zhou and Xuan Zeng
- 9.7.2**
9:00 – 9:30 A Thermally-Aware Energy Minimization Methodology for Global Interconnects.....1213
Soheil Nazar Shahsavani, Alireza Shafaei, Shahin Nazarian and Massoud Pedram
- 9.7.3**
9:30 – 10:00 Analysis and Optimization of Variable-Latency Designs in the Presence of Timing Variability.....1219
Chang-Lin Tsai, Chao-Wei Cheng, Ning-Chi Huang and Kai-Chiang Wu

Session Title	Interactive Presentations
Session Code / Room	IP4
Date / Time	Thursday, 30 March 2017 / 10:00 – 10:30

- IP4-1** 1024-Channel 3D Ultrasound Digital Beamformer in a Single 5W FPGA.....1225
F. Angiolini, A. Ibrahim, W. Simon, A. C. Yüzügüler, M. Arditi, J.-P. Thiran and G. De Micheli
- IP4-2** LAANT: A Library to Automatically Optimize EDP for OpenMP Applications.....1229
Arthur Francisco Lorenzon, Jeckson Dellagostin Souza and Antonio Carlos Schneider Beck
- IP4-3** Improving the Accuracy of the Leakage Power Estimation of Embedded CPUs.....1233
Ting-Wu Chin, Shiao-Li Tsao, Kuo-Wei Hung and Pei-Shu Huang

IP4-4	Schedule-Aware Loop Parallelization for Embedded MPSoCs by Exploiting Parallel Slack.....1237 <i>Miguel Angel Aguilar, Rainer Leupers, Gerd Ascheid, Nikolaos Kavvadias and Liam Fitzpatrick</i>
IP4-5	Reducing Code Management Overhead in Software-Managed Multicores.....1241 <i>Jian Cai, Yooseong Kim, Youngbin Kim, Aviral Shrivastava and Kyoungwoo Lee</i>
IP4-6	Performance Evaluation and Optimization of HBM-Enabled GPU for Data-intensive Applications.....1245 <i>Maohua Zhu, Youwei Zhuo, Chao Wang, Wenguang Chen and Yuan Xie</i>
IP4-7	DAC: Dedup-Assisted Compression Scheme for Improving Lifetime of NAND Storage Systems.....1249 <i>Jisung Park, Sungjin Lee and Jihong Kim</i>
IP4-8	Lifetime Adaptive ECC in NAND Flash Page Management.....1253 <i>Shunzhuo Wang, Fei Wu, Zhonghai Lu, You Zhou, Qin Xiong, Meng Zhang and Changsheng Xie</i>
IP4-9	3D-DPE:A3D High-Bandwidth Dot-Product Engine for High-Performance Neuromorphic Computing.....1257 <i>Miguel Angel Lastras-Montaña, Bhaswar Chakrabarti, Dmitri B. Strukov and Kwang-Ting Cheng</i>
IP4-10	A Schedulability Test for Software Migration on Multicore Systems.....1261 <i>Jung-Eun Kim, Richard Bradford, Tarek Abdelzaher and Lui Sha</i>
IP4-11	Adaptive Power Delivery System Management for Many-Core Processors with On/Off-Chip Voltage Regulators.....1265 <i>Haoran Li, Jiang Xu, Zhe Wang, Peng Yang, Rafael K. V. Maeda and Zhongyuan Tian</i>
IP4-12	Flying and Decoupling Capacitance Optimization for Area-Constrained On-Chip Switched-Capacitor Voltage Regulators.....1269 <i>Xiaoyang Mi, Hesam Fathi Moghadam and Jae-sun Seo</i>
IP4-13	Enhancing Analog Yield Optimization for Variation-aware Circuits Sizing.....1273 <i>Ons Lahiouel, Mohamed H. Zaki and Sofiène Tahar</i>
IP4-14	A New Sampling Technique for Monte Carlo-based Statistical Circuit Analysis.....1277 <i>Hiwa Mahmoudi and Horst Zimmermann</i>
IP4-15,	Automatic Technology Migration of Analog IC Designs using Generic Cell Libraries.....1281 <i>José Cachaço, Nuno Machado, Nuno Lourenço, Jorge Guilherme and Nuno Horta,</i>
IP4-16	Noise-Sensitive Feedback Loop Identification in Linear Time-Varying Analog Circuits.....1285 <i>Ang Li, Peng Li, Tingwen Huang and Edgar Sánchez-Sinencio</i>
IP4-17	CAnDy-TM: Comparative Analysis of Dynamic Thermal Management in Many-Cores using Model Checking.....1289 <i>Syed Ali Asadullah Bukhari, Faiq Khalid Lodhi, Osman Hasan, Muhammad Shafique and Jörg Henkel</i>
IP4-18	Power Pre-Characterized Meshing Algorithm for Finite Element Thermal Analysis of Integrated Circuits.....1293 <i>Shohdy Abdelkader, Alaa ELRouby and Mohamed Dessouky</i>

Session Title	Wearable and Smart Medical Devices Day: Diagnosis and prevention systems
Session Code / Room	10.1 / 5BC
Date / Time	Thursday, March 30, 2017 / 11:00 – 12:30
Chair	José L. Ayala, <i>Universidad Complutense de Madrid, ES</i>
Co-Chair	Chris Van Hoof, <i>IMEC, BE</i>
10.1.1 11:00 – 11:20	Enabling Technologies for Next Generation Bioanalytics on Chip.....N/A <i>Carlota Guiducci</i>
10.1.2 11:20 – 11:45	Bioelectronics Medicines - Bridging Biology with Technology.....N/A <i>Firat Yazicioglu</i>
10.1.3 11:45 – 12:05	Prediction Models in the State-of-the-Art Wireless Monitoring Devices.....N/A <i>Josué Pagán, Ramin Fallahzadeh, Hassan Ghasemzadeh, José M. Moya, José L. Risco-Martín and José L. Ayala</i>
10.1.4 12:05 – 12:30	Wearable Electronics - What is it Good for - and What is Missing to Support the Quality of Life of Elderly People?.....N/A <i>Ralf Brederlow</i>

Session Title	Hot Topic Session: EDA as an Emerging Technology Enabler
Session Code / Room	10.2 / 4BC
Date / Time	Thursday, March 30, 2017 / 11:00 – 12:30
Chair	Mathias Soeken, <i>EPFL, CH,</i>
Co-Chair	Ian Oâ€™Connor, <i>Ecole Centrale de Lyon, FR</i>
10.2.1 11:00 – 11:30	Logic Optimization and Synthesis: Trends and Directions in Industry.....1303 <i>Luca Amarú, Patrick Vuillod, Jiong Luo and Janet Olson</i>
10.2.2 11:30 – 12:00	Carbon Nanotubes Enable Major Energy Efficiency Benefits for Sub-10nm Digital Systems.....N/A <i>Gage Hills, Max Shulaker, Chi-Shuen Lee, Peter Debacker, Marie Garcia Bardon, Praveen Raghavan, Aaron Thean</i>
10.2.3 12:00 – 12:15	Wave Pipelining for Majority-based Beyond-CMOS Technologies.....1306 <i>O. Zografos, A. De Meester, E. Testa, M. Soeken, P.-E. Gaillardon, G. De Micheli, L. Amarú, P. Raghavan, F. Catthoor, R. Lauwereins</i>
10.2.4 12:15 – 12:30	Design Automation for Quantum Architectures.....1312 <i>Martin Roetteler, Krysta M. Svore, Dave Wecker and Nathan Wiebe</i>

Session Title	Side-Channel Attacks
Session Code / Room	10.3 / 2BC
Date / Time	Thursday, March 30, 2017 / 11:00 – 12:30
Chair	Oscar Reparaz, <i>KU Leuven, BE</i>
Co-Chair	Wieland Fischer, <i>Infineon, DE,</i>
10.3.1 11:00 – 11:30	Side-Channel Plaintext-Recovery Attacks on Leakage-Resilient Encryption.....1318 <i>Thomas Unterluggauer, Mario Werner and Stefan Mangard</i>
10.3.2 11:30 – 12:00	Static Power Side-Channel Analysis of a Threshold Implementation Prototype Chip.....1324 <i>Thorben Moos, Amir Moradi and Bastian Richter</i>

10.3.3 Side-Channel Power Analysis of XTS-AES.....1330
12:00 – 12:30 *Chao Luo, Yunsi Fei and A. Adam Ding*

Session Title	Emerging Architectures for Reconfigurable Computing
Session Code / Room	10.4 / 3A
Date / Time	Thursday, March 30, 2017 / 11:00 – 12:30
Chair	Alessandro Cilardo , <i>University of Naples Federico II, IT</i>
Co-Chair	Florent de Dinechin , <i>ENS-Lyon, FR</i> ,

10.4.1 A Field Programmable Transistor Array Featuring Single-Cycle Partial/Full Dynamic
11:00 – 11:30 Reconfiguration.....1336
Jingxiang Tian, Gaurav Rajavendra Reddy, Jiajia Wang, William Swartz Jr., Yiorgos Makris and Carl Sechen

10.4.2 A Power Gating Switch Box Architecture in Routing Network of SRAM-Based FPGAs
11:30 – 12:00 in Dark Silicon Era.....1342
Zeinab Seifoori, Behnam Khaleghi and Hossein Asadi

10.4.3 A Static-Placement, Dynamic-Issue Framework for CGRA Loop Accelerator.....1348
12:00 – 12:30 *Zhongyuan Zhao, Weiguang Sheng, Weifeng He, ZhiGang Mao and Zhaoshi Li*

Session Title	Emerging NoC Directions
Session Code / Room	10.5 / 3C
Date / Time	Thursday, March 30, 2017 / 11:00 – 12:30
Chair	Jiang Xu , <i>Hong Kong University of Science and Technology, HK</i>
Co-Chair	Tushar Krishna , <i>GeorgiaTech, US</i>

10.5.1 Machine Learning Enabled Power-Aware Network-on-Chip Design.....1354
11:00 – 11:30 *Dominic DiTomaso, Ashif Sikder, Avinash Kodi and Ahmed Louri*

10.5.2 Performance Evaluation and Design Trade-offs for Wireless-enabled SMART NoC.....1360
11:30 – 12:00 *Karthi Duraisamy and Partha Pratim Pande*

10.5.3 Robust TSV-based 3D NoC Design to Counteract Electromigration and Crosstalk Noise.....1366
12:00 – 12:15 *Sourav Das, Janardhan Rao Doppa, Partha Pratim Pande and Krishnendu Chakrabarty*

10.5.4 Performance and Energy Aware Wavelength Allocation on Ring-Based WDM 3D
12:15 – 12:30 Optical NoC.....1372
J. Luo, A. Elantably, V.D. Pham, C. Killian, D. Chillet, S. Le Beux, O. Sentieys and I. O'Connor

Session Title	Approximate computing and neural networks for novel communication and multimedia systems
Session Code / Room	10.6 / 5A
Date / Time	Thursday, March 30, 2017 / 11:00 – 12:30
Chair	Norbert Wehn , <i>Technical University Kaiserslautern, DE</i> ,
Co-Chair	Gerogios Keramidas , <i>Think Silicon, GR</i>

10.6.1 Exploiting Special-Purpose Function Approximation for Hardware-Efficient QR-
11:00 – 11:30 Decomposition.....1378
Jochen Rust and Steffen Paul

10.6.2
11:30 – 12:00 Embracing Approximate Computing for Energy-Efficient Motion Estimation in High Efficiency Video Coding.....1384
Walaa El-Harouni, Semeen Rehman, Bharath Srinivas Prabakaran, Akash Kumar, Rehan Hafiz and Muhammad Shafique

10.6.3
12:00 – 12:30 Hardware Architecture of Bidirectional Long Short-Term Memory Neural Network for Optical Character Recognition.....1390
Vladimir Rybalkin, Norbert Wehn, Mohammad Reza Yousefi and Didier Stricker

Session Title	Adaptive and Resilient Cyber-Physical Systems
Session Code / Room	10.7 / 3B
Date / Time	Thursday, March 30, 2017/ 11:00 – 12:30
Chair	Rolf Ernst, TU Braunschweig, DE
Co-Chair	Paul PoP, Technical University of Denmark, DK

10.7.1
11:00 – 11:30 MoDNN: Local Distributed Mobile Computing System for Deep Neural Network.....1396
Jiachen Mao, Xiang Chen, Kent W. Nixon, Christopher Krieger and Yiran Chen

10.7.2
11:30 – 12:00 Energy-Adaptive Scheduling of Imprecise Computation Tasks for QoS Optimization in Real-Time MPSoC Systems.....1402
Junlong Zhou, Jianming Yan, Tongquan Wei, Mingsong Chen and Xiaobo Sharon Hu

10.7.3
12:00 – 12:15 Fix the Leak! An Information Leakage Aware Secured Cyber-Physical Manufacturing System.....1408
Sujit Rokka Chhetri, Sina Faezi and Mohammad Abdullah Al Faruque

10.7.4
12:15 – 12:30 Efficient Drone Hijacking Detection using Onboard Motion Sensors.....1414
Zhiwei Feng, Nan Guan, Mingsong Lv, Weichen Liu, Qingxu Deng, Xue Liu and Wang Yi

Session Title	Lunch Time Keynote Session
Session Code / Room	11.0/Garden Foyer
Date / Time	Thursday, March 30, 2017 / 13:30 – 14:00
Chair	David Atienza, EPFL, CH,

11.0.1
13:20 – 13:50 The Engineering to Medicine Metamorphosis.....xxxviii
Sani R. Nassif,

Session Title	Wearable and Smart Medical Devices Day: HW and SW design constraints in medical devices
Session Code / Room	11.1 / 5BC
Date / Time	Thursday, March 30, 2017 / 14:00 – 15:30
Chair	José L. Ayala, Universidad Complutense de Madrid, ES
Co-Chair	Chris Van Hoof, IMEC, BE

11.1.1
14:00 – 14:30 Reconfigurable Embedded Systems Applications for Versatile Biomedical Measurements.....1420
Luca Cerina and Marco D. Santambrogio

11.1.2
14:30 – 15:00 Ultra Low Power Microelectronics for Wearable and Medical Devices.....1426
P.-F. Rüedi, A. Bishof, M. K. Augustyniak, P. Persechini, J.-L. Nagel, M. Pons, S. Emery and O. Chételat

11.1.3 Design Challenges for Wearable EMG Applications.....1432
15:00 – 15:30 *Bojan Milosevic, Simone Benatti and Elisabetta Farella*

Session Title	Emerging Technologies for Future Memory Design
Session Code / Room	11.2 / 4BC
Date / Time	Thursday, March 30, 2017 / 14:00 – 15:30
Chair	Weisheng Zhao, Beihang University, CN,
Co-Chair	Jean-Michel Portal, Aix-Marseille Université, FR,

11.2.1 Hybrid VC-MTJ/CMOS Non-volatile Stochastic Logic for Efficient Computing.....1438
14:00 – 14:30 *Shaodi Wang, Saptadeep Pal, Tianmu Li, Andrew Pan, Cecile Grezes, Pedram Khalili-Amiri, Kang L. Wang and Puneet Gupta*

11.2.2 Design and Benchmarking of Ferroelectric FET based TCAM.....1444
14:30 – 15:00 *Xunzhao Yin, Michael Niemier and X. Sharon Hu*

11.2.3 Leveraging Access Port Positions to Accelerate Page Table Walk in DWM-based Main Memory.....1450
15:00 – 15:15 *Hoda Aghaei Khouzani, Pouya Fotouhi, Chengmo Yang and Guang R. Gao*

11.2.4 VAET-STT: A Variation Aware Estimator Tool for STT-MRAM based Memories.....1456
15:15 – 15:30 *Sarath Mohanachandran Nair, Rajendra Bishnoi, Mohammad Saber Golanbari, Fabian Oboril and Mehdi B. Tahoori*

Session Title	Exploiting Heterogeneity for Big Data Computing
Session Code / Room	11.3 / 2BC
Date / Time	Thursday, March 30, 2017 / 14:00 – 15:30
Chair	Georgios Keramidas, Think Silicon S.A./Technological Educational Institute of Western Greece, GR
Co-Chair	Houman Homayoun, George Mason University, US

11.3.1 A Novel Zero Weight/Activation-Aware Hardware Architecture of Convolutional Neural Network.....1462
14:00 – 14:30 *Dongyoung Kim, Junwhan Ahn and Sungjoo Yoo*

11.3.2 A Mechanism for Energy-Efficient Reuse of Decoding and Scheduling of x86 Instruction Streams.....1468
14:30 – 15:00 *Marcelo Brandalero and Antonio Carlos S. Beck*

11.3.3 Understanding the Impact of Precision Quantization on the Accuracy and Energy of Neural Networks.....1474
15:00 – 15:15 *Soheil Hashemi, Nicholas Anthony, Hokchhay Tann, R. Iris Bahar and Sherief Reda*

11.3.4 Big vs Little Core for Energy-Efficient Hadoop Computing.....1480
15:15 – 15:30 *Maria Malik, Katayoun Neshatpour, Tinoosh Mohsenin, Avesta Sasan and Houman Homayoun*

Session Title	Advances in Timing and Layout
Session Code / Room	11.4 / 3A
Date / Time	Thursday, March 30, 2017 / 14:00 – 15:30
Chair	Mark Po-Hung Lin , <i>National Chung Cheng University, TW</i>
Co-Chair	Ibrahim Elfadel , <i>Masdar Institute of Technology, AE</i>
11.4.1 14:00 – 14:30	Quantifying Error: Extending Static Timing Analysis with Probabilistic Transitions.....1486 <i>Kevin E. Murray, Andrea Suardi, Vaughn Betz and George Constantinides</i>
11.4.2 14:30 – 15:00	On Refining Standard Cell Placement for Self-aligned Double Patterning.....1492 <i>Ye-Hong Chen, Sheng-He Wang and Ting-Chi Wang</i>
11.4.3 15:00 – 15:15	Cut Mask Optimization for Multi-Patterning Directed Self-Assembly Lithography.....1498 <i>Wachirawit Ponghiran, Seongbo Shim and Youngsoo Shin</i>
11.4.4 15:15 – 15:30	Clock Data Compensation Aware Clock Tree Synthesis in Digital Circuits with Adaptive Clock Generation.....1504 <i>Taesik Na, Jong Hwan Ko and Saibal Mukhopadhyay</i>

Session Title	Smart Energy and Automotive Systems
Session Code / Room	11.5 / 3C
Date / Time	Thursday, March 30, 2017 / 14:00 – 15:30
Chair	Geoff Merrett , <i>University of Southampton, GB</i>
Co-Chair	Michele Magno , <i>ETHZ, CH</i> ,

11.5.1 14:00 – 14:30	On Reducing Busy Waiting in AUTOSAR via Task-Release-Delta-based Runnable Reordering.....1510 <i>Robert Höttger, Burkhard Igel and Olaf Spinczyk</i>
11.5.2 14:30 – 15:00	Power Neutral Performance Scaling for Energy Harvesting MP-SoCs.....1516 <i>Benjamin J. Fletcher, Domenico Balsamo and Geoff V. Merrett</i>
11.5.3 15:00 – 15:15	Efficient Decentralized Active Balancing Strategy for Smart Battery Cells.....1522 <i>Nitin Shivaraman, Arvind Easwaran and Sebastian Steinhorst</i>
11.5.4 15:15 – 15:30	WULoRa: An Energy Efficient IoT End-Node for Energy Harvesting and Heterogeneous Communication.....1528 <i>Michele Magno, Faycal Ait Aoudia, Matthieu Gautier, Olivier Berder and Luca Benini</i>

Session Title	Dependable microprocessors and systems
Session Code / Room	11.6 / 5A
Date / Time	Thursday, March 30, 2017 / 14:00 – 15:30
Chair	Maksim Jenihhin , <i>Tallinn University of Technology, EE</i>
Co-Chair	Antonio Miele , <i>Politecnico di Milano, IT</i>
11.6.1 14:00 – 14:30	Characterization of Stack Behavior Under Soft Errors.....1534 <i>Junchi Ma and Yun Wang</i>
11.6.2 14:30 – 15:00	Multi-Armed Bandits for Efficient Lifetime Estimation in MPSoC design.....1540 <i>Calvin Ma, Aditya Mahajan and Brett H. Meyer</i>
11.6.3 15:00 – 15:30	Hardware-Based On-Line Intrusion Detection via System Call Routine Fingerprinting.....1546 <i>Liwei Zhou and Yiorgos Makris</i>

Session Title	Formal Methods and Verification: Core Technologies and Applications
Session Code / Room	11.7 / 3B
Date / Time	Thursday, March 30, 2017 / 14:00 – 15:30
Chair	Barbara Jobstmann, EPFL / Cadence, CH
Co-Chair	Christoph Scholl, University of Freiburg, DE

- 11.7.1** Static Netlist Verification for IBM High-Frequency Processors using a Tree-Grammar.....1552
14:00 – 14:30 *Christoph Jäschke, Ulla Herter, Claudia Wolkober, Carsten Schmitt and Christian Zoellin*
- 11.7.2** Reverse Engineering of Irreducible Polynomials in GF(2m) Arithmetic.....1558
14:30 – 15:00 *Cunxi Yu, Daniel Holcomb and Maciej Ciesielski*
- 11.7.3** Formal Specification and Dependability Analysis of Optical Communication Networks.....1564
15:00 – 15:30 *Umar Siddique, Khaza Anuarul Hoque and Taylor T. Johnson*

Session Title	Hot Topic Session: Biologically-inspired techniques for smart, secure and low power SoCs
Session Code / Room	11.8 / Exhibition Theatre
Date / Time	Thursday, March 30, 2017 / 14:00 – 15:30
Chair	Andy M. Tyrrell, University of York, GB
Co-Chair	Lukas Sekanina, Brno University of Technology, CZ

- 11.8.1** An Evolutionary Approach to Runtime Variability Mapping and Mitigation on a Multi-Reconfigurable Architecture.....1570
14:00 – 14:30 *Simon J. Bale, Pedro B. Campos, Martin A. Trefzer, James A. Walker and Andy M. Tyrrell*
- 11.8.2** Towards Low Power Approximate DCT Architecture for HEVC Standard.....1576
14:30 – 14:45 *Zdenek Vasicek, Vojtech Mrazek and Lukas Sekanina*
- 11.8.3** Semantic Driven Hierarchical Learning for Energy-Efficient Image Classification.....1582
14:45 – 15:00 *Priyadarshini Panda and Kaushik Roy*
- 11.8.4** Machine Learning for Run-Time Energy Optimisation in Many-Core Systems.....1588
15:00 – 15:15 *Dwaipayan Biswas, Vibishna Balagopal, Rishad Shafik, Bashir M. Al-Hashimi and Geoff V. Merrett*
- 11.8.5** An Evolutionary Approach to Hardware Encryption and Trojan-Horse Mitigation.....1593
15:15 – 15:30 *Andrea Marcelli, Marco Restifo, Ernesto Sanchez and Giovanni Squillero*

Session Title	Interactive Presentations
Session Code / Room	IP5/IP area
Date / Time	Thursday, March 30, 2017 / 15:30 – 16:00

- IP5-1** Formal Model for System-Level Power Management Design.....1599
Mirela Simonovic Vojin Zivojnovic and Lazar Saranovac
- IP5-2** Extending Memory Capacity of Neural Associative Memory based on Recursive Synaptic Bit Reuse.....1603
Tianchan Guan, Xiaoyang Zeng and Mingoo Seok
- IP5-3** Anomalies in Scheduling Control Applications and Design Complexity.....1607
Amir Aminifar and Enrico Bini

IP5-4	Contract-Based Integration of Automotive Control Software.....1611 <i>Tobias Sehnke, Matthias Schultalbers and Rolf Ernst</i>
IP5-5	Modeling and Integrating Physical Environment Assumptions in Medical Cyber-Physical System Design.....1615 <i>Zhicheng Fu, Chunhui Guo, Shangping Ren, Yu Jiang and Lui Sha</i>
IP5-6	A Utility-Driven Data Transmission Optimization Strategy in Large Scale Cyber-Physical Systems.....1619 <i>Soumi Chattopadhyay, Ansuman Banerjee and Bei Yu</i>
IP5-7	Protect Non-volatile Memory from Wear-out Attack based on Timing Difference of Row Buffer Hit/Miss.....1623 <i>Haiyu Mao, Xian Zhang, Guangyu Sun and Jiwu Shu</i>
IP5-8	Effects of Cell Shapes on the Routability of Digital Microfluidic Biochips.....1627 <i>Leonard Schneider, Oliver Keszocze, Jannis Stoppe and Rolf Drechsler</i>
IP5-9	LESS: Big Data Sketching and Encryption on Low Power Platform.....1631 <i>Amey Kulkarni, Colin Shea, Houman Homayoun and Tinoosh Mohsenin</i>
IP5-10	TruncApp: A Truncation-based Approximate Divider for Energy Efficient DSP Applications.....1635 <i>Shaghayegh Vahdat, Mehdi Kamal, Ali Afzali-Kusha, Massoud Pedram and Zainalabedin Navabi</i>
IP5-11,	Timing-Aware Wire Width Optimization for SADP Process.....1639 <i>Youngsoo Song, Sangmin Kim and Youngsoo Shin</i>
IP5-12	Formal Timing Analysis of Non-Scheduled Traffic in Automotive Scheduled TSN Networks.....1643 <i>Fedor Smirnov, Michael Glaß, Felix Reimann and Jürgen Teich</i>
IP5-13	Ultra Low-Power Visual Odometry for Nano-Scale Unmanned Aerial Vehicles.....1647 <i>Daniele Palossi, Andrea Marongiu and Luca Benini,</i>
IP5-14	Long Range Wireless Sensing Powered by Plant-Microbial Fuel Cell.....1651 <i>Maurizio Rossi, Pietro Tosato, Luca Gemma, Luca Torquati, Cristian Catania, Sergio Camalò and Davide Brunelli</i>
IP5-15	On the Cooperative Automatic Lane Change: Speed Synchronization and Automatic ``Courtesy".....1655 <i>Alexandre Lombard, Florent Perronnet, Abdeljalil Abbas-Turki and Abdellah El Moudni</i>
IP5-16	Evaluating Matrix Representations for Error-Tolerant Computing.....1659 <i>Pareesa Ameneh Golnari and Sharad Malik</i>
IP5-17	Simulation-Based Design Procedure for sub 1V CMOS Current Reference.....1663 <i>Dmitry Osipov and Steffen Paul</i>

Session Title	Advances in Microfluidics and Neuromorphic Architectures
Session Code / Room	12.2 /4BC
Date / Time	Thursday, March 30, 2017/ 16:00 – 17:30
Chair	Tsung-Yi Ho, National Tsing Hua University, TW
Co-Chair	Li Jiang, Shanghai Jiao Tong University, CN

12.2.1 16:00 – 16:30	Fast Architecture-Level Synthesis of Fault-Tolerant Flow-Based Microfluidic Biochips.....1667 <i>Wei-Lun Huang, Ankur Gupta, Sudip Roy, Tsung-Yi Ho and Paul Pop</i>
12.2.2 16:30 – 17:00	CoSyn: Efficient Single-Cell Analysis Using a Hybrid Microfluidic Platform.....1673 <i>Mohamed Ibrahim, Krishnendu Chakrabarty and Ulf Schlichtmann</i>
12.2.3 17:00 – 17:15	Verification of Networked Labs-on-Chip Architectures.....1679 <i>Andreas Grimmer, Werner Haselmayr, Andreas Springer and Robert Wille</i>

12.2.4 Synthesis of Activation-Parallel Convolution Structures for Neuromorphic Architectures.....1685
17:15 – 17:30 Seban Kim and Jaeyong Chung

Session Title	Security Tools
Session Code / Room	12.3 / 2BC
Date / Time	Thursday, March 30, 2017 / 16:00 – 17:30
Chair	Francesco Regazzoni, AlaRI/USI, CH
Co-Chair	Georg Sigl, TU Munich, DE

12.3.1 Register Transfer Level Information Flow Tracking for Provably Secure Hardware Design.....1691
16:00 – 16:30 Armaiti Ardeshiricham, Wei Hu, Joshua Marxen and Ryan Kastner

12.3.2 Dude, Is My Code Constant Time?.....1697
16:30 – 17:00 Oscar Reparaz, Josep Balasch and Ingrid Verbauwhede

12.3.3 Information Flow Tracking in Analog/Mixed-Signal Designs through Proof-Carrying Hardware IP.....1703
17:00 – 17:30 Mohammad-Mahdi Bidmeshki, Angelos Antonopoulos and Yiorgos Makris

Session Title	Formal and Predictive Models for System Design
Session Code / Room	12.4 / 3A
Date / Time	Thursday, March 30, 2017/ 16:00 – 17:30
Chair	Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE,
Co-Chair	Michael Huebner, Ruhr-University Bochum, DE

12.4.1 Sampling-Based Binary-Level Cross-Platform Performance Estimation.....1709
16:00 – 16:30 Xinnian Zheng, Haris Vikalo, Shuang Song, Lizy K. John and Andreas Gerstlauer

12.4.2 A Layered Formal Framework for Modeling of Cyber-Physical Systems.....1715
16:30 – 17:00 George Ungureanu and Ingo Sander

12.4.3 Efficient Synchronization Methods for LET-based Applications on a Multi-Processor System on Chip.....1721
17:00 – 17:30 Gabriela Breaban, Sander Stuijk and Kees Goossens

Session Title	Power Modeling, Estimation and Verification
Session Code / Room	12.5 / 3C
Date / Time	Thursday, March 30, 2017 / 16:00 – 17:30
Chair	Pascal Vivet, CEA-Leti, FR
Co-Chair	Hiroshi Nakamura, University of Tokyo, JP

12.5.1 Physics-based Electromigration Modeling and Assessment for Multi-Segment Interconnects in Power Grid Networks.....1727
16:00 – 16:30 Xiaoyi Wang, Hongyu Wang, Jian He, Sheldon X.-D. Tan, Yici Cai and Shengqi Yang

12.5.2 Fast Leakage Aware Thermal Simulator for 3D Chips.....1733
16:30 – 17:00 Hameedah Sultan and Smruti R. Sarangi

12.5.3 Blind Identification of Power Sources in Processors.....1739
17:00 – 17:15 Sherief Reda and Adel Belouchrani

12.5.4 Fast Low Power Rule Checking for Multiple Power Domain Design.....1745
17:15 – 17:30 *Chien-Pang Lu and Iris Hui-Ru Jiang*

Session Title	Efficient design methodologies for high-performance analog circuits and systems.
Session Code / Room	12.6 / 5A
Date / Time	Thursday, March 30, 2017 / 16:00 – 17:30
Chair	Nuno Horta, Instituto de Telecomunicacoes, PT
Co-Chair	Deuk Heo, Washington State University, US

12.6.1 Benefits of Asynchronous Control for Analog Electronics: Multiphase Buck Case Study.....1751
16:00 – 16:30 *Danil Sokolov, Vladimir Dubikhin, Victor Khomenko, David Lloyd, Andrey Mokhov and Alex Yakovlev*

12.6.2 High-Density MOM Capacitor Array with Novel Mortise-Tenon Structure for Low-Power SAR ADC.....1757
16:30 – 17:00 *Nai-Chen Chen, Pang-Yen Chou, Helmut Graeb and Mark Po-Hung Lin*

12.6.3 Adaptive Interference Rejection in Human Body Communication using Variable Duty Cycle Integrating DDR Receiver.....1763
17:00 – 17:30 *Shovan Maity, Debayan Das and Shreyas Sen*

Session Title	Software optimization for emerging memory architectures and technologies
Session Code / Room	12.7 / 3B
Date / Time	Thursday, March 30, 2017 / 16:00 – 17:30
Chair	Semeen Rehman, Technische Universitaet Dresden, DE
Co-Chair	Gianpiero Cabodi, Politecnio di Torino, IT

12.7.1 Efficient Storage Management for Aged File Systems on Persistent Memory.....1769
16:00 – 16:30 *Kaisheng Zeng, Youyou Lu, Hu Wan and Jiwu Shu*

12.7.2 LookNN: Neural Network with No Multiplication.....1775
16:30 – 17:00 *Mohammad Samragh Razlighi, Mohsen Imani, Farinaz Koushanfar and Tajana Rosing*

12.7.3 Pegasus: Efficient Data Transfers for PGAS Languages on Non-Cache-Coherent Many-Cores.....1781
17:00 – 17:30 *Manuel Mohr and Carsten Tradowsky*

Session Title	Hot Topic Session: Cyberphysical Microfluidic Biochips: EDA Challenges and Opportunities to Bridge the Gap between Microfluidics and Microbiology
Session Code / Room	12.8 / Exhibition Theatre
Date / Time	Thursday, March 30, 2017 / 16:00 – 17:30
Chair	Jan Madsen, Technical University of Denmark, DK
Co-Chair	Seetal Potluri, Technical University of Denmark, DK

12.8.1 Digital-Microfluidic Biochips for Quantitative Analysis: Bridging the Gap between Microfluidics and Microbiology.....1787
16:00 – 16:30 *Mohamed Ibrahim and Krishnendu Chakrabarty*

12.8.2 The Case for Semi-Automated Design of Microfluidic Very Large Scale Integration (mVLSI) Chips.....1793
16:30 – 17:00 *Jeffrey McDaniel, William H. Grover and Philip Brisk*

12.8.3	Synthesis of On-chip Control Circuits for mVLSI Biochips.....1799
17:00 – 17:15	<i>Seetal Potluri, Alexander Schneider, Martin Hørslev-Petersen, Paul Pop and Jan Madsen</i>
12.8.4	Scheduling and Optimization of Genetic Logic Circuits on Flow-Based Microfluidic Biochips.....1805
17:15 – 17:30	<i>Yu-Jhih Chen, Sumit Sharma, Sudip Roy and Tsung-Yi Ho</i>

Additional Papers:

The Engineering Challenges in Quantum Computing.....836
<i>C. G. Almudever, L. Lao, X. Fu, N. Khammassi, I. Ashraf, D. Iorga, S. Varsamopoulos, C. Eichler, A. Wallraff, L. Geck, A. Kruth, J. Knoch, H. Bluhm, K Bertels</i>
An Optimal Approach for Low-Power Migraine Prediction Models in the State-of-the-Art Wireless Monitoring Devices.....1297
<i>Josue Pagan, Ramin Fallahzadeh, Hassan Ghasemzadeh, Jose M. Moya, Jose L. Risco-Martin</i>
Mixed-Criticality Processing Pipelines.....1811
<i>Dionisio de Niz, Bjorn Andersson, Hyoseung Kim, Mark Klein, Linh Thi Xuan Phan, and Raj Rajkumar</i>