

2016 International Conference on Field-Programmable Technology (FPT 2016)

**Xi'an, China
7-9 December 2016**



**IEEE Catalog Number: CFP16528-POD
ISBN: 978-1-5090-5603-3**

**Copyright © 2016 by the Institute of Electrical and Electronics Engineers, Inc
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP16528-POD
ISBN (Print-On-Demand):	978-1-5090-5603-3
ISBN (Online):	978-1-5090-5602-6

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

CONTENT

Message from the General Chair and Program Co-Chairs

Yu Peng, Brent Nelson and Shaojun Wang

Organization

Table of Contents

Keynote Lecture

High – Level Synthesis – The Right Side of History	1
The Configurable Cloud – Accelerating Hyperscale Datacenter Services with FPGAs.....	2
FPGA as Service in Public Cloud: Why and How	3

Device

High Density, Low Energy, Magnetic Tunnel Junction Based Block RAMs for Memory-rich FPGAs.....	4
<i>Kosuke Tatsumura, Sadegh Yazdanshenas and Vaughn Betz</i>	
Analysis of Transient Voltage Fluctuations in FPGAs	12
<i>Dennis R.E. Gnad, Fabian Oboril, Saman Kiamehr and Mehdi B. Tahoori</i>	
An Energy-Efficient Near/Sub-Threshold FPGA Interconnect Architecture Using Dynamic Voltage Scaling and Power-Gating	20
<i>He Qi, Oluseyi Ayorinde and Benton H. Calhoun</i>	

Architecture

Integer Computations with Soft GPGPU on FPGAs.....	28
<i>Muhammed Al Kadi and Michael Huebner</i>	
Network-Attached FPGAs for Data Center Applications.....	36
<i>Jagath Weerasinghe, Raphael Polig, Francois Abel, Christoph Hagleitner</i>	
Hypervisor Mechanisms to Manage FPGA Reconfigurable Accelerators.....	44
<i>Tian Xia, Jean-Christophe Prévotet and Fabienne Nouvel</i>	

Application

FPGA-based Acceleration of FDAS Module Using OpenCL	53
<i>Haomiao Wang, Ming Zhang, Prabu Thiagaraj and Oliver Sinnem</i>	
Automatic Code Generation of Convolutional Neural Networks in FPGA Implementation.....	61
<i>Zhiqiang Liu, Yong Dou, Jingfei Jiang and Jinwei Xu</i>	
An Efficient Implementation of Online Arithmetic	69
<i>Yiren Zhao, John Wickerson and George A. Constantinides</i>	
Accelerating Binarized Neural Networks:Comparison of FPGA, CPU, GPU, and ASIC.....	77
<i>Eriko Nurvitadhi, David Sheffield, Jaewoong Sim, Asit Mishra, Ganesh Venkatesh and Debbie Marr</i>	

Random Projections for Scaling Machine Learning on FPGAs	85
<i>Sean Fox, Stephen Tridgell, Craig Jin and Philip H.W. Leong</i>	
High-speed Regular Expression Matching with Pipelined Automata.....	93
<i>Denis Matoušek, Jan Kořenek and Viktor Puš</i>	
Reliability	
Fine-grained Module-based Error Recovery in FPGA-based TMR Systems.....	101
<i>Zhuoran Zhao, Dimitris Agiakatsikas, Nguyen T. H. Nguyen, Ediz Cetin and Oliver Diessel</i>	
Enhanced Source-Level Instrumentation for FPGA In-System Debug of High-Level Synthesis Designs	109
<i>Jose P. Pinilla and Steven J. E. Wilton</i>	
A Programmable Configuration Controller for Fault-Tolerant Applications.....	117
<i>Lingkan Gong, Tong Wu, Nguyen T. H. Nguyen, Dimitris Agiakatsikas, Zhuoran Zhao, Ediz Cetin and Oliver Diessel</i>	
High Level Synthesis (HLS)	
Tessellation-Based Multi-Block Memory Mapping Scheme for High-Level Synthesis with FPGA	125
<i>Juan Escobedo and Mingjie Lin</i>	
High-Level Synthesis of Resource-Shared Microarchitectures from Irregular Complex C-Code	133
<i>Björn Liebig and Andreas Koch</i>	
Spector: An OpenCL FPGA Benchmark Suite	141
<i>Quentin Gautier, Alric Althoff, Pingfan Meng and Ryan Kastner</i>	
Network on Chip (NoC)	
Deflection Routing for Multi-Level FPGA Overlay NoCs.....	149
<i>Chethan Kumar H B, Shubham Agarwal and Nachiket Kapre</i>	
Hybrid Hard NoCs for Efficient FPGA Communication.....	157
<i>Tianqi Liu, Naveen Kumar Dumpala and Russell Tessier</i>	
Poster	
Debugging Framework for FPGA-based Soft Processors	165
<i>David Sidler and Ken Eguro</i>	
Dynamic Scheduling of Voter Checks in FPGA-based TMR Systems.....	169
<i>Nguyen T. H. Nguyen, Dimitris Agiakatsikas, Ediz Cetin and Oliver Diessel</i>	
Energy-aware Scheduling for Task Adaptive FPGAs.....	173
<i>Wei Ting Loke and Chin Yang Koay</i>	
Enrich C-Based High – Level Synthesis with Parallel Pattern Templates.....	177
<i>Lana Josipovic, Nithin George and Paolo Ienne</i>	
Automatic Wire Modeling to Explore Novel FPGA Architectures	181
<i>Grace Zgheib and Paolo Ienne</i>	
Rapid Design Space Exploration for Soft Core Processor Customization and Selection.....	185
<i>Deshya Wijesundera, Alok Prakashy and Thambipillai Srikanthan</i>	
Application Debug in FPGAs in the Presence of Multiple Asynchronous Clocks.....	189
<i>Georgios Tzimpragos, Da Cheng, Stephanie Tapp, Balakrishna Jayadev and Amitava Majumdar</i>	
Hardware Trojan Avoidance and Detection for Dynamically Re-configurable FPGAs	193
<i>Nandeesha Veeranna and Benjamin Carrion Schafer</i>	

Dataflow Design for Optimal Incremental SVM Training	197
<i>Shengjia Shao, Oskar Mencer and Wayne Luk</i>	
FPGA Acceleration of TreePM N-body Simulations for Modified Newton Dynamics	201
<i>Tianqi Wang, Linlin Zheng, Xi Jin, Bo Peng, Chuanjun Wang</i>	
hCODE: An Open-source Platform for FPGA Accelerators.....	205
<i>Qian Zhao, Takuya Nakamichi, Motoki Amagasaki, Masahiro Iida, Morihiro Kugaand Toshinori Sueyoshi</i>	
Fast polynomial arithmetic for Somewhat Homomorphic Encryption operations in hardware with Karatsuba algorithm...	209
<i>Vincent Migliore, Maria Méndez Real, Vianney Lapotre, Arnaud Tisserandz, Caroline Fontainey and Guy Gogniat</i>	
FAU: Fast and Error-Optimized Approximate Adder Units on LUT-Based FPGAs	213
<i>Jorge Echavarria, Stefan Wildermann, Andreas Becher, Jürgen Teich and Daniel Ziener</i>	
Variable Pipeline Structure for Coarse Grained Reconfigurable Array CMA	217
<i>Naoki Ando, Koichiro Masuyama, Hayate Okuhara and Hideharu Amano</i>	
A survey of NoC evaluation platforms on FPGAs	221
<i>Otavio A. de Lima Jr., Virginie Fresse and Frédéric Rousseau</i>	
A Modular Architecture for Dynamically Reconfigurable Middlebox with Customized Reconfiguration Handler	225
<i>Tze Hon Tan, Chia Yee Ooi and M. N. Marsono</i>	
Exploring Shared SRAM Tables Among NPN Equivalent Large LUTs in SRAM-Based FPGAs	229
<i>Ali Asghar, Muhammad Mazher Iqbal, Waqar Ahmed, Mujahid Ali, Husain Parvez and Muhammad Rashid</i>	
Enabling In-Situ Logic-In-Memory Capability Using Resistive-RAM Crossbar Memory.....	233
<i>Naifeng Jing, Taozhong Li, Zhongyuan Zhao, Wei Jin, Yanan Sun, Weifeng He and Zhigang Mao</i>	
Design and Implementation of Open-Source SATA III Core for Stratix V FPGAs.....	237
<i>Sumedh Guha, Wen Wang, Shafeeq Ibraheem, Mahesh Balakrishnan and Jakub Szefer</i>	
Time-Independent Discrete Gaussian Sampling For Post-Quantum Cryptography	241
<i>A. Khalid, J. Howe, C. Rafferty and M. O'Neill</i>	
High Performance Deformable Part Model Accelerator Based on FPGA.....	245
<i>Qi Zhan, Min Gao, Li Jiao, Wei Cao, Xuegong Zhou and Lingli Wang</i>	
FPGA Implementation of a Real-Time Super-Resolution System Using a Convolutional Neural Network.....	249
<i>Taito Manabe, Yuichiro Shibata and Kiyoshi Oguri</i>	
EMA-FPRMs: An Efficient Minimization Algorithm for Fixed Polarity Reed-Muller Expressions	253
<i>Zhenxue He, Limin Xiao, Longbing Zhang, Fei Gu, Zhisheng Huo,Mingfa Zhu, Li Ruan, Rui Liu and Xiang Wang</i>	
An Efficient FPGA Implementation of Mahalanobis Distance-Based Outlier Detection for Streaming Data	257
<i>Yuto Arai, Shin'ichi Wakabayashi, Shinobu Nagayama and Masato Inagi</i>	
Real-time Object Detection and Classification for High-Speed Asymmetric-Detection Time-Stretch Optical Microscopy on FPGA.....	261
<i>Maolin Wang, Ho-Cheung Ng, Bob M.F. Chung, B. Sharat Chandra Varma,Manish Kumar Jaiswal, Kevin K. Tsia, Ho Cheung Shum and Hayden Kwok-Hay So</i>	
Caffeinated FPGAs: FPGA Framework For Convolutional Neural Networks.....	265
<i>Roberto DiCecco, Griffin Lacey, Jasmina Vasiljevic, Paul Chow, Graham Taylor and Shawki Areibi</i>	
Hardware TCP Offload Engine based on 10-Gbps Ethernet for Low-Latency Network Communication.....	269
<i>Li Ding, Ping Kang, Wenbo Yin, Linli Wang</i>	

Fixed-ratio DXT Format Frame Buffer Compressor for Mobile Graphics Systems	273
<i>Yuzhi Zhou, Xi Jin, and Tian Xiang</i>	
A Memory-Based Realization of a Binarized Deep Convolutional Neural Network	277
<i>Hiroki Nakahara, Haruyoshi Yonekawa, Tsutomu Sasao, Hisashi Iwamoto and Masato Motomura</i>	
FPGA based Hardware Accelerator for KAZE Feature Extraction Algorithm.....	281
<i>Lester Kalms, Ahmed Elhossini and Ben Juurlink</i>	
IC Security Evaluation against Fault InjectionAttack Based on FPGA Emulation	285
<i>Song Xu, Qiang Liu, Tao Li and Hongxiang Fan</i>	
An Acceleration of a Random Forest Classification using Altera SDK for OpenCL	289
<i>Hiroki Nakahara, Akira Jinguji, Tomonori Fujii and Simpei Sato</i>	
Ph.D. Forum	
Functional Verification as a Tool for Monitoring Impact of Faults in SRAM-based FPGAs.....	293
<i>Jakub Podivinsky, Ondrej Cekan, Jakub Lojda and Zdenek Kotasek</i>	
Random Stimuli Generation Based on a Stochastic Context-Free Grammar	295
<i>Ondrej Cekan, Jakub Podivinsky and Zdenek Kotasek</i>	
Implementation of Fault Tolerant Techniques into FPNNs	297
<i>Martin Krcma, Zdenek Kotasek and Jakub Lojda</i>	
Evaluation of Variable Precision Computing with Variable Precision FFT Implementation on FPGA	299
<i>Mengjun Li, Yongxin Zhu, Xu Wang, Tian Huang, Weida Chen, Bin Liu and Yishu Mao</i>	
HLS-based Fault Tolerance Approach for SRAM-based FPGAs.....	301
<i>Jakub Lojda, Jakub Podivinsky, Martin Krcma, Zdenek Kotasek</i>	
Demo	
SMCFA: A Zynq-based Stacked Multi CPU-FPGA Architecture	303
<i>Lin Li and Quansheng Yang</i>	
A Moving Object Extraction and Classification System based on Zynq and IBM SuperVessel	307
<i>Zhehao Li, Jifang Jin, Lingli Wang, Ji Yang and Jiahua Lu</i>	
Implementation of Parallel Medical Ultrasound Imaging Algorithm on CAPI-Enabled FPGA	311
<i>Junying Chen, Shunseng Zhou and Huaqing Min</i>	
Asymmetric Multiprocessing for Motion Control based on Zynq SoC.....	315
<i>Xinyu CHEN, Yong GU, Chenxu WANG and Xuguang GUAN</i>	
Design Competition	
Identification of Trax Threats using Pattern Matching.....	319
<i>Donald G. Bailey</i>	
Trax Solver on Zynq Using Incremental Update Algorithm	323
<i>Hiroshi Nakahara, Tetsui Ohkubo ,Hideki Shimura ,Ryotaro Sakai,Chiharu Tsuruta,Takahiro Kaneda ,Hideharu Amano</i>	
Trax Player Implementation on FPGA using High Level Synthesis Tool	327
<i>Akira Kojima</i>	
Author Index	