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Tutorial Day
Sunday, August 21, 2016

9:00 am	**Tutorial 1**	**Using Next Generation Memory Technologies DRAM and Beyond**	
9:00 – 9:10	Introduction		Vidya Rajagopalan
9:10 – 9:45	Memory as We Approach a New Horizon 1		Thomas Pawlowski, **Micron Technology**
9:45 – 10:15	The Future of Graphic and Mobile Memory for New Applications ..13		Jim Kim, **Samsung**
11:15 – 11:35	**BREAK**		
11:35 – 11:10	The Era of High Bandwidth Memory 26		Kevin Tran, **SK Hynix**
11:10 – 11:45	HBM Package Integration: Technology Trends, Challenges and Applications 37		Suresh Ramalingam, **Xilinx**
11:45 – 12:15	Memory Technology and Applications 46		Allen Rush, **AMD**
12:15 – 12:30	Q & A Panel		
12:30 – 1:45	**Lunch**		
1:45 pm	**Tutorial 2**	**3D Depth for Consumers: From Sensors to Apps**	
1:45 – 2:00	Intro: 3D Sensors for the Rest of Us 53		Larry Yang, **Google**
2:00 – 2:30	VR and AR Anytime and Everywhere: Contributions of PMD Depth Sensing to an Evolving Ecosystem 60		Bernd Buxbaum, **PMD Tech**
2:30 – 3:00	"Speaking in Volumes": Volumetric Data 70 Acceleration for Dense SLAM		David Moloney, **Movidius**
3:00 – 3:30	Inuitive Breakthrough Solution for AR and VR Worlds 80		Dor Zepeniuk, **Inuitive**
3:30 – 3:45	**BREAK**		
3:45 – 4:15	3D Reconstruction with Tango 87 Mobile 3D Capture for Professional		Ivan Dryanovs, **Google**
4:15 – 5:00	Applications 99		Rafael Spring, **DotProduct**

5:00 – 6:00 **Reception**

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Conference Day 1
Monday, August 22, 2016

9:30 – 9:45am	**Introductory Remarks**		
9:45 – 11:15am	**Session 1**	**GPUs & HPCs**	
	The Bifrost GPU architecture and the ARM Mali-G71 GPU 118 Pascal GPU with NVLink 134 ARMv8-A Next Generation Vector Architecture for HPC 146		Jem Davies, **ARM** John Danskin, Denis Foley, **NVIDIA** Nigel Stephens, **ARM**
11:15 – 11:45am	**Break**	**Poster presentations**	
11:45 – 12:45pm	**Session 2**	**Mobile**	
	Helio X20: The First Tri-Gear Mobile SoC with CorePilotTM 3.0 Technology 162 Samsung's Exynos M1 Processor 174		David Lee, **Mediatek** Brad Burgess, **Samsung**
12:45 – 2:15pm	**Lunch**		
2:15 – 3:00pm	**Keynote 1**	Mixed Reality	
		Nick Baker, **Microsoft**	
3:00 – 4:00pm	**Session 3**	**Low Power SoC**	
	Design and Development of a an Ultra-Low Power x86 MCU Class SoCs 183 Introducting "PARKER" Next Generation Tegra System-on-Chip 198		Peter Barry, **Intel** Andi Skende, **NVIDIA**
4:00 – 4:30pm	**Break**	**Poster presentations**	
4:30 – 6:00pm	**Session 4**	**Vision & Imaging**	
	From Model to FPGA: Software-Hardware Co-Design for Efficient Neural Network Acceleration 207 The path to Embedded Vision and AI using a low power Vision DSP 221 High Performance DSP for Vision, Imaging and Neural Networks 235		Song Yao, **Deephi** and **Tsinghua University** Yair Siegel, **CEVA** Greg Efland, **Cadence**
6:00 – 7:30 pm	**Reception**		

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Conference Day 2
Tuesday, August 23, 2016

8:30 – 10:00am	**Session 5**	**Interconnects**	
	A 16nm 256-bit Wide 89.6GByte/s Total Bandwidth In-Package Interconnect with 0.3V Swing and 0.062pJ/bit Power in InFO Package 250	Mu-Shan Lin TSMC	
	100Gbit/s, 120km, PAM 4 Based Switch to Switch, Layer 2 Silicon Photonics based Optical Interconnects for Datacenters 266	Radhakrishnan Nagarajan, Sudeep Bhoja, **InPhi**, Tom Issenhuth, **Microsoft**	
	Intel Omni-Path 4.8 Tbps Switch ASIC and Platform 275	James Kunz, **Intel**	
10:00 -- 10:30am	**Break**	**Poster presentations**	
10:30 – 12:00pm	**Session 6**	**Emerging Embedded**	
	A "Zero-displacement" Active Ultrasonic Force Sensor for Mobile Applications 284	Sam Sheng, **Sentons**	
	Quantum Dot-Based Imagers for Multispectral Cameras and Sensors 294	Emanuele Mandelli, **InVisage**	
	Clearmotion: Building the World's First Super Active Suspension System 309	Shakeel Avadhany, **Levant**	
12:00 – 1:15pm	**Lunch**		
1:15 – 2:15pm	**Keynote 2**	Are We There Yet? Silicon in Self-Driving Cars	
		Daniel Rosenband, **Google**	
2:15 – 3:15pm	**Session 7**	**Multcore Research**	
	Piton: A 25-core Academic Manycore Research Processor 319	Michael McKeown, **Princeton University**	
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3:15 -- 3:45pm	**Break**	**Poster presentations**	
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	Embedded Deep Neural Networks: "The Cost of Everything and the Value of Nothing" 350	David Moloney, **Movidius**	
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5:15 – 5:45pm	**Break**	**Poster presentations**	
5:45 – 7:15pm	**Session 9**	**Processors**	
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	POWER9: Processor for the Cognitive Era 408	Brian Thompto, **IBM**	
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7:15 – 7:30pm	**Closing Remarks**		

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	A Dynamically Scheduled Architecture for the Synthesis of Graph Methods 436	Marco Minutoli*, Vito Giovanni Castellana*, Antonino Tumeo*, Marco Lattuada+, Fabrizio Ferrandi+	*High Performance Computing, Pacific Northwest National Laboratory, +DEIB, Politecnico di Milano
	LiveSynth: Towards an Interactive Synthesis Flow N/A	Rafael Trapani Possignolo, Jose Renau	University of California, Santa Cruz
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