

2017 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA 2017)

Hsinchu, Taiwan
24-27 April 2017



IEEE Catalog Number: CFP17846-POD
ISBN: 978-1-5090-5806-8

**Copyright © 2017 by the Institute of Electrical and Electronics Engineers, Inc
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

| | |
|-------------------------|-------------------|
| IEEE Catalog Number: | CFP17846-POD |
| ISBN (Print-On-Demand): | 978-1-5090-5806-8 |
| ISBN (Online): | 978-1-5090-5805-1 |
| ISSN: | 1930-8868 |

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

TABLE OF CONTENTS

| | |
|--|-----------|
| HETEROGENEOUS SOCS | 1 |
| <i>Subramanian S. Iyer</i> | |
| WORLD MEGATREND OF INTELLIGENT ROBOTICS AND AI: IMPACT ON VLSI-DAT | 2 |
| <i>Ren C. Luo</i> | |
| TCAD BASED DESIGN-TECHNOLOGY CO-OPTIMISATIONS IN ADVANCED TECHNOLOGY NODES | 3 |
| <i>Asen Asenov ; Karim El Sayed ; Ricardo Borges ; Plamen Asenov ; Campbell Millar ; Terry Ma</i> | |
| NEW EMBEDDED MEMORIES, FROM LAB TO FAB..... | 5 |
| <i>David Eggleston</i> | |
| EXTENDED ABSTRACT: INDUSTRIAL PERFORMANCE TO SERVE ECONOMICAL REBOUND | 6 |
| <i>Bertrand Bleneau</i> | |
| BUILDING BEST IN CLASS SYSTEM SOLUTIONS: ENABLED BY COLLABORATION | 8 |
| <i>Suhita Devineni</i> | |
| NAVIGATING THROUGH THE FRAGMENTED APPLICATION MAZE..... | 9 |
| <i>Keh-Ching Huang</i> | |
| RRAM TECHNOLOGY AND ITS EMBEDDED POTENTIAL ON IOT APPLICATIONS | 10 |
| <i>Chiahua Ho</i> | |
| SOFT ELECTRONICS FOR THE HUMAN BODY | 11 |
| <i>John A. Rogers</i> | |
| TERAHERTZ SYSTEMS-ON-CHIP ENABLED BY NANO-IC TECHNOLOGIES | 12 |
| <i>Mau-Chung Frank Chang</i> | |
| NOVEL MEMORY HIERARCHY WITH E-STT-MRAM FOR NEAR-FUTURE APPLICATIONS..... | 13 |
| <i>Shinobu Fujita ; Hiroki Noguchi ; Kazutaka Ikegami ; Susumu Takeda ; Kumiko Nomura ; Keiko Abe</i> | |
| LOW-CURRENT SPIN TRANSFER TORQUE MRAM | 15 |
| <i>G. Hu ; J. J. Nowak ; G. Lauer ; J. H. Lee ; J. Z. Sun ; J. Harms ; A. Annunziata ; S. Brown ; W. Chen ; Y. H. Kim ; N. Marchack ; S. Murthy ; C. Kothandaraman ; E. J. O'Sullivan ; J. H. Park ; M. Reuter ; R. P. Robertazzi ; P. L. Trouilloud ; Y. Zhu ; D. C. Worledge</i> | |
| EMBEDDED NONVOLATILE MEMORY WITH STT-MRAMS AND ITS APPLICATION FOR NONVOLATILE BRAIN-INSPIRED VLSIS..... | 17 |
| <i>Tetsuo Endoh</i> | |
| EMBEDDED NON-VOLATILE MEMORY SYSTEM AS AN ENabler OF SMARTER WORLD..... | 20 |
| <i>Takashi Kono</i> | |
| STT-MRAM MEMORIES FOR IOT APPLICATIONS: CHALLENGES AND OPPORTUNITIES AT CIRCUIT LEVEL AND ABOVE | 24 |
| <i>Massimo Alioto</i> | |
| UTILIZING NVDIMM TO ALLEVIATE THE I/O PERFORMANCE GAP FOR BIG DATA WORKLOADS | 25 |
| <i>Zili Shao</i> | |
| THE ROAD TO A TRILLION: MAKING THE IOT WORK..... | 26 |
| <i>Rob Aitken</i> | |
| VIRTUAL REALITY: THE NEW ERA OF THE FUTURE WORLD | 27 |
| <i>Raymond Pao</i> | |
| ANALYTICAL SOLUTION FOR RESURF AND BREAKDOWN CHARACTERISTICS OF FINGER STI DEMOS TRANSISTORS | 28 |
| <i>H. C. Tsai ; R. H. Liou ; C. H. Lien</i> | |
| IMPACTS OF WORK FUNCTION VARIATION AND LINE EDGE ROUGHNESS ON HYBRID TFET-MOSFET MONOLITHIC 3D SRAMS | 30 |
| <i>Jian-Hao Wang ; Pin Su ; Ching-Te Chuang</i> | |
| EVALUATION OF ANALOG PERFORMANCE OF MONOLAYER AND BILAYER TWO-DIMENSIONAL TRANSITION METAL DICHALCOGENIDE (TMD) MOSFETS..... | 32 |
| <i>Hung-Yi Lee ; Chang-Hung Yu ; Pin Su ; Ching-Te Chuang</i> | |
| PERFORMANCE EVALUATION OF PASS-TRANSISTOR-BASED CIRCUITS USING MONOLAYER AND BILAYER 2-D TRANSITION METAL DICHALCOGENIDE (TMD) MOSFETS FOR 5.9NM NODE..... | 34 |
| <i>Chang-Hung Yu ; Jun-Teng Zheng ; Pin Su ; Ching-Te Chuang</i> | |

| | |
|--|----|
| TWIN GATE TUNNEL FET BASED CAPACITORLESS DYNAMIC MEMORY | 36 |
| <i>Nupur Navlakha ; Jyi-Tsong Lin ; Abhinav Kranti</i> | |
| GE N-CHANNEL FINFET PERFORMANCE ENHANCEMENT USING LOW WORK FUNCTION METAL-INTERFACIAL LAYER-GE CONTACTS | 38 |
| <i>Prashanth P. Manik ; Sachin Dev ; Nayana Remesh ; Yaksh Rawal ; Siddhant Khopkar ; Saurabh Lodha</i> | |
| INVESTIGATION AND COMPARISON OF DESIGN SPACE FOR ULTRA-THIN-BODY GEOI/SOI NEGATIVE CAPACITANCE FETS | 40 |
| <i>Ho-Pei Lee ; Chien-Lin Yu ; Wei-Xiang You ; Pin Su</i> | |
| TEMPERATURE COMPENSATED SUPER-HIGH-FREQUENCY (2–8 GHz) SURFACE ACOUSTIC WAVE DEVICES | 42 |
| <i>Salahuddin Raju ; Changjian Zhou ; Bin Li ; Mansun Chan</i> | |
| IMPACT OF SUBSTRATE ON THE FREQUENCY BEHAVIOR OF TRANS-CONDUCTANCE IN ULTRATHIN BODY AND BOX FDSDI MOS DEVICES - A PHYSICAL INSIGHT | 44 |
| <i>Mandar Bhoir ; Pragya Kushwaha ; Yogesh S. Chauhan ; Nihar R. Mohapatra</i> | |
| TCAD-BASED CHARACTERIZATION OF LOGIC CELLS: POWER, PERFORMANCE, AREA, AND VARIABILITY | 46 |
| <i>Hw. Karner ; C. Kernstock ; Z. Stanojevic ; O. Baumgartner ; F. Schanovsky ; M. Karner ; D. Helms ; R. Eilers ; M. Metzdorf</i> | |
| SCALING OF GATE DIELECTRIC ON GE SUBSTRATE | 48 |
| <i>Yung-Hsiang Chan ; Bing-Yue Tsui</i> | |
| EUV EXTENDIBILITY RESEARCH AT BERKELEY LAB | 50 |
| <i>P. Naulleau ; C. Anderson ; M. Benk ; W. Chao ; K. Goldberg ; E. Gullikson ; M. Miyakawa ; A. Wojdyla</i> | |
| DSA: PROGRESS TOWARD INDUSTRY ACCEPTANCE | 52 |
| <i>Anthony Vanderheyden ; Darron Jurajda ; Douglas Guerrero</i> | |
| ELECTRON MULTI-BEAM TECHNOLOGY | 54 |
| <i>Elmar Platzgummer</i> | |
| NEGATIVE CAPACITANCE FETS WITH STEEP SWITCHING BY FERROELECTRIC HF-BASED OXIDE | 56 |
| <i>M. H. Lee ; P. -G. Chen ; S. -T. Fan ; C. -Y. Kuo ; H. -H. Chen ; S. -S. Gu ; Y. -C. Chou ; C. -H. Tang ; R. -C. Hong ; Z. -Y. Wang ; M. -H. Liao ; K. -S. Li ; M. -C. Chen ; C. W. Liu</i> | |
| III-V/GE MOSFETS AND TFETS FOR ULTRA-LOW POWER LOGIC LSIS | 58 |
| <i>Shinichi Takagi ; Mitsuru Takenaka</i> | |
| HIGH PERFORMANCE PMOS WITH STRAINED HIGH-GE-CONTENT SIGE FINS FOR ADVANCED LOGIC APPLICATIONS | 60 |
| <i>Pouya Hashemi ; Takashi Ando ; Karthik Balakrishnan ; Siyuranga Koswatta ; Kam-Leung Lee ; John A. Ott ; Kevin Chan ; John Bruley ; Sebastian U. Engelmann ; Vijay Narayanan ; Effendi Leobandung ; Renee T. Mo</i> | |
| INGAAs QUANTUM-WELL MOSFETS FOR FUTURE LOGIC APPLICATIONS | 62 |
| <i>Dae-Hyun Kim</i> | |
| FILAMENT CONTROL OF FIELD-ENHANCED WOX RESISTIVE MEMORY TOWARD LOW POWER APPLICATIONS | 63 |
| <i>Chao-Hung Wang ; Kuang-Hao Chiang ; Yu-Hsuan Lin ; Jau-Yi Wu ; Yung-Han Ho ; Erh-Kun Lai ; Dai-Ying Lee ; Ming-Hsui Lee ; Kuang-Yeu Hsieh ; Chih-Yuan Lu</i> | |
| OCCURRENCE AND SOLUTION TO OVERCOME 1ST RESET RESISTANCE PINNING EFFECT IN Ti/HFO_x BASED RRAM FOR LOW POWER NONVOLATILE MEMORY APPLICATIONS | 65 |
| <i>Sk. Ziaur Rahaman ; Heng-Yuan Lee ; Yu-De Lin ; Chien-Hua Hsu ; Kan-Hsueh Tsai ; Wei-Su Chen ; Yu-Sheng Chen ; Pang-Shiu Chen ; Pei-Hua Wang</i> | |
| A HIGH ACCURACY AND ROBUST MACHINE LEARNING NETWORK FOR PATTERN RECOGNITION BASED ON BINARY RRAM DEVICES | 67 |
| <i>Chen Liu ; Runze Han ; Sheng Zhang ; Maochuan Li ; Zheng Zhou ; Peng Huang ; Lifeng Liu ; Xiaoyan Liu ; Jinrong Kang</i> | |
| DESIGN AND OPTIMIZATION OF STRONG PHYSICAL UNCLONABLE FUNCTION (PUF) BASED ON RRAM ARRAY | 69 |
| <i>Yachuan Pang ; Huaiqiang Wu ; Bin Gao ; Rui Liu ; Shan Wang ; Shimeng Yu ; An Chen ; He Qian</i> | |
| A UNIVERSAL MODEL FOR INTERFACE-TYPE THRESHOLD SWITCHING PHENOMENA BY COMPREHENSIVE STUDY OF VANADIUM OXIDE-BASED SELECTOR | 71 |
| <i>Chih-Yang Lin ; Ying-Chen Chen ; Meiqi Guo ; Chih-Hung Pan ; Fu-Yuan Jin ; Yi-Ting Tseng ; Cheng Chih Hsieh ; Xiaohan Wu ; Min-Chen Chen ; Yao-Feng Chang ; Fei Zhou ; Burt Fowler ; Kuan-Chang Chang ; Tsung-Ming Tsai ; Ting-Chang Chang ; Yonggang Zhao ; Simon M. Sze ; Sanjay Banerjee ; Jack C. Lee</i> | |
| ON THE PHYSICAL MODELING OF RANDOM TELEGRAPH NOISE (RTN) AMPLITUDE IN NANOSCALE MOSFETS: FROM IDEAL TO STATISTICAL DEVICES | 73 |
| <i>Zexuan Zhang ; Shaofeng Guo ; Zhe Zhang ; Runsheng Wang ; Ru Huang</i> | |

| | |
|--|-----|
| A DESIGN METHODOLOGY OF EFFICIENT ON-CHIP WIRELESS POWER TRANSMISSION | 75 |
| <i>Salahuddin Raju ; Clarissa C. Prawoto ; Mansun Chan ; C. Patrick Yue</i> | |
| DEVELOPMENT AND ELECTRICAL INVESTIGATION OF THROUGH GLASS VIA AND THROUGH SI VIA IN 3D INTEGRATION | 77 |
| <i>Geng-Ming Chang ; Shih-Wei Lee ; Ching-Yun Chang ; Kuan-Neng Chen</i> | |
| CONTACT ENGINEERING AND CHANNEL DOPING FOR ROBUST CARBON NANOTUBE NFETS | 79 |
| <i>Jianshi Tang ; Damon Farmer ; Sarunya Bangsaruntip ; Kuan-Chang Chiu ; Bharat Kumar ; Shu-Jen Han</i> | |
| ASYMMETRIC S/D CONTACTS WITH BN TUNNELING BARRIER ON BLACK PHOSPHOROUS FETS | 81 |
| <i>Lingming Yang ; Mengwei Si ; Qing Paduano ; Mike Snure ; Peide Ye</i> | |
| DENSITY FUNCTIONAL THEORY MOLECULAR DYNAMICS SIMULATIONS AND EXPERIMENTAL MEASUREMENTS OF A-HFO₂/A-SIO/SIGE(001) AND A-HFO₂/A-SIO₂/SIGE(001) INTERFACES | 83 |
| <i>E. Chagarov ; K. Sardashti ; I. Kwak ; S. Ueda ; M. Yakimov ; A. C. Kummel</i> | |
| A STEEP SLOPE PHASE-FET BASED ON 2D MOS₂ AND THE ELECTRONIC PHASE TRANSITION IN VO₂ | 85 |
| <i>Benjamin Grisafe ; Nikhil Shukla ; Matthew Jerry ; Suman Datta</i> | |
| ION IMPLANTATION AFTER GERMANIDATION TECHNIQUE FOR LOW THERMAL BUDGET GE CMOS DEVICES: FROM BULK GE TO UTB-GEOI SUBSTRATE | 87 |
| <i>Wen Hsin Chang ; Toshifumi Irisawa ; Hiroyuki Ishii ; Hiroyuki Hattori ; Hiroyuki Ota ; Noriyuki Uchida ; Tatsuro Maeda</i> | |
| SELECTIVE ETCHING OF SILICON IN PREFERENCE TO GERMANIUM AND SI_{0.5}GE_{0.5} | 89 |
| <i>Christopher F. Ahles ; Jong Youn Choi ; Steven Wolf ; Andrew C. Kummel</i> | |
| I/O DEVICE OPTIMIZATION TECHNIQUES TAILED FOR HIGHLY-SCALED FINFET TECHNOLOGY | 91 |
| <i>Ming-Huei Lin ; Chung-An Hu ; Chia-Cheng Chen ; Tien-Shun Chang ; Yun-Ju Sun ; Hou-Yu Chen ; Vincent S. Chang ; Shyh-Horng Yang</i> | |
| STRESSOR DESIGN FOR FINFETS WITH AIR-GAP SPACERS | 93 |
| <i>Darsen D. Lu ; Angada B. Sachid ; Yao-Min Huang ; Yi-Ju Chen ; Chun-Chi Chen ; Min-Cheng Chen ; Chenming Hu</i> | |
| SEMICONDUCTOR-ON-INSULATOR LATERAL BIPOLAR TRANSISTORS FOR HIGH-SPEED LOW-POWER APPLICATIONS | 95 |
| <i>Jeng-Bang Yau ; J. Cai ; T. H. Ning ; K. K. Chan</i> | |
| A NOVEL DESIGN OF P-N STAGGERED FACE-TUNNELING TFET TARGETING FOR LOW POWER AND APPROPRIATE PERFORMANCE APPLICATIONS | 97 |
| <i>E. R. Hsieh ; Y. C. Fan ; K. Y. Chang ; C. H. Liu ; C. H. Chien ; Steve S. Chung</i> | |
| FERROELECTRICITY IN HFO₂ THIN FILMS AS A FUNCTION OF ZR DOPING | 99 |
| <i>Golnaz Karbasian ; Ava Tan ; Ajay Yadav ; Eric Martin Henry Sorensen ; Claudy Rayan Serrao ; Asif Islam Khan ; Korok Chatterjee ; Sangwan Kim ; Chenming Hu ; Sayeef Salahuddin</i> | |
| INTEGRATION OF III-V NANOWIRES FOR THE NEXT RF- AND LOGIC TECHNOLOGY GENERATION | 101 |
| <i>Lars-Erik Wernersson</i> | |
| DEVICE-ARCHITECTURE CO-DESIGN FOR HYPERDIMENSIONAL COMPUTING WITH 3D VERTICAL RESISTIVE SWITCHING RANDOM ACCESS MEMORY (3D VRAM) | 103 |
| <i>Haitong Li ; Tony F. Wu ; Subhasish Mitra ; H. -S. Philip Wong</i> | |
| 1x- TO 2x-NM MTJ SWITCHING AT SUB-3 NS PULSES WITH COMPATIBLE CURRENT IN SUB-20 NM CMOS FOR HIGH PERFORMANCE EMBEDDED STT-MRAM | 105 |
| <i>Daisuke Saida ; Saori Kashiwada ; Megumi Yakabe ; Tadaomi Daibou ; Keiko Abe ; Hiroki Noguchi ; Junichi Ito ; Shinobu Fujita ; Miyoshi Fukumoto ; Shinji Miwa ; Yoshishige Suzuki</i> | |
| BACK-SIDE INTEGRATION OF HYBRID III-V ON SILICON DBR LASERS | 107 |
| <i>J. Durel ; B. Ben Bakir ; C. Jany ; S. Cremer ; K. Hassan ; B. Szelag ; T. Bria ; V. Larrey ; L. Sanchez ; P. Brianceau ; J. -A Dallery ; R. Guiavarch ; T. Card ; R. Thibon ; J. -E. Broquin ; F. Bauf</i> | |
| NOVEL TFET CIRCUITS FOR HIGH-PERFORMANCE ENERGY-EFFICIENT HETEROGENEOUS MOSFET/TFET LOGIC | 109 |
| <i>Daniel H. Morris ; Uygar E. Avci ; Kaushik Vaidyanathan ; Huichu Liu ; Tanay Karnik ; Ian A. Young</i> | |
| EXPLORATION AND EVALUATION OF TCAM WITH HYBRID TUNNELING FET AND FINFET DEVICES FOR ULTRA-LOW-VOLTAGE APPLICATIONS | 111 |
| <i>Meng-Hsuan Tu ; Yin-Nien Chen ; Pin Su ; Ching-Te Chuang</i> | |

| | |
|---|-----|
| DENSE N OVER CMOS 6T SRAM CELLS USING 3D SEQUENTIAL INTEGRATION | 113 |
| <i>C-M. V. ; C. Fenouillet-Beranger ; M. Brocard ; O. Billoint ; G. Cibrario ; L. Brunet ; X. Garros ; C. Leroux ; M. Casse ; A. Laurent ; A. Toffoli ; G. Romano ; R. Kies ; R. Gassilloud ; N. Rambal ; V. Lapras ; M-P. Samson ; C. Tallaron ; C. Tabone ; B. Previtali ; D. Barge ; A. Ayres ; L. Pasini ; P. Besombes ; F. Andrieu ; P. Batude ; T. Skotnicki ; M. Vinet</i> | |
| AN INVESTIGATION OF PROGRAM DISTURB CHARACTERISTICS AND DATA PATTERN EFFECT IN 128G 3D NAND FLASH MEMORIES | 115 |
| <i>Yu-Hung Yeh ; Sheng-Hung Shih ; Jen-Chien Fu ; Chrong-Jung Lin ; Ya-Chin King</i> | |
| HARDWARE IMPLEMENTATION OF PHYSICALLY UNCLONABLE FUNCTION (PUF) IN PERPENDICULAR STT MRAM | 117 |
| <i>D. Y. Wang ; Y. C. Hsin ; K. Y. Lee ; G. L. Chen ; S. Y. Yang ; H. H. Lee ; Y. J. Chang ; I. J. Wang ; Y. C. Kuo ; Y. S. Chen ; P. H. Wang ; C. I. Wu ; D. D. Tang</i> | |
| A MAGNETIC SHIFT REGISTER WITH PERIODIC POTENTIAL ENERGY MODULATION | 119 |
| <i>T. Kondo ; H. Morise ; T. Shimada ; M. Quinsat ; M. Kado ; Y. Ootera ; S. Nakamura</i> | |
| Author Index | |