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TECHNICAL PROGRAM

Opening Remarks

Monday, May 29, 9:20-9:40

M. Mori, *Hitachi, Ltd.*

Plenary 1

Monday, May 29, 9:40-10:50

Chair: M. Mori, *Hitachi, Ltd.*

Co-chair: J. Shen, *Illinois Institute of Technology*

PL1-1 **Power Electronics as the Enabling Technology for Sustainable Energy in the Smart City**

J. Driesen

Katholieke Universiteit Leuven / EnergyVille, Belgium

PL1-2 **The Future Vision of Industrial Robot**

K. Yasuda

Yaskawa Electric Corp., Japan

Plenary 2

Monday, May 29, 11:10-12:20

Chair: I. Omura, *Kyushu Institute of Technology*

Co-chair: K. Sheng, *Zhejiang University*

PL2-1 **Application Opportunities and Expectations for Wide Bandgap Power Devices in Power Supply**

Z. Zhao, C. Cai and T. Wang

Delta Electronics (Shanghai) Co., Ltd., China

PL2-2 **GaN Power IC Technology: Past, Present, and Future**

D. Kinzer

Navitas Semiconductor, USA

Session 1: Power ICs: Isolated and High-Speed Drivers

Monday, May 29, 13:50-15:30

Chair: O. Trescases, *University of Toronto*

Co-chair: H. Fujii, *Renesas Electronics Corporation*

1-1 **Challenges in Reliably Driving GaN Devices (Invited)**

P.L. Brohlin

Texas Instruments Incorporated, USA

1-2 **Power Electronics 2.0: IoT-Connected and AI-Controlled Power Electronics Operating Optimally for Each User (Invited)**

M. Takamiya[1], K. Miyazaki[1], H. Obara[2,3], T. Sai[1], K. Wada[2] and T. Sakurai[1]

[1]*University of Tokyo, Japan,* [2]*Tokyo Metropolitan University, Japan and* [3] *Yokohama National University, Japan*

1-3 **A 1 W Power Consumption GaN-Based Isolated Gate Driver for a 1.0 MHz GaN Power System**
S. Che, S. Nagai, N. Negoro, Y. Kawai, O. Tabata, S. Enomoto, Y. Anda and T. Hatsuda
Panasonic Corporation, Japan

1-4 **High Speed Digital Optical Signal Transfer for Power Transistor Gate Driver Applications**
D. Colin[1] and N. Rouger[2]
[1]*Univ. Grenoble Alpes, France and* [2]*Université de Toulouse, France*

Session 2: SiC Diodes

Monday, May 29, 15:45-17:25

Chair: P. Godignon, *CNM Barcelona*
Co-chair: K.-Y. Lee, *National Taiwan University*

2-1 **6.5 kV Schottky-Barrier-Diode-Embedded SiC-MOSFET for Compact Full-Unipolar Module**
K. Kawahara, S. Hino, K. Sadamatsu, Y. Nakao, Y. Yamashiro, Y. Yamamoto, T. Iwamatsu, S. Nakata, S. Tomohisa and S. Yamakawa
Mitsubishi Electric Corporation, Japan

2-2 **High Efficiency High Reliability SiC MOSFET with Monolithically Integrated Schottky Rectifier**
F.-J. Hsu, C.-T. Yen, C.-C. Hung, H.-T. Hung, C.-Y. Lee, L.-S. Lee, Y.-F. Huang, T.-L. Chen and P.-J. Chuang
Hestia Power Incorporated, Taiwan

2-3 **SiC MOSFET with Built-in SBD for Reduction of Reverse Recovery Charge and Switching Loss in 10-kV Applications**
H. Jiang[1,2], J. Wei[3], X. Dai[1,2], C. Zheng[1,2], M. Ke[1], X. Deng[4], Y. Sharma[1], I. Deviny[1] and P. Mawby[5]
[1]*Dynex Semiconductor Ltd., UK,* [2]*Zhuzhou CRRC Times Electric Co., Ltd., China,* [3]*Hong Kong University of Science and Technology, Hong Kong,* [4]*University of Electronic Science and Technology of China, China and* [5]*University of Warwick, UK*

2-4 **Experimental Investigation of SiC 6.5kV JBS Diodes Safe Operating Area**
A. Mihaila[1], E. Bianda[1], L. Knoll[1], U. Vemulapati[1], L. Kranz[1], G. Alfieri[1], V. Soler[2], P. Godignon[2], C. Papadopoulos[1] and M. Rahimo[1]
[1]*ABB Switzerland Ltd., Switzerland and* [2]*Consejo Superior de Investigaciones Científicas, Spain*

Session 3: IGBTs

Tuesday, May 30, 8:45-10:25

Chair: T. Minato, *Mitsubishi Electric Corporation*

Co-chair: T. Laska, *Infineon Technologies*

3-1 **A Novel Hybrid Power Module with Dual Side-Gate HiGT and SiC-SBD**

Y. Takeuchi, T. Miyoshi, T. Furukawa, M. Shiraishi and M. Mori

Hitachi, Ltd., Japan

3-2 **Conductivity Modulation in the Channel Inversion Layer of Very Narrow Mesa IGBT**

M. Tanaka[1] and A. Nakagawa[2]

[1]*Nihon Synopsys G.K., Japan and* [2]*Nakagawa Consulting Office, LLC., Japan*

3-3 **Hole Path Concept for Low Switching Loss and Low EMI Noise with High IE-Effect**

M. Sawada[1], Y. Sakurai[1], K. Ohi[1], Y. Ikura[1], Y. Onozawa[1], T. Yamazaki[1] and Y. Nabetani[2]

[1]*Fuji Electric Co., Ltd, Japan and* [2]*University of Yamanashi, Japan*

3-4 **A New Sub-Micron Trench Cell Concept in Ultrathin Wafer Technology for Next Generation 1200 V IGBTs**

C. Jaeger[1], A. Philippou[1], A. Vellei[2], J.G. Laven[1] and A. Härtl[1]

[1]*Infineon Technologies AG, Germany and* [2]*Infineon Technologies Austria AG, Austria*

Session 4: Low Voltage Devices & Power IC Device Technology

Tuesday, May 30, 10:40-12:20

Chair: P. Rutter, *Nexperia*

Co-chair: N. Fujishima, *Fuji Electric Co., Ltd.*

4-1 **A 90nm Bulk BiCDMOS Platform Technology with 15-80V LD-MOSFETs for Automotive Applications**

H. Fujii[1], S. Tokumitsu[1], T. Mori[1], T. Yamashita[2], T. Maruyama[2], T. Maruyama[2], Y. Maruyama[1], S. Nishimoto[1], H. Arie[1], S. Kubo[1] and T. Ipposhi[1]

[1]*Renesas Semiconductor Manufacturing Co., Ltd., Japan and* [2]*Renesas Electronics Corporation, Japan*

4-2 **High/Low-Side Hybrid Output Transistor with High Thermal-SOA**

S. Wada[1], K. Ikegaya[2], T. Oshima[2] and Y. Kobayashi[2]

[1]*Hitachi, Ltd., Japan and* [2]*Hitachi Automotive Systems, Japan*

4-3 **Trench Schottky Rectifiers with Non-Uniform Trench Depths**
M. Mudholkar, M.T. Quddus, Y. Kalderon, M. Thomason and A. Salih
ON Semiconductor, USA

4-4 **A Composite Structure Named Self-Adjusted Conductivity Modulation SOI-LIGBT with Low On-State Voltage**
W. Sun[1], J. Zhu[1], Z. Yang[1], F. Bian[1], X. Tong[1], Y. Tian[1], Y. Yi[1], Y. Gu[2], S. Zhang[2] and W. Su[2]
[1]*Southeast University, China and* [2]*CSMC Technologies Corporation, China*

Session 5: GaN Device: Technology and Dynamic Effects

Tuesday, May 30, 13:50-15:30

Chair: O. Häberlen, *Infineon Technologies*
Co-chair: Y. Uemoto, *Panasonic Corporation*

5-1 **High-Performance Fully-Recessed Enhancement-Mode GaN MIS-FETs with Crystalline Oxide Interlayer**
M. Hua[1,2], Z. Zhang[1], Q. Qian[1], J. Wei[1], Q. Bao[1], G. Tang[1] and K.J. Chen[1,2]
[1]*Hong Kong University of Science and Technology, Hong Kong and* [2]*HKUST Shenzhen Research Institute, China*

5-2 **Kilovolt GaN MOSHEMT on Silicon Substrate with Breakdown Electric Field Close to the Theoretical Limit**
M. Tao[1], M. Wang[1], C.P. Wen[1], J. Wang[1], Y. Hao[1], W. Wu[1], K. Cheng[2] and B. Shen[1]
[1]*Peking University, China and* [2]*Enkris Semiconductor, China*

5-3 **Negative Dynamic Ron in AlGaN/GaN Power Devices**
P. Moens[1], M.J. Uren[2], A. Banerjee[1], M. Meneghini[3], B. Padmanabhan[4], W. Jeon[4], S. Karboyan[2], M. Kuball[2], G. Meneghesso[3], E. Zanoni[3] and M. Tack[1]
[1]*ON Semiconductor, Belgium,* [2]*University of Bristol, UK,* [3]*Università degli Studi di Padova, Italy and* [4]*ON Semiconductor, USA*

5-4 **Buffer Trapping-Induced R_{ON} Degradation in GaN-on-Si Power Transistors: Role of Electron Injection from Si Substrate**
S. Yang[1], C. Zhou[2], S. Han[1], K. Sheng[1] and K.J. Chen[2]
[1]*Zhejiang University, China and* [2]*Hong Kong University of Science and Technology, Hong Kong*

Poster Session 1: High Voltage

Tuesday, May 30, 15:45-17:45

Chair: T. Yamazaki, *Fuji Electric Co., Ltd.*

HV-P1 **High-Voltage Diode Robustness During Short-Circuit Type III**
J. Fuhrmann, D. Hammes and H.-G. Eckel
Universität Rostock, Germany

HV-P2 **A New 1200 V-Class Edge Termination Structure with Trench Double Field Plates for High dV/dt Performance**
W. Yang[1], H. Feng[1], Y. Liu[1], X. Fang[1], Y. Onozawa[2], H. Tanaka[2], K. Mitsuzuka[2] and J.K.O. Sin[1]
[1]*Hong Kong University of Science and Technology, Hong Kong and* [2]*Fuji Electric Co., Ltd., Japan*

HV-P3 **A Novel Injection Enhanced Floating Emitter (IEFE) IGBT Structure Improving the Ruggedness Against Short-Circuit and Thermal Destruction**
R. Bhojani[1], J. Lutz[1], R. Baburske[2], H.-J. Schulze[2] and F.-J. Niedernostheide[2]
[1]*Technische Universität Chemnitz, Germany and* [2]*Infineon Technologies AG, Germany*

HV-P4 **Advanced RFC Diode Utilizing a Novel Vertical Structure for Softness and High Dynamic Ruggedness**
K. Nakamura and K. Shimizu
Mitsubishi Electric Corporation, Japan

HV-P5 **Novel Emitter Controlled Diode with Copper Metallization in Ultrathin Wafer Technology: Setting a Performance Benchmark**
F.J. Santos Rodriguez[1], D. Schloegl[1], F. Hille[2], P.C. Brandt[2], M. Pfaffenlehner[2], A.R. Stegner[2] and A. Härtl[2]
[1]*Infineon Technologies Austria AG, Austria and* [2]*Infineon Technologies AG, Germany*

HV-P6 **Study of the Electrostatic Potential of the Floating-P Region During the Turn-on Period of IGBT**
Y. Ikura[1], Y. Onozawa[1] and A. Nakagawa[2]
[1]*Fuji Electric Co., Ltd., Japan and* [2]*Nakagawa Consulting Office, LLC., Japan*

HV-P7 **A Snapback-Free RC-IGBT with Alternating N/P Buffers**
G. Deng, X. Luo, K. Zhou, Q. He, X. Ruan, Q. Liu, T. Sun and B. Zhang
University of Electronic Science and Technology of China, China

HV-P8 **RFC Diode with High Avalanche Stability and UIS Capability**
F. Masuoka, K. Tanaka, T. Kachi, Y. Yoshiura and K. Shimizu
Mitsubishi Electric Corporation, Japan

HV-P9 **Direct Photo Emission Monitoring for Analysis of IGBT Destruction Mechanism Using Streak Camera**

T. Matsudai[1], K. Endo[1], T. Ogura[1], T. Matsumoto[2], K. Uchiyama[2], F. Niikura[2] and K. Koshikawa
[1]*Toshiba Corporation, Japan and* [2]*Hamamatsu Photonics K.K., Japan*

HV-P10 **Transient Overvoltage Induced Failure of MOS-Controlled Thyristor under Ultra-High di/dt Condition**

C. Liu, W. Chen, H. Tao, Y. Shi, X. Tang, W. Gao, Q. Zhou, Z. Li and B. Zhang
University of Electronic Science and Technology of China, China

HV-P11 **IGBT Field-Stop Design for Good Short Circuit Ruggedness and a Better Trade-Off with Respect to Static and Dynamic Switching Characteristics**

H.P. Felsl, F.-J. Niedernostheide and H.-J. Schulze
Infineon Technologies AG, Germany

HV-P12 **A Novel 1700V RET-IGBT (Recessed Emitter Trench IGBT) Shows Record Low $V_{CE(ON)}$, Enhanced Current Handling Capability and Short Circuit Robustness**

I. Deviny[1], H. Luo[2,3], Q. Xiao[2,3], Y. Yao[2,3], C. Zhu[1], L.-K. Ngwendson[1], H. Xiao[2,3], X. Dai[1,2,3] and G. Liu[2,3]
[1]*Dynex Semiconductor Ltd., UK,* [2]*State key Laboratory of Advanced Power Semiconductor Devices, China and* [3]*Zhuzhou CRRC Times Electric Co., Ltd., China*

HV-P13 **TCAD Analysis of Short-Circuit Oscillations in IGBTs**

P. Diaz Reigosa[1], F. Iannuzzo[1] and M. Rahimo[2]
[1]*Aalborg University, Denmark and* [2]*ABB Switzerland Ltd., Switzerland*

HV-P14 **Investigations of Inhomogeneous Reverse Recovery Behavior of the Body Diode in Superjunction MOSFET**

Z. Yang[1], J. Zhu[1], X. Tong[1], W. Sun[1], F. Bian[1], Y. Tian[1], Y. Zhu[2], P. Ye[2], Z. Li[2] and B. Hou[3]
[1]*Southeast University, China,* [2]*WUXI NCE Power CO., LTD, China and* [3]*No.5 Electronics Research Institute of the Ministry of Industry and Information Technology, China*

HV-P15 **Physics of Current Limited Failures During Avalanche for 600V Fast Recovery Diodes**

L. Maresca, M. Riccio, P. Mirone, G. Romano, G. Breglio and A. Irace
Università degli Studi di Napoli Federico II, Italy

HV-P16 **Free-Carrier Absorption Experiments for the Investigation of the Physical Device Properties in IGBTs with Hydrogen-Related Donors**
A. Korzenietz[1], G. Wachutka[1], F. Hille[2], C. Sandow[2] and F.-J. Niedernostheide[2]
[1]*Technische Universität München, Germany and* [2]*Infineon Technologies AG, Germany*

HV-P17 **Formulation of Single Event Burnout Failure Rate for High Voltage Devices in Satellite Electrical Power System**
Y. Shiba, E. Dashdondog, M. Sudo and I. Omura
Kyushu Institute of Technology, Japan

Poster Session 1: Power ICs

Tuesday, May 30, 15:45-17:45

Chair: T. Yamazaki, *Fuji Electric Co., Ltd.*

ICD-P1 **A Circuit Simulation Flow for Substrate Minority Carrier Injection in Smart Power ICs**
M. Kollmitzer[1], M. Olbrich[2] and E. Barke[2]
[1]*Infineon Technologies Austria AG, Austria and* [2]*Leibniz University Hannover, Germany*

ICD-P2 **A New Downsized HVIC with High ESD Tolerance**
T. Tanaka, M. Yamaji, A. Jonishi, H. Ohashi and H. Sumida
Fuji Electric Co., Ltd., Japan

ICD-P3 **Distributed Electro-Thermal Model Based on Fast and Scalable Algorithm for GaN Power Devices and Circuit Simulations**
V. Sodan[1,2], S. Stoffels[1], H. Oprins[1], M. Baelmans[2], S. Decoutere[1] and I. De Wolf[1,2]
[1]*IMEC, Belgium and* [2]*Katholieke Universiteit Leuven, Belgium*

ICD-P4 **Investigation of a Latch-Up Immune Silicon Controlled Rectifier for Robust ESD Application**
Z. Qi[1], M. Qiao[1], X. Zhou[1], W. Yang[1], D. Fang[1,2], S. Cheng[1,2], S. Zhang[2], Z. Li[1] and B. Zhang[1]
[1]*University of Electronic Science and Technology of China, China and* [2]*CSMC Technologies Co., Ltd., China*

ICD-P5 **Riddle and Bond Silicon on Insulator (RABSOI)**
R. Spetik, F. Kudrna and L. Valek
ON Semiconductor s.r.o Czech Republic, Czech Republic

Poster Session 1: GaN Power

Tuesday, May 30, 15:45-17:45

Chair: T. Yamazaki, *Fuji Electric Co., Ltd.*

GaN-P1 **Design Considerations of Vertical GaN Nanowire Schottky Barrier Diodes**
G. Sabui[1], V.Z. Zubialevich[2], M. White[2], P. Pampili[2], P.J. Parbrook[2], M. McLaren[3], M. Arredondo-Arechavala[3] and Z.J. Shen[1]
[1]*Illinois Institute of Technology, USA,* [2]*University College Cork, Ireland and* [3]*Queen's University Belfast, Ireland*

GaN-P2 **Highly Reliable GaN MOS-HFET with High Short-Circuit Capability**
Y. Eum, K. Oyama, N. Otake and S. Hoshi
Denso Corporation, Japan

GaN-P3 **Relation between UIS Withstanding Capability and Gate Leakage Currents for High Voltage GaN-HEMTs**
T. Naka and W. Saito
Toshiba Corporation, Japan

GaN-P4 **An AlGaN/GaN Current Regulating Diode**
A. Zhang, Q. Zhou, W. Chen, Y. Shi, Z. Li and B. Zhang
University of Electronic Science and Technology of China, China

GaN-P5 **A High-Performance GaN E-Mode Reverse Blocking MISHEMT with MIS Field Effect Drain for Bidirectional Switch**
Y. Shi, W. Chen, C. Liu, G. Hu, J. Liu, X. Cui, H. Tao, J. Zhang, Y. Shi, A. Zhang, Z. Li, Q. Zhou and B. Zhang
University of Electronic Science and Technology of China, China

GaN-P6 **Experimental Study of the Short-Circuit Performance for a 600V Normally-Off p-Gate GaN HEMT**
T. Oeder[1,2], A. Castellazzi[3] and M. Pfost[4]
[1]*Robert Bosch Center for Power Electronics, Germany,* [2]*Reutlingen University, Germany,* [3]*University of Nottingham, UK and* [4]*Technische Universität Dortmund, Germany*

GaN-P7 **PEALD Induced Interface Engineering of AlNO/AlGaN/GaN MIS Diode with Alternate Insertion of AlN in Al_2O_3**
Q. Wang[1,2], X. Cheng[1], L. Zheng[1,2], L. Shen[1,2], J. Li[1,2], D. Zhang[1,2], R. Qian[1,2] and Y. Yu[1]
[1]*Chinese Academy of Sciences, China and* [2]*University of Chinese Academy of Sciences, China*

GaN-P8 **Design and Control of Interface Reaction between Al-Based Dielectrics and AlGaN Layer for Hysteresis-Free AlGaN/GaN MOS-HFETs**
K. Watanabe[1], M. Nozaki[1], T. Yamada[1], S. Nakazawa[2], Y. Anda[2], M. Ishida[2], T. Ueda[2], A. Yoshigoe[3], T. Hosoi[1], T. Shimura[1] and H. Watanabe[1]
[1]*Osaka University, Japan,* [2]*Panasonic Corporation, Japan and* [3]*Japan Atomic Energy Agency, Japan*

GaN-P9 **Switching Characteristics of Monolithically Integrated Si-GaN Cascoded Rectifiers**
J. Ren, C. Liu, C.W. Tang, K.M. Lau and J.K.O. Sin
Hong Kong University of Science and Technology, Hong Kong

GaN-P10 **On the Vertical Leakage of GaN-on-Si Lateral Transistors and the Effect of Emission and Trap-to-Trap-Tunneling Through the AlN/Si Barrier**
G. Longobardi[1], S. Yang[1], D. Pagnano[1], G. Camuso[1], F. Udrea[1], J. Sun[2], R. Garg[2], M. Imam[2] and A. Charles[2]
[1]*University of Cambridge, UK and* [2]*Infineon Technologies Americas Corp, USA*

GaN-P11 **Investigation of Current Collapse Mechanism of LPCVD Si_3N_4 Passivated AlGaN/GaN HEMTs by Fast Soft-Switched Current-DLTS and CC-DLTFS**
X. Wang[1], X. Kang[1], J. Zhang[2], K. Wei[1], S. Huang[1] and X. Liu[1]
[1]*Chinese Academy of Sciences, China and* [2]*University of Electronic Science and Technology of China, China*

GaN-P12 **Impact of Substrate Termination on Dynamic Performance of GaN-on-Si Lateral Power Devices**
G. Tang[1,2], J. Wei[1,2], Z. Zhang[1], X. Tang[1,2], M. Hua[1,2], H. Wang[1] and K.J. Chen[1,2]
[1]*Hong Kong University of Science and Technology, Hong Kong and* [2]*HKUST Shenzhen Research Institute, China*

Session 6: SiC MOSFETs

Wednesday, May 31, 9:00-11:05

Chair: T. Kuroiwa, *Mitsubishi Electric Corporation*
Co-chair: A. Zhang, *Xi'an Jiaotong University*

6-1 **Performance and Ruggedness of 1200V SiC - Trench - MOSFET**
D. Peters[1], R. Siemieniec[2], T. Aichinger[2], T. Basler[1], R. Esteve[2], W. Bergner[2] and D. Kueck[2]
[1]*Infineon Technologies AG, Germany and* [2]*Infineon Technologies Austria AG, Austria*

6-2 **Robust 3.3kV Silicon Carbide MOSFETs with Surge and Short Circuit Capability**
L. Knoll, A. Mihaila, F. Bauer, V. Sundaramoorthy, E. Bianda, R. Minamisawa, L. Kranz, M. Bellini, U. Vemulapati, H. Bartolf, S. Kicin, S. Skibin, C. Papadopoulos and M. Rahimo
ABB Switzerland Ltd., Switzerland

6-3 **Reliability-Aware Design of Metal/High-*K* Gate Stack for High-Performance SiC Power MOSFET**
T. Hosoi[1], S. Azumo[2], Y. Kashiwagi[2], S. Hosaka[2], K. Yamamoto[3], M. Aketa[3], H. Asahara[3], T. Nakamura[3], T. Kimoto[4], T. Shimura[1] and H. Watanabe[1]
[1]*Osaka University, Japan,* [2]*Tokyo Electron Limited, Japan,* [3]*ROHM Co., Ltd., Japan and* [4]*Kyoto University, Japan*

6-4 **Reliability Assessment of a Large Population of 3.3 kV, 45 A 4H-SiC MOSFETs**
E. Van Brunt, D.J. Lichtenwalner, R. Leonard, A. Burk, S. Sabri, B. Hull, S. Allen and J.W. Palmour
Wolfspeed, USA

6-5 **Design and Fabrication of 3.3kV SiC MOSFETs for Industrial Applications (Late News)**
X. Huang, L. Fursin, A. Bhalla, W. Simon and J.C. Dries
United Silicon Carbide Inc., USA

Session 7: Packaging: Power Modules

Wednesday, May 31, 11:20-12:35

Chair: S. Nagai, *Panasonic Corporation*
Co-chair: A. Castellazzi, *Nottingham University*

7-1 **High Efficient Approach to Utilize SiC MOSFET Potential in Power Modules**
I. Kasko, S.E. Berberich, M. Gross, P. Beckedahl and S. Buetow
Semikron Elektronik GmbH & Co. KG, Germany

7-2 **High Power Density Side-Gate HiGT Modules with Sintered Cu Having Superior High-Temperature Reliability to Sintered Ag**
T. Furukawa[1], M. Shiraishi[1], Y. Yasuda[1], A. Konno[1], M. Mori[1], T. Morita[2], S. Watanabe[2], T. Arai[2], M. Nakamura[2] and D. Kawase[2]
[1]*Hitachi, Ltd., Japan and* [2]*Hitachi Power Semiconductor Device, Ltd., Japan*

7-3 **New Power Module Integrating Output Current Measurement Function**
S. Tabata[1], K. Hasegawa[1], M. Tsukuda[1,2] and I. Omura[1]
[1]*Kyushu Institute of Technology, Japan and* [2]*Green Electronics Research Institute, Japan*

Session 8: Power ICs: Automotive and Industrial Applications

Wednesday, May 31, 14:05-14:55

Chair: J. Sakano, *Hitachi, Ltd.*

Co-chair: M. Swanenberg, *NXP Semiconductors*

8-1 **Fully Integrated High Voltage High Current Gate Driver for MOSFET-Inverters**

B. Vogler, R. Herzer, M. Dienstbier and S. Buetow

Semikron Elektronik GmbH & Co. KG, Germany

8-2 **An IGBT Gate Driver IC with Collector Current Sensing**

J. Chen[1], W. Zhang[1], A. Shorten[1], J. Yu[1], W.T. Ng[1], M. Sasaki[2], T. Kawashima[2] and H. Nishio[2]

[1]*University of Toronto, Canada and* [2]*Fuji Electric Co., Ltd., Japan*

Poster Session 2: Low Voltage & Power IC Device

Wednesday, May 31, 15:10-17:10

Chair: T. Yamazaki, *Fuji Electric Co., Ltd.*

LVT-P1 **Novel LDMOS with Assisted Deplete-Substrate Layer Consist of Super Junction under the Drain**

S. Yuan, B. Duan, H. Cai, Z. Cao and Y. Yang

Xidian University, China

LVT-P2 **Novel Superjunction LDMOS with Multi-Floating Buried Layers**

Z. Cao, B. Duan, S. Yuan, H. Guo, J. Lv, T. Shi and Y. Yang

Xidian University, China

LVT-P3 **180nm HVIC Technology for Digital AC/DC Power Conversion**

D. Disney, W.-C. Lin, X. Liu, S. Pandey and J. Kim

GLOBALFOUNDRIES Singapore Pte. Ltd., Singapore

LVT-P4 **U-Shaped Channel SOI-LIGBT with Dual Trenches to Improve the Trade-Off Between Saturation Voltage and Turn-Off Loss**

L. Zhang[1], J. Zhu[1], W. Sun[1], M. Zhao[1], J. Chen[1], X. Huang[1], D. Ding[1], Y. Gu[2], S. Zhang[2] and B. Hou[3]

[1]*Southeast University, China,* [2]*CSMC Technologies Corporation, China and* [3]*No.5 Electronics Research Institute of the Ministry of Industry and Information Technology, China*

LVT-P5 **Best-in-Class LDMOS with Ultra-Shallow Trench Isolation and P-Buried Layer from 18V to 40V in 0.18µm BCD Technology**

F. Jin[1,2], D. Liu[1], J. Xing[1], X. Yang[1], J. Yang[1], W. Qian[1], W. Yue[1], P. Wang[2], M. Qiao[3] and B. Zhang[3]

[1]*Shanghai Huahong Grace Semiconductor Manufacturing Corporation, China,* [2]*Fudan University, China and* [3]*University of Electronic Science and Technology of China, China*

LVT-P6 **A Novel 80V HS-DMOS with Gradual-RESURF Profile to Reduce Ron_sp for High-Side Operation**

T.-Y. Huang[1], C.-H. Huang[1,2], C.-F. Huang[2], J.-M. Liu[1], K.-H. Lo[1,2], C.-H. Cheng[2], J.-Y. Jiang[2], T.-Y. Tsai[1], T.-W. Liao[1] and J. Gong[3]

[1]*Richtek Technology Corporation, Taiwan,* [2]*National Tsing Hua University, Taiwan and* [3]*Tunghai University, Taiwan*

LVT-P7 **Dielectric RESURF as an Alternative to Shield RESURF for an Improved and Easy-to-Manufacture Low Voltage Trench MOSFETs**

Z. Hossain[1], G. Sabui[2] and J.Z. Shen[2]

[1]*ON Semiconductor, USA and* [2]*Illinois Institute of Technology, USA*

LVT-P8 **Low On-Resistance High Voltage Thin Layer SOI LDMOS Transistors with Stepped Field Plates**

K. Hara[1], T. Kakegawa[1], S. Wada[1], T. Utsumi[2] and T. Oda[2]

[1]*Hitachi, Ltd., Japan and* [2]*Hitachi Power Semiconductor Device, Ltd., Japan*

LVT-P9 **A Novel High-Voltage LDMOS with Shielding-Contact Structure for HCI SOA Enhancement**

H.-L. Liu, Z.-W. Jhou, S.-T. Huang, S.-W. Lin, K.-F. Lin, C.-T. Lee and C.-C. Wang

United Microelectronics Corporation, Taiwan

LVT-P10 **A Snapback-Free Shorted-Anode SOI LIGBT with Multi-Segment Anode**

K. Zhou, T. Sun, Q. Liu, B. Zhang, Z. Li and X. Luo

University of Electronic Science and Technology of China, China

LVT-P11 **Edge Termination Design of a 700-V Triple RESURF LDMOS with N-Type Top Layer**

M. Qiao[1], Z. Wang[1], H. Wang[2], F. Jin[2], Z. Li[1] and B. Zhang[1]

[1]*University of Electronic Science and Technology of China, China and* [2]*Shanghai Huahong Grace Semiconductor Manufacturing Corporation, China*

LVT-P12 **A Novel 700V Deep Trench Isolated Double RESURF LDMOS with P-Sink Layer**
S. Cheng[1,2], D. Fang[1,2], M. Qiao[1], S. Zhang[2], G. Zhang[2], Y. Gu[2], Y. He[1], X. Zhou[1], Z. Qi[1], Z. Li[1] and B. Zhang[1]
[1]*University of Electronic Science and Technology of China, China and* [2]*CSMC Technologies Corporation, China*

LVT-P13 **Simple and Efficient Approach to Improve Hot Carrier Immunity of a p-LDMOSFET**
A. Sakai[1], K. Eikyu[1], H. Fujii[2], T. Mori[2], Y. Akiyama[1] and Y. Yamaguchi[1]
[1]*Renesas Electronics Corporation, Japan and* [2]*Renesas Semiconductor Manufacturing Co., Ltd., Japan*

LVT-P14 **High-Speed Power MOSFET with Low Reverse Transfer Capacitance Using a Trench/Planar Gate Architecture**
J. Wei[1], Y. Wang[1], M. Zhang[2], H. Jiang[3,4] and K.J. Chen[1]
[1]*Hong Kong University of Science and Technology, Hong Kong,* [2]*Hong Kong Polytechnic University, Hong Kong,* [3]*Dynex Semiconductor Ltd., UK and* [4]*Zhuzhou CRRC Times Electric Co., Ltd., China*

LVT-P15 **A Novel Contact Field Plate Application in Drain-Extended-MOSFET Transistors**
L. Wei, C. Chao, U. Singh, R. Jain, L.L. Goh and P.R. Verma
GLOBALFOUNDRIES Singapore Pte. Ltd., Singapore

LVT-P16 **Increasing Breakdown Voltage of p-Channel LDMOS in BCD Technology with Novel Backside Process**
C. Schmidt and G. Spitzlsperger
LFoundry S.r.l., Germany

Poster Session 2: SiC and Other Material Devices

Wednesday, May 31, 15:10-17:10

Chair: T. Yamazaki, *Fuji Electric Co., Ltd.*

SiC-P1 **Low on-Resistance and Fast Switching of 13-kV SiC MOSFETs with Optimized Junction Field-Effect Transistor Region**
H. Kitai[1], Y. Hozumi[1], H. Shiomi[1], K. Fukuda[1] and M. Furumai[2]
[1]*National Institute of Advanced Industrial Science and Technology, Japan and* [2]*Sumitomo Electric Industries, Ltd., Japan*

SiC-P2 **Suppression of Charge Accumulation on Termination Area of 4H-SiC Power Devices**
H. Matsushima, R. Yamada and A. Shima
Hitachi, Ltd., Japan

SiC-P3 **Design of Self-Aligned 3.3-kV DMOSFET Using Tilted Ion Implantation**
T. Morikawa, T. Ishigaki and A. Shima
Hitachi, Ltd., Japan

SiC-P4 **A New SiC Diode with Significantly Reduced Threshold Voltage**
M. Draghici[1], R. Rupp[2], R. Elpelt[2], R. Gerlach[2] and R. Schörner[2]
[1]*Infineon Technologies Austria AG, Austria and* [2]*Infineon Technologies AG, Germany*

SiC-P5 **Interfacial Damage Extraction Method for SiC Power MOSFETs Based on C-V Characteristics**
J. Wei[1], S. Liu[1], R. Ye[1], X. Chen[1], H. Song[1], W. Sun[1], W. Su[2], S. Ma[2], Y. Liu[2], F. Lin[2] and B. Hou[3]
[1]*Southeast University, China,* [2]*CSMC Technologies Corporation, China and* [3]*Science and Technology on Reliability Physics and Application Technology of Electronic Component Laboratory, China*

SiC-P6 **Experimental and Numerical Demonstration and Optimized Methods for SiC Trench MOSFET Short-Circuit Capability**
M. Namai, J. An, H. Yano and N. Iwamuro
University of Tsukuba, Japan

SiC-P7 **Power Cycling Methods for SiC MOSFETs**
C. Herold, J. Sun, P. Seidel, L. Tinschert and J. Lutz
Technische Universität Chemnitz, Germany

SiC-P8 **Highly Rugged 1200 V 80 mΩ 4-H SiC Power MOSFET**
I.-H. Ji, A. Gendron-Hansen, M. Lee, E. Maxwell, B. Odekirk, D. Sdrulla, C. Hong, A.S. Kashyap and F. Faheem
Microsemi Corporation, USA

SiC-P9 **A Comparative Study of Channel Designs for SiC MOSFETs: Accumulation Mode Channel Vs. Inversion Mode Channel**
W. Sung[1], K. Han[2] and B.J. Baliga[2]
[1]*State University of New York Polytechnic Institute, USA and* [2]*North Carolina State University, USA*

SiC-P10 **Characterization of X-Ray Radiation Hardness of Diamond Schottky Barrier Diode and Metal-Semiconductor Field-Effect Transistor**
H. Umezawa[1], S. Ohmagari[1], Y. Mokuno[1] and J.H. Kaneko[2]
[1]*National Institute of Advanced Industrial Science and Technology, Japan and* [2]*Hokkaido University, Japan*

SiC-P11 **Highly Accurate Virtual Dynamic Characterization of Discrete SiC Power Devices**
I. Kovačević-Badstübner, T. Ziemann, B. Kakarla and U. Grossner
Eidgenössische Technische Hochschule Zürich, Switzerland

SiC-P12 **Charge Storage Effect in SiC Trench MOSFET with a Floating p-Shield and Its Impact on Dynamic Performances**
J. Wei[1], M. Zhang[2], H. Jiang[3,4], H. Wang[1] and K.J. Chen[1]
[1]*Hong Kong University of Science and Technology, Hong Kong,* [2]*Hong Kong Polytechnic University, Hong Kong,* [3]*Dynex Semiconductor Ltd., UK and* [4]*Zhuzhou CRRC Times Electric Co., Ltd., China*

SiC-P13 **Influence of Gate Bias on the Avalanche Ruggedness of SiC Power MOSFETs**
A. Fayyaz[1], A. Castellazzi[1], G. Romano[2], M. Riccio[2], A. Irace[2], J. Urresti[3] and N. Wright[3]
[1]*University of Nottingham, UK,* [2]*Università degli Studi di Napoli Federico II, Italy and* [3]*Newcastle University, UK*

SiC-P14 **Evaluation of Drain Current Decrease by AC Gate Bias Stress in Commercially Available SiC MOSFETs**
M. Sometani[1], Y. Iwahashi[1], M. Okamoto[1], S. Harada[1], Y. Yonezawa[1], H. Okumura[1] and H. Yano[2]
[1]*National Institute of Advanced Industrial Science and Technology, Japan and* [2]*University of Tsukuba, Japan*

SiC-P15 **Short Circuit Capability and High Temperature Channel Mobility of SiC MOSFETs**
J. Sun, H. Xu, X. Wu, S. Yang, Q. Guo and K. Sheng
Zhejiang University, China

Poster Session 2: Module and Package

Wednesday, May 31, 15:10-17:10

Chair: T. Yamazaki, *Fuji Electric Co., Ltd.*

PK-P1 **A New Characterization Technique for Extracting Parasitic Inductances of Fast Switching Power MOSFETs Using Two-Port Vector Network Analyzer**
T. Liu, R. Ning, T.Y. Wong and Z.J. Shen
Illinois Institute of Technology, USA

PK-P2 **Current Distribution Based Power Module Screening by New Normal/Abnormal Classification Method with Image Processing**
M. Tsukuda[1], D. Yuki[2], H. Tomonaga[2], H. Kim[2] and I. Omura[2]
[1]*Green Electronics Research Institute, Japan and* [2]*Kyushu Institute of Technology, Japan*

PK-P3 **Power Cycling Capability of High Power IGBT Modules with Focus on Short Load Pulse Duration**

G. Zeng[1], Y. Ye[1], J. Lutz[1], R. Alvarez[2] and P. Correa[2]
[1]*Technische Universität Chemnitz, Germany and*
[2]*Siemens AG, Germany*

PK-P4 **Highly Thermal-Fatigue Resistant Si_3N_4 Substrates with Excellent Mechanical and Thermal Properties**

H. Miyazaki[1], Y. Zhou[1], K. Hirao[1], S. Fukuda[1], N. Izu[1], H. Hyuga[1], S. Iwakiri[2] and H. Hirotsuru[2]
[1]*National Institute of Advanced Industrial Science and Technology, Japan and* [2]*Denka Co., Ltd., Japan*

PK-P5 **High Power, High Frequency SiC-MOSFET System with Outstanding Performance, Power Density and Reliability**

S. Buetow, R. Herzer, G. Koenigsmann, M. Rossberg and A. Maul
Semikron Elektronik GmbH & Co. KG, Germany

PK-P6 **Stacked Resin Structure for Reducing Warpage of Transfer-Molded Modules**

S. Iwahashi, T. Otsuka and T. Nakamura
ROHM Co., Ltd., Japan

PK-P7 **Suppression of Self-Excited Oscillation for Common Package of Si-IGBT and SiC-MOS**

K. Saito[1], T. Miyoshi[2], D. Kawase[3], S. Hayakawa[3], T. Masuda[2] and Y. Sasajima[4]
[1]*Hitachi Europe Ltd., UK,* [2]*Hitachi, Ltd., Japan,* [3]*Hitachi Power Semiconductor Device, Ltd., Japan and* [4]*Ibaraki University, Japan*

PK-P8 **Chip-on-Board Assembly of 800V Si L-IGBTs for High Performance Ultra-Compact LED Drivers**

A.M. Aliyu[1], B. Mouawad[1], A. Castellazzi[1], P. Rajaguru[2], C. Bailey[2], V. Pathirana[3], N. Udugampola[3], T. Trajkovic[3] and F. Udrea[3]
[1]*University of Nottingham, UK,* [2]*University of Greenwich, UK and* [3]*University of Cambridge & Cambridge Microelectronics Ltd., UK*

PK-P9 **Pressure Contact Multi-Chip Packaging of SiC Schottky Diodes**

J. Ortiz Gonzalez[1], O. Alatise[1], P. Mawby[1], A.M. Aliyu[2] and A. Castellazzi[2]
[1]*University of Warwick, UK and* [2]*University of Nottingham, UK*

PK-P10 **Improving the Die Utilization and Lifetime in a Multi-Die SiC Power Module by Means of Integrated Per-Die Gate Buffers**

J. Ewanchuk, J. Brandelero and S. Mollov
Mitsubishi Electric Research Centre Europe, France

PK-P11 **Optimal Design of SiC MOSFETs for 20kW DCDC Converter**
W. Zhou, S. Yang, X. Wu and K. Sheng
Zhejiang University, China

Session 9: GaN Device: Robustness and Switching Losses

Thursday, June 1, 8:35-9:50

Chair: S. Pendharkar, *Texas Instruments*
Co-chair: T. Tsai, *TSMC*

9-1 **New Calorimetric Power Transistor Soft-Switching Loss Measurement Based on Accurate Temperature Rise Monitoring**
D. Neumayr, M. Guacci, D. Bortis and J.W. Kolar
Eidgenössische Technische Hochschule Zürich, Switzerland

9-2 **Pulse Robustness of AlGaN/GaN HEMTs with Schottky- and MIS-Gates**
C. Unger[1], M. Mocanu[2], M. Pfost[1], P. Waltereit[3] and R. Reiner[3]
[1]*Technische Universität Dortmund, Germany,* [2]*Hochschule Reutlingen, Germany and* [3]*Fraunhofer Institute for Applied Solid State Physics, Germany*

9-3 **Short-Circuit Capability in p-GaN HEMTs and GaN MISHEMTs**
M. Fernández[1], X. Perpiñà[1], M. Vellvehi[1], X. Jordà[1], J. Roig[2], F. Bauwens[2] and M. Tack[2]
[1]*Consejo Superior de Investigaciones Científicas, Spain and* [2]*ON Semiconductor, Belgium*

Session 10: Low Voltage Devices & Power IC Device Reliability & Ruggeddness

Thursday, June 1, 10:05-11:45

Chair: K. Kobayashi, *Toshiba Corporation*
Co-chair: Y. Miura, *Renesas Electronics Corporation*

10-1 **Investigation into HCI Improvement by a Split-Recessed-Gate Structure in an STI-Based nLDMOSFET**
T. Mori, H. Fujii, S. Kubo and T. Ipposhi
Renesas Semiconductor Manufacturing Co., Ltd., Japan

10-2 **Modeling of Time Dependent Breakdown Voltage Degradation in Trench Field Plate Power MOSFET**
T. Nishiwaki, K. Kobayashi and Y. Kawaguchi
Toshiba Corporation, Japan

10-3 **A New ESD Self-Protection Structure for 700V High Side Gate Drive IC**
S. Kim[1], D. LaFonteese[1], D. Zhu[1], S. Sridhar[1], S. Pendharkar[1], H. Endoh[2] and K. Boku[2]
[1] *Texas Instruments Incorporated, USA and* [2] *Texas Instruments Incorporated, Japan*

10-4 **HBM Robustness Optimization of Fully Isolated Nch-LDMOS for Negative Input Voltage Using Unique Index Parameter**
F. Takeuchi, H. Nagano, T. Sakamoto, K. Kimura and F. Matsuoka
Toshiba Corporation, Japan

Session 11: High Voltage Devices

Thursday, June 1, 13:05-14:45

Chair: C. Yun, *Trinno Technology*
Co-chair: Y.C. Choi, *Fairchild Semiconductor*

11-1 **Process Design of Superjunction MOSFETs for High Drain Current Capability and Low On-Resistance**
W. Saito
Toshiba Corporation, Japan

11-2 **High Aspect Ratio Deep Trench Termination (HARDT^2) Technique Surrounding Die Edge as Dielectric Wall to Improve High Voltage Device Area Efficiency**
T. Yamaguchi, H. Okumura, T. Shiraishi, T. Fujita, Y. Ata and K. Kobayashi
Toshiba Corporation, Japan

11-3 **An Advanced Bimode Insulated Gate Transistor BIGT with Low Diode Conduction Losses Under a Positive Gate Bias**
M. Rahimo, C. Papadopoulos, C. Corvasce and A. Kopta
ABB Switzerland Ltd., Switzerland

11-4 **Dependence of Switching Waveform on Charge Imbalance in Superjunction MOSFET Used in Inductive Load Circuit**
D. Arai, S. Hisada, M. Yamaji and S. Kunori
Shindengen Electric Mfg. Co., Ltd., Japan

Session 12: Packaging: Module Technology

Thursday, June 1, 15:00-15:50

Chair: J. Lutz, *Technical University of Chemnitz*

Co-chair: K. Saito, *Hitachi, Ltd.*

12-1 **Prominent Interface Structure and Bonding Material of Power Module for High Temperature Operation**

K. Sugiura[1,2], T. Iwashige[1], J. Kawai[1], K. Tsuruta[1], C. Chen[2], S. Nagao[2], H. Zhang[2], T. Sugahara[2], K. Suganuma[2], S. Kurosaka[3], Y. Sakuma[3] and Y. Oda[3]

[1]*Denso Corporation, Japan,* [2]*Osaka University, Japan and* [3]*C. Uyemura & Co., Ltd., Japan*

12-2 **Highly Reliable High-Temperature Superplastic Al-Zn Eutectoid Solder Joining with Stress Relaxation Characteristics for Next Generation SiC Power Semiconductor Devices**

J. Onuki[1], A. Chiba[1], M. Kawakami[1], K. Tamahashi[1], Y. Sugawara[1], T. Inami[1], M. Kobiyama[1], Y. Motohashi[1] and Y. Kawamata[2]

[1]*Ibaraki University, Japan and* [2]*Senju Metal Industry, Japan*

Award & Closing

Thursday, June 1, 15:50-16:10

Chairpersons: M. Mori, *Hitachi, Ltd.*

K. Hamada, *Toyota Motor Corporation*

I. Omura, *Kyushu Institute of Technology*

J. Shen, *Illinois Institute of Technology*