2017 International Mixed Signals Testing Workshop (IMSTW 2017)

Thessaloniki, Greece
3 – 5 July 2017

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Monday July 3, 2017

07:30 – 08:30: Registration

08:30 – 09:30: FEDFRO Opening Session

8:30 – 8:45 Welcome message

8:45 – 9:30 FEDFRO keynote talk 1

Trends and challenges in today's safety critical SoCs, Y. Zorian (Synopsis)

09:30 – 09:45: Break

09:45 – 10:45: IMSTW Opening Session

9:45 – 9:55 Welcome message

9:55 – 10:45 Opening keynote

Trends, their implications and solution approaches for future mixed characterization and test, Jochen Rivoir (Advantest)

10:45 – 11:00: Coffee Break

11:00 – 12:00: Session 1

Moderator: Haralampos-G. Stratigopoulos, LIP6

- **Likelihood-sampling adaptive fault simulation.....1**
  G. Leger, and A. Gines, IMSE-CNM, Universidad de Sevilla, Spain
- **Harmonic cancelation strategies for on-chip sinusoidal signal generation using digital resources.....7**
  H. Malloug, M. J. Barragan, S. Mir, TIMA, France
  H. Le Gall, STMicroelectronics, France

12:00 – 13:00: Session 2

Moderator: Rafael Castro, IMSE-CNM

- **Correntropy Applied to Fault Detection in Analogue Circuits.....13**
  J. Machado da Silva, INESC TEC, Universidade do Porto, Portugal
- **A Fault Analysis Framework for Analog Models Based on Abstraction (Invited talk).....N/A**
  E. Fraccaroli and F. Fummi, Univeristy of Verona, Italy

13:00 – 14:00: Lunch

14:00 – 15:00 Embedded Tutorial 1

Moderator: Salvador Mir, TIMA

- **Toward Silicon-Based Cognitive Neuromorphic ICs.....N/A**
  Y. Makris, UT Dallas, USA

15:00 – 15:15: Break

15:15 – 16:45: Special Session IMSTW-IOLTS:

Reliability on Electronic Devices and Circuits

Organizers: Francisco V. Fernandez, IMSE-CNM, Spain, and Günhan Dündar, Boğaziçi University, Turkey

- **Statistical characterization of unreliability effects in a 65-nm CMOS transistor array.....N/A**
  J. Diaz-Fortuny, J. Martin-Martinez, R. Rodriguez, M. Nafria, Universitat Autonoma de Barcelona, Spain,
  R. Castro-Lopez, E. Roca and F.V. Fernandez IMSE-CNM Universidad de Sevilla, Spain
- **Reliability Analysis and Mitigation of Near Threshold Caches.....18**
  A. Gebregiorgis and M. B. Tahoori, Karlsruhe Institute of Technology, Germany
- **Reliability of 3D-Printed Dynamic Scanners.....24**
  B. Mert Gönültaş, S. Aygün, R. Khayatzadeh, F. Çivitci, M. Berke Yelten and O. Ferhanoğlu, Istambul Technical University, Turkey
  Y. D. Gökdel, Bilgi University, Turkey

16:45 – 17:00: Break

20:00: Welcome Reception

Tuesday July 4, 2017

08:30 – 09:30: Embedded Tutorial 2:

Moderator: Gildas Léger, IMSE-CNM

- **Adapting the Test Process for Mixed-Signal ICs: Algorithm, Metrics, and Demonstration.....N/A**
  H. G. Stratigopoulos, LIP6, France
  C. Streitwieser, ams AG, Austria

09:30 – 09:45: Break

09:45 – 10:45: Panel IVSW-IMSTW: Emerging Design Challenges for Complex SoCs.

- **Panelist:** Bozena Kaminska, Antonio Acosta, Abhijit Chatterji, Padelis Papadopoulos, Antonio Rubio, Linda Milor
  Moderator: Magdy Abadir

11:45 – 11:15: Coffee Break

11:15 – 12:15: Session 3

Moderator: José Machado da Silva, U. Porto

- **Analytical Study of On-chip Generations of Analog Sine-Wave Based on Combined Digital Signals.....28**

S. David-Grignot, A. Lamlih, V. Kerzérho, F. Azaïs, F. Soulier, and S. Bernard, LIRMM, France,
Tristan Rouyer Sylvain Bonhommeau, Ifremer, France

- **Analog Circuit Testing (Invited talk).....33**
  A. Hatzopoulos, Aristotle University of Thessaloniki, Greece

12:15 – 13:30: Lunch

13:30 – 14:30: Session 4

Moderator: Elena Ioana Vatajelu, TIMA

- **Design of Efficient Analog Physically Unclonable Functions Using Alternative Test Principles.....39**
  S. Deyati, B. Muldrey, and A. Chatterjee, Georgia Institute of Technology, USA
  A. Singh, Auburn University, USA
- **Verification and test of real circuits - Structure-Preserving Modelling based on Signal Flow Graph (Invited talk).....43**
  M. Denguir and S. Sattler, Friedrich-Alexander-University Erlangen Nuremberg, Germany

14:30 – 14:45: Break

16:00: Social Event

Wednesday July 5, 2017

08:30 – 09:15: FEDFRO Keynote talk 2

- **Rigorous System Design, J. Sifakis (Verimag)**

09:15 – 09:30: Break

09:30 – 10:30: Distinguished speaker talk (shared with IVSW)

- **Secure Authentication of Electronic Systems with Autonomous Optical Nano-Devices.....N/A**
  B. Kaminska, Simon Fraser University, Canada

10:30 – 11:40: Coffee Break

10:45 – 11:45: Session 5

Moderator: A. Hatzopoulos, Aristotle University of Thessaloniki

- **Design of a Piece-Wise-Linear Ramp ADC for CMOS imagers (Invited talk).....N/A**
  C. Pastorelli, and S. Mir, TIMA, France
  P. Mellot, and C. Tubert, STMicroelectronics
- **A dimensionality-reduction method for test data - Fault diagnosis (Invited talk).....49**
  M. Denguir and S. Sattler, Friedrich-Alexander-University Erlangen Nuremberg, Germany

11:40 – 11:50: Break

11:50 – 12:20: Session 6

Moderator: Gildas Léger, IMSE-CNM

12:20-12:30: Workshop Closing Remarks

12:30-13:45 Lunch