2017 54th ACM/EDAC/IEEE Design Automation Conference (DAC 2017)

Austin, Texas, USA 18-22 June 2017

Pages 1-505



IEEE Catalog Number: CFP17DAC-POD ISBN: 978-1-5090-5664-4

Copyright © 2017 by the Institute of Electrical and Electronics Engineers, Inc. All Rights Reserved

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

*** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.

 IEEE Catalog Number:
 CFP17DAC-POD

 ISBN (Print-On-Demand):
 978-1-5090-5664-4

 ISBN (Online):
 978-1-4503-4927-7

ISSN: 0738-100X

Additional Copies of This Publication Are Available From:

Curran Associates, Inc 57 Morehouse Lane Red Hook, NY 12571 USA Phone: (845) 758-0400

Fax: (845) 758-2633

E-mail: curran@proceedings.com Web: www.proceedings.com





10.1 Ivory: Early-Stage Design Space Exploration Tool for Integrated Voltage Regulators.....1

An Zou, Jingwen Leng, Yazhou Zu, Tao Tong, Vijay Janapa Reddi, David Brooks, Gu-Yeon Wei, Xuan Zhang

- **10.2** Multi-Variable Dynamic Power Management for the GPU Subsystem.....7

 Pietro Mercati, Raid Ayoub, Michael Kishinevsky, Eric Samson, Marc Beuchat, Francesco Paterna, Tajana Simunic Rosing
- **10.3** Adaptive Thermal Management for 3D ICs with Stacked DRAM Caches.....13 *Dawei Li, Kaicheng Zhang, Akhil Guliani, Seda Ogrenci-Memik*
- **10.4** 3 Channel Dependency-Based Power Model for Mobile AMOLED Displays.....19 *Seongwoo Hong, Suk-Won Kim, Young-Jin Kim*
- **11.1** Arbitrary Precision and Complexity Tradeoffs for Gate-Level Information Flow Tracking.....25 *Andrew Becker, Wei Hu, Yu Tai, Philip Brisk, Ryan Kastner, Paolo Ienne*
- **11.2** Secure Information Flow Verification with Mutable Dependent Types.....31 *Andrew Ferraiuolo, Weizhe Hua, Andrew C Myers, G. Edward Suh*
- **11.3** Toggle MUX: How X-Optimism Can Lead to Malicious Hardware.....37 *Christian Krieg, Clifford Wolf, Axel Jantsch, Tanja Zseby*
- **11.4** XFC: A Framework for Exploitable Fault Characterization in Block Ciphers.....43 *Punit Khanna, Chester D Rebeiro, Aritra Hazra*
- **12.1** Efficient Hierarchical Performance Modeling for Integrated Circuits via Bayesian Co-Learning.....49 *Mohamad B Alawieh, Fa Wang, Xin Li*
- **12.2** Coupled Circuit/EM Simulation for Radio Frequency Circuits.....55 *Hans-Georg Brachtendorf, Kai Bittner, Wim Schoenmaker, Pascal Reynier*
- **12.3** Efficient Bayesian Yield Optimization Approach for Analog and SRAM Circuits.....61 *Mengshuo Wang, Fan Yang, Changhao Yan, Xuan Zeng, Xiangdong Hu*

12.4 A Scaling Compatible, Synthesis Friendly VCO-Based Delta-Sigma ADC Design and Synthesis
Methodology67
Biying Xu, Shaolan Li, Nan Sun, David Z. Pan

- **13.1** Extensibility-Driven Automotive In-Vehicle Architecture Design.....73 Samarjit Chakraborty, Wenchao Li, Hengyi Liang, Debayan Roy, Licong Zhang, Qi Zhu
- **13.2** Extensibility in Automotive Security: Current Practice and Challenges.....79 Sandip Ray, Wen Chen, Jayanta Bhadra, Mohammad Abdullah Al Faruque
- **13.3** Dynamic Platforms for Uncertainty Management in Future Automotive E/E Architectures.....85 *Philipp Mundhenk, Ghizlane Tibba, Licong Zhang, Felix Reimann, Debayan Roy, Samarjit Chakraborty*
- **14.1** A Pathway to Enable Exponential Scaling for the Beyond-CMOS Era....91

 Jian-Ping Wang, Kaushik Roy, Sachin Sapatnekar, X. Sharon Hu, Supriyo Datta, Steven Koester, Caroline Ross, Chia-Ling Chien, Paul Crowell, Roland Kawakami, Chris Kim, Azad Naeemi, Anand Raghunathan, Michael Niemier
- **14.2** In Quest of the Next Information Processing Substrate.....97
 Suman Datta, Alan Seabaugh, Michael Niemier, Arijit Raychowdhury, Darrell Schlom, Debdeep Jena, Grace Xing, H.-S. Philip Wong, Eric Pop, Sayeef Salahuddin, Sumeet Gupta, Supratik Gupta
- **14.3** A Systems Approach to Computing in Beyond CMOS Fabrics.....103

 Ameya Patil, Naresh Shanbhag, Lav Varshney, Eric Pop, H.-S. Philip Wong, Subhasish Mitra, Jan Rabaey, Jeffrey Weldon, Larry Pileggi, Sasikanth Manipatruni, Dmitri Nikonov, Ian Young
- **18.1** TrojanGuard: Simple and Effective Hardware Trojan Mitigation Techniques for Pipelined MPSoCs.....105 *Amin Malekpour, Roshan G Ragel, Aleksandar Ignjatovic, Sri Parameswaran*
- **18.2** Leveraging Compiler Optimizations to Reduce Runtime Fault Recovery Overhead.....111 Fateme S Hosseini, Pouya Fotouhi, Chengmo Yang, Guang R Gao
- **18.3** Energy-Aware Standby-Sparing on Heterogeneous Multicore Systems.....117 *Abhishek Roy, Hakan Aydin, Dakai Zhu*
- **18.4** Deep Reinforcement Learning for Building HVAC Control.....123 *Tianshu Wei, Yanzhi Wang, Qi Zhu*

19.1 No-Jump-Into-Basic-Block: Enforce Basic Block CFI on the Fly for Real-World Binaries129 Wenjian He, Sanjeev Das, Wei Zhang, Yang Liu
19.2 LO-FAT: Low-Overhead Control Flow Attestation in Hardware135 Ghada Dessouky, Shaza Zeitouni, Thomas Nyman, Andrew Paverd, Lucas V Davi, Patrick Koeberl, N. Asokan, Ahmad-Reza Sadeghi
19.3 Analyzing Hardware Based Malware Detectors141 Nisarg Patel, Avesta Sasan, Houman Homayoun
19.4 Instruction-Level Data Isolation for the Kernel on ARM147 Yeongpil Cho, Donghyun Kwon, Yunheung Paek
20.1 FlexCL: An Analytical Performance Model for OpenCL Workloads on Flexible FPGAs153 Shuo Wang, Yun Liang, Wei Zhang
20.2 A Comprehensive Framework for Synthesizing Stencil Algorithms on FPGAs using OpenCL Model159 <i>Shuo Wang, Yun Liang</i>
20.3 Automated Systolic Array Architecture Synthesis for High Throughput CNN Inference on FPGAs165 <i>Xuechao Wei, Cody Hao Yu, Peng Zhang, Youxiang Chen, Yuxin Wang, Han Hu, Yun Liang, Jason Cong</i>
20.4 LSC: A Large-Scale Consensus-Based Clustering Algorithm for High-Performance FPGAs171 Love Singhal, Mahesh A Iyer, Saurabh Adya
21.2 Linear Periodically Time-Varying (LPTV) Circuits Enable New Radio Architectures for Emerging Wireless Communication Paradigms177 Negar Reiskarimian, Linxiao Zhang, Harish Krishnaswamy
22.1 Challenges and Potential for Incorporating Model-Based Design in Medical Device Development181 <i>Louis Lintereur</i>
26.1 Fault-Tolerant Training with On-Line Fault Detection for RRAM-Based Neural Computing Systems182 <i>Lixue Xia, Mengyun Liu, Xuefei Ning, Krishnendu Chakrabarty, Yu Wang</i>
26.2 Learning to Produce Direct Tests for Security Verification Using Constrained Process Discovery188

Kuo-Kai Hsieh, Li-C Wang, Wen Chen, Jayanta Bhadra

26.3 Formal Techniques for Effective Co-Verification of Hardware/Software Co-Designs.....194 Rajdeep Mukherjee, Mitra Purandare, Raphael Polig, Daniel Kroening 26.4 Template Aware Coverage -Taking Coverage Analysis to the Next Level.....200 Raviv Gal, Einat Kermany, Bilal Saleh, Avi Ziv, Michael Behm, Bryan Hickerson **26.5** A-TEAM: Automatic Template-Based Assertion Miner.....206 Alessandro Danese, Nicolò Dalla Riva, Graziano Pravadelli **26.6** Path-Specific Functional Timing Verification Under Floating and Transition Modes of Operation.....212 Chun-Ning Lai, Jie-Hong (Roland) Jiang **27.1** Hierarchical Dataflow Modeling of Iterative Applications.....218 Hyesun Hong, Hyunok Oh, Soonhoi Ha 27.2 Stress-Aware Loops Mapping on CGRAs with Considering NBTI Aging Effect.....224 Jiangyuan Gu, Shouyi Yin, Shaojun Wei 27.3 Towards Aging-Induced Approximations.....230 Hussam Amrouch, Behnam Khaleghi, Andreas Gerstlauer, Jörg Henkel 27.4 QuAd: Design and Analysis of Quality-Area Optimal Low-Latency Approximate Adders.....236 Muhammad Abdullah Hanif, Rehan Hafiz, Osman Hasan, Muhammad Shafique 27.5 Bandwidth Optimization Through On-Chip Memory Restructuring for HLS.....242 Jason Cong, Peng Wei, Cody Hao Yu, Peipei Zhou 27.6 Energy-Efficient Execution for Repetitive App Usage on big.LITTLE Architectures.....248 Xianfeng Li, Guikang Chen, Wen Wen 28.1 DIMP: A Low-Cost Diversity Metric Based on Circuit Path Analysis.....254 Sergi Alcaide, Carles Hernandez, Antoni Roca, Jaume Abella

28.2 Estimation of Safe Sensor Measurements of Autonomous System Under Attack.....260

Raj Gautam Dutta, Xiaolong Guo, Teng Zhang, Kevin Kwiat, Charles Kamhoua, Laurent L Njilla, Yier Jin

28.3 Modeling the Effects of AUTOSAR Overheads on Application Timing and Schedulability266 <i>Manish Chauhan, Rodolfo Pellizzoni, Krzysztof Czarnecki</i>
28.4 Optimizing Message Routing and Scheduling in Automotive Mixed-Criticality Time-Triggered Networks272 Fedor Smirnov, Michael Glaß, Felix Reimann, Jürgen Teich
28.5 Real-Time Multi-Scale Pedestrian Detection for Driver Assistance Systems278 Maryam Hemmati, Morteza Biglari-Abhari, Smail Niar, Stevan Berber
28.6 Crossroads - Time-Sensitive Autonomous Intersection Management Technique284 Edward P Andert, Mohammad Khayatian, Aviral Shrivastava
31.1 Vertical M1 Routing-Aware Detailed Placement for Congestion and Wirelength Reduction in sub 10nm Nodes290 Peter Debacker, Kwangsoo Han, Andrew B Kahng, Hyein Lee, Praveen Raghavan, Lutong Wang
31.2 Toward Optimal Legalization for Mixed-Cell-Height Circuit Designs296 <i>Jianli Chen, Ziran Zhu, Wenxing Zhu, Yao-Wen Chang</i>
31.3 Fogging Effect Aware Placement in Electron Beam Lithography302 <i>Yu-Chen Huang, Yao-Wen Chang</i>
31.4 Pin Accessibility-Driven Cell Layout Redesign and Placement Optimization308 <i>Jaewoo Seo, Jinwook Jung, Sangmin Kim, Youngsoo Shin</i>
31.5 Fast Predictive Useful Skew Methodology for Timing-Driven Placement Optimization314 Seungwon Kim, SangGi Do, Seokhyeong Kang
31.6 Timing Driven Incremental Multi-Bit Register Composition Using a Placement-Aware ILP Formulation320 <i>Ioannis Seitanidis, Giorgos Dimitrakopoulos, Pavlos Mattheakis, Laurent H Masse-Navette, David Chinnery</i>
35.1 A 700fps Optimized Coarse-to-Fine Shape Searching Based Hardware Accelerator for Face Alignment326

Qiang Wang, Leibo Liu, Wenping Zhu, Huiyu Mo, Chenchen Deng, Shaojun Wei

35.2 An Efficient Memristor-Based Distance Accelerator for Time Series Data Mining on Data Centers.....332 Xiaowei Xu, Dewen Zeng, Wenyao Xu, Yiyu Shi, Yu Hu **35.3** Dadu: Accelerating Inverse Kinematics for High-DOF Robots.....338 Shigi Lian, Yinhe Han, Ying Wang, Hang Xiao, Xiaowei Li, Yungang Bao, Ninghui Sun 35.4 Towards Design and Automation of Hardware-Friendly NOMA Receiver with Iterative Multi-User Detection....344 Muhammad A Pasha, Momin A Uppal, Muhammad Hassan Ahmed, Muhammad Aimal Rehman, Muhammad Awais Bin Altaf **36.1** Fixed-Parameter Tractable Algorithms for Optimal Layout Decomposition and Beyond.....350 Jian Kuang, Evangeline F. Y. Young 36.2 Layout Hotspot Detection with Feature Tensor Generation and Deep Biased Learning.....356 Haoyu Yang, Jing Su, Yi Zou, Bei Yu, Evangeline Young 36.3 Minimizing Cluster Number with Clip Shifting in Hotspot Pattern Classification.....362 Kuan-Jung Chen, Yu-Kai Chuang, Bo-Yi Yu, Shao-Yun Fang 36.4 iClaire: A Fast and General Layout Pattern Classification Algorithm.....368 Wei-Chun Chang, Iris Hui-Ru Jiang, Yen-Ting Yu, Wei-Fang Liu 37.1 Compiler Techniques to Reduce the Synchronization Overhead of GPU Redundant Multithreading.....374 Manish Gupta, Daniel Lowell, John Kalamatianos, Steven Raasch, Vilas Sridharan, Dean Tullsen, Rajesh Gupta 37.2 Power-Aware Performance Tuning of GPU Applications Through Microbenchmarking.....380 Nicola Bombieri, Federico Busato, Franco Fummi 37.3 Low-Overhead Aging-Aware Resource Management on Embedded GPUs.....386 Haeseung Lee, Muhammad Shafique, Mohammad Abdullah Al Faruque

37.4 Optimizing Memory Efficiency for Convolution Kernels on Kepler GPUs.....392

Xiaoming Chen, Jianxu Chen, Danny Z Chen, Xiaobo Sharon Hu

- **38.1** A Testbed to Verify the Timing Behavior of Cyber-Physical Systems.....398

 Aviral Shrivastava, Mohammadreza Mehrabian, Mohammad Khayatian, Patricia Derler, Hugo Andrade, Kevin Stanton, Ya-Shian Li-Baboud, Edward Griffor, Marc Weiss, and John Eidson
- **43.1** Minimizing Thermal Gradient and Pumping Power in 3D IC Liquid Cooling Network Design.....404 *Gengjie Chen, Jian Kuang, Zhiliang Zeng, Hang Zhang, Evangeline F. Y. Young, Bei Yu*
- **43.2** Minimizing Pipeline Stalls in Distributed-Controlled Coarse-Grained Reconfigurable Arrays with Triggered Instruction Issue and Execution.....410

 Yanan Lu, Leibo Liu, Yangdong Deng, Jian Weng, Zhaoshi Li, Chenchen Deng, Shaojun Wei
- **43.3** A Clock Tree Optimization Framework with Predictable Timing Quality.....416 *Rickard Ewetz*
- **43.4** Optimal Circuits for Parallel Bit Reversal.....422 *Ren Chen, Viktor K Prasanna*
- **44.1** Towards Full-System Energy-Accuracy Tradeoffs: A Case Study of An Approximate Smart Camera System.....428 *Arnab Raha, Vijay Raghunathan*
- **44.2** Statistical Error Analysis for Low Power Approximate Adders.....434 *Muhammad Kamran Ayub, Osman Hasan, Muhammad Shafique*
- **44.3** CFPU: Configurable Floating Point Multiplier for Energy-Efficient Computing.....440 *Mohsen Imani, Daniel N Peroni, Tajana Simunik Rosing*
- **44.4** Error Propagation Aware Timing Relaxation For Approximate Near Threshold Computing.....446 Anteneh Gebregiorgis, Saman Kiamehr, Mehdi B Tahoori
- **45.1** Accurate High-Level Modeling and Automated Hardware/Software Co-Design for Effective SoC Design Space Exploration.....452 Wei Zuo, Louis Noel Pochet, Andrey Ayupov, Taemin Kim, Chung-Wei Lin, Shinichi Shiraishi, Deming Chen
- **45.2** Exploiting Thread and Data Level Parallelism for Ultimate Parallel SystemC Simulation.....458 *Tim Schmidt, Guantao Liu, Rainer Doemer*

- **45.3** HALWPE: Hardware-Assisted Light Weight Performance Estimation for GPUs.....464 *Kenneth O'Neal, Emily Shriver, Michael Kishinevsky, Philip Brisk*
- **45.4** Statistical Pattern Based Modeling of GPU Memory Access Streams.....470 Reena Panda, Xinnian Zheng, Jiajun Wang, Andreas Gerstlauer, Lizy K. John
- **46.3** ObfusCADe: Obfuscating Additive Manufacturing CAD Models Against Counterfeiting.....476 *Nikhil Gupta, Fei Chen, Nektarios Georgios Tsoutsos, Michail Maniatakos*
- **47.1** Specification, Verification and Design of Evolving Automotive Software.....482 Ramesh S, Birgit Vogel-Heuser, Wanli Chang, Debayan Roy, Licong Zhang, Samarjit Chakraborty
- **47.2** Safety Guard: Runtime Enforcement for Safety-Critical Cyber-Physical Systems.....488 *Meng Wu, Haibo Zeng, Chao Wang, Huafeng Yu*
- **51.1** Energy and Performance Trade-off in Nanophotonic Interconnects Using Coding Techniques.....494 *Cedric Killian, Daniel Chillet, Sebastien Le Beux, Dung V Pham, Olivier Sentieys, Ian D O'Connor*
- **51.2** MOCA: An Inter/Intra-Chip Optical Network for Memory.....500 *Zhehui Wang, Zhengbin Pang, Peng Yang, Jiang Xu, Xuanqi Chen, Rafael K Vivas Maeda, Zhifei Wang, Luan H.K. Duong, Haoran Li, Zhe Wang*
- **51.3** Low-Power On-Chip Network Providing Guaranteed Services for Snoopy Coherent and Artificial Neural Network Systems.....506 Bhavya K Daya, Li-Shiuan Peh, Anantha Chandrakasan
- **51.4** Task Mapping on SMART NoC: Contention Matters, Not the Distance.....512 *Lei Yang, Weichen Liu, Peng Chen, Nan Guan, Mengquan Li*
- **51.5** Accelerating Graph Community Detection with Approximate Updates via an Energy-efficient NoC.....518 *Karthi Duraisamy, Hao Lu, Partha P Pande, Ananth Kalyanaraman*
- **51.6** Network Synthesis for Database Processing Units.....524 Andrea Lottarini, Stephen Edwards, Kenneth A Ross, Martha Kim
- **52.1** Age-Aware Logic and Memory Co-Placement for RRAM-FPGAs.....530 *Yuan Xue, Chengmo Yang, Jingtong Hu*

52.2 Maximizing Forward Progress with Cache-Aware Backup for Self-powered Non-Volatile Processors.....536 Jing Li, Mengying Zhao, Lei Ju, Chun Jason Xue, Zhiping Jia 52.3 Toss-up Wear Leveling: Protecting Phase-Change Memories From Inconsistent Write Patterns.....542 Xian Zhang, Guangyu Sun 52.4 Exploiting Parallelism for Convolutional Connections in Processing-In-Memory Architecture.....548 Yi Wang, Mingxu Zhang, Jing Yang 52.5 Leave the Cache Hierarchy Operation as It Is: A New Persistent Memory Accelerating Approach.....554 Chun-Hao Lai, Jishen Zhao, Chia-Lin Yang **52.6** Ultra-Efficient Processing In-Memory for Data Intensive Applications.....560 Mohsen Imani, Saransh Gupta, Tajana Simunik Rosing 53.1 RIC: Relaxed Inclusion Caches for Mitigating LLC Side-Channel Attacks.....566 Mehmet Kayaalp, Khaled N Khasawneh, Hodjat Asghari Esfeden, Jesse Elwell, Nael Abu-Ghazaleh, Dmitry Ponomarev, Aamer Jaleel **53.2** FFD: A Framework for Fake Flash Detection.....572 Zimu Guo, Xiaolin Xu, Mark Tehranipoor, Domenic Forte 53.3 Delay Locking: Security Enhancement of Logic Locking Against IC Counterfeiting and Overproduction.....578 Yang Xie, Ankur Srivastava 53.4 Secure and Reliable XOR Arbiter PUF Design: An Experimental Study Based on 1 Trillion Challenge Response Pair Measurements.....584 Chen Zhou, Keshab K Parhi, Chris H Kim 53.5 ASSURE: Authentication Scheme for SecURE Energy Efficient Non-Volatile Memories.....590 Joydeep Rakshit, Kartik Mohanram 53.6 On Mitigation of Side-Channel Attacks in 3D ICs: Decorrelating Thermal Patterns From Power and

Activity.....596

Johann Knechtel, Ozgur Sinanoglu

56.3 Cryo-CMOS Electronic Control for Scalable Quantum Computing.....602 Fabio Sebastiano, Harald Homulle, Bishnu Patra, Rosario Incandela, Jeroen van Dijk, Lin Song, Masoud Babaie, Andrei Vladimirescu, Edoardo Charbon

60.1 PriSearch: Efficient Search on Private Data.....608 *M. Sadegh Riazi, Ebrahim M. Songhori , Farinaz Koushanfar*

60.2 An Architecture for Learning Stream Distributions with Application to RNG Testing.....614 *Alric Althoff, Ryan Kastner*

60.3 Cryptography for Next Generation TLS: Implementing the RFC 7748 Elliptic Curve448 Cryptosystem in Hardware.....620

Pascal Sasdrich, Tim Güneysu

60.4 Cross-Level Monte Carlo Framework for System Vulnerability Evaluation Against Fault Attack.....626 *Meng Li, Liangzhen Lai, Vikas Chandra, David Z. Pan*

61.1 Streak: Synergistic Topology Generation and Route Synthesis for On-Chip Performance-Critical Signal Groups.....632

Derong Liu, Vinicius Livramento, Salim Chowdhury, Duo Ding, Huy Vo, Akshay Sharma, David Z. Pan

61.2 TraPL: Track Planning of Local Congestion for Global Routing.....638

Daohang Shi, Azadeh Davoodi

61.3 Concurrent Pin Access Optimization for Unidirectional Routing.....644 *Xiaoqing Xu, Yibo Lin, Vinicius Livramento, David Z. Pan*

61.4 Incorporating the Role of Stress on Electromigration in Power Grids with Via Arrays.....650 *Vivek Mishra, Palkesh Jain, Sravan K Marella, Sachin S Sapatnekar*

62.1 SmartSwap: High-Performance and User Experience Friendly Swapping in Mobile Systems.....656 *Xiao Zhu, Duo Liu, Kan Zhong, Jinting Ren, Tao Li*

62.2 Reducing LDPC Soft-Sensing Latency by Lightweight Data Refresh for Flash Read Performance Improvement.....662

Yajuan Du, Qiao Li, Liang Shi, Deqing Zou, Hai Jin, Chun Jason Xue

62.3 Improving Performance and Lifetime of Large-Page NAND Storages Using Erase-Free Subpage Programming668 Myungsuk Kim, Jaehoon Lee, Sungjin Lee, Jisung Park, Jihong Kim
62.4 VirtualGC: Enabling Erase-Free Garbage Collection to Upgrade the Performance of Rewritable SLC NAND Flash Memory674 <i>Tseng-Yi Chen, Yuan-Hao Chang, Yuan-Hung Kuan, Yu-Ming Chang</i>
63.1 TIME: A Training-in-Memory Architecture for Memristor-Based Deep Neural Networks680 Ming Cheng, Lixue Xia, Zhenhua Zhu, Yi Cai, Yuan Xie, Yu Wang, Huazhong Yang
63.2 RESPARC: A Reconfigurable and Energy-Efficient Architecture with Memristive Crossbars for Deep Spiking Neural Networks686 Aayush Ankit, Abhronil Sengupta, Priyadarshini Panda, Kaushik Roy
63.3 Hardware-Software Codesign of Accurate, Multiplier-Free Deep Convolutional Neural Networks692 <i>Hokchhay Tann, Soheil Hashemi, Iris Bahar, Sherief Reda</i>
63.4 A New Stochastic Computing Multiplier and Its Application to Deep Neural Networks698 <i>Hyeonuk Sim, Jongeun Lee</i>
64.1 Optimized Design of a Human Intranet Network704 Ali Moin, Pierluigi Nuzzo, Alberto L Sangiovanni-Vincentelli, Jan M Rabaey
64.2 ArchEx: An Extensible Framework for the Exploration of Cyber-Physical System Architectures710 Dmitrii Kirov, Pierluigi Nuzzo, Roberto Passerone, Alberto L Sangiovanni-Vincentelli
64.3 EDiFy: An Execution Time Distribution Finder716 Boudewijn Braams, Sebastian J Altmeyer, Andy D Pimentel
64.4 Real-Time Meets Approximate Computing: An Elastic CNN Inference Accelerator with Adaptive Trade-off Between QoS and QoR722 <i>Ying Wang, Huawei Li, Xiaowei Li</i>
65.1 ESL Design with SystemC AMS: Introducing a top-down design methodology for mixed-signal systems728

Martin Barnasconi, Sumit Adhikari

65.2 Dealing with Uncertainties in Analog/Mixed-Signal Systems.....733 Christoph Grimm, Michael Rathmair 65.3 Advances in Formal Methods for the Design of Analog/Mixed-Signal Systems.....739 Vladimir Dubikhin, Chris Myers, Daniel Sokolov, Ioannis Syranidis, Alex Yakovlev 66.1 Test Methodology for Dual-Rail Asynchronous Circuits.....745 Kuan Yen Huang, Ting-Yu Shen, Chien Mo Li 66.2 Sneak-Path Based Test and Diagnosis for 1R RRAM Crossbar Using Voltage Bias Technique.....751 Tianjian Li, Xiangyu Bi, Naifeng Jing, Xiaoyao Liang, Li Jiang **66.3** A New Paradigm for Synthesis of Linear Decompressors.....757 Emil Gizdarski, Peter Wohl, John Waicukauski 66.4 InCheck: An In-Application Recovery Scheme for Soft-Errors.....763 Moslem Didehban, Sai Ram Dheeraj Lokam, Aviral Shrivastava 67.1 Latency-Aware Packet Processing on CPU-GPU Heterogeneous Systems.....769 Arian Maghazeh, Unmesh Dutta Bordoloi, Usman Dastgeer, Alexandru Andrei, Petru Eles, Zebo Peng 67.2 Cooperative DVFS for Energy-Efficient HEVC Decoding on Embedded CPU-GPU Architecture.....775 Fan Gong, Lei Ju, Deshan Zhang, Mengying Zhao, Zhiping Jia 67.3 Fast and Energy-Efficient Digital Filters for Signal Conditioning in Low-Power Microcontrollers.....781 Carlos Moreno, Sebastian Fischmeister 67.4 Enabling Write-Reduction Strategy for Journaling File Systems Over Byte-Addressable NVRAM.....787 Tseng-Yi Chen, Yuan-Hao Chang, Shuo-Han Chen, Chih-Ching Kuo, Ming-Chang Yang, Hsin-Wen Wei, Wei-Kuan Shih 68.1 HyCUBE: A CGRA with Reconfigurable Single-Cycle Multi-hop Interconnect.....793 Manupa Karunaratne, Aditi Kulkarni Mohite, Tulika Mitra, Li-Shiuan Peh **68.2** Phase-Driven Learning-Based Dynamic Reliability Management For Multi-Core Processors.....799

Zhiyuan Yang, Caleb Serafy, Tiantao Lu, Ankur Srivastava

- **68.3** A Heterogeneous SDR MPSoC in 28 nm CMOS for Low-Latency Wireless Applications.....805 Sebastian Haas, Tobias Seifert, Benedikt Nöthen, Stefan Scholze, Sebastian Höppner, Andreas Dixius, Esther Perez Adeva, Thomas Augustin, Friedrich Pauls, Sadia Moriam, Mattis Hasler, Erik Fischer, Yong Chen, Emil Matus, Georg Ellguth, Stephan Hartmann, St
- **68.4** Greybox Design Methodology: A Program Driven Hardware Co-Optimization with Ultra-Dynamic Clock Management.....811 *Tianyu Jia, Russ Joseph, Jie Gu*
- **69.1** Transport or Store? Synthesizing Flow-Based Microfluidic Biochips using Distributed Channel Storage.....817

 Chunfeng Liu, Bing Li, Hailong Yao, Paul Pop, Tsung-Yi Ho, Ulf Schlichtmann
- **69.2** A Discrete Model for Networked Labs-on-Chips: Linking the Physical World to Design Automation.....823 Andreas Grimmer, Werner Haselmayr, Andreas Springer, Robert Wille
- **69.3** Component-Oriented High-Level Synthesis for Continuous-Flow Microfluidics Considering Hybrid-Scheduling.....829

 Mengchu Li, Tsun-Ming Tseng, Bing Li, Tsung-Yi Ho, Ulf Schlichtmann
- **69.4** On Quality Trade-off Control for Approximate Computing Using Iterative Training.....835 *Chengwen Xu, Xiangyu Wu, Wenqi Yin, Qiang Xu, Naifeng Jing, Xiaoyao Liang, Li Jiang*
- **70.1** On Characterizing Near-Threshold SRAM Failures in FinFET Technology.....841 Shrikanth Ganapathy, John Kalamatianos, Keith Kasprak, Steven Raasch
- **70.2** Correlated Rare Failure Analysis via Asymptotic Probability Evaluation.....847 *Jun Tao, Handi Yu, Dian Zhou, Yangfeng Su, Xuan Zeng, Xin Li*
- **70.3** Making DRAM Stronger Against Row Hammering.....853 *Mungyu Son, Hyunsun Park, Junwhan Ahn, Sungjoo Yoo*
- **70.4** Developing Dynamic Profiling and Debugging Support in OpenCL for FPGAs.....859 Anshuman Verma, Huiyang Zhou, Skip Booth, Robbie King, James Coole, John Marshall, Andy Keep, Wuchun Feng
- **71.1** Accelerator Design for Deep Learning Training.....865 *Kailash Gopalakrishnan, Ankur Agrawal, Chia-Yu Chen, Jungwook Choi, Kailash Gopalakrishnan, Jinwook Oh, Sunil Shukla, Viji Srinivasan, Wei Zhang*

72.1 Co-Training of Feature Extraction and Classification Using Partitioned Convolutional Neural Networks867
Wei-Yu Tsai, Jinhang Choi, Tulika Parija, Priyanka Gomatam, Chita R Das, John Sampson, Vijaykrishnan Narayanan
72.2 Design of an Energy-Efficient Accelerator for Training of Convolutional Neural Networks Using Frequency-Domain Computation873
Jong Hwan Ko, Burhan A Mudassar, Taesik Na, Saibal Mukhopadhyay

- **72.3** A Kernel Decomposition Architecture for Binary-Weight Convolutional Neural Networks.....879 *Hyeonuk Kim, Jaehyeong Sim, Yeongjae Choi, Lee-Sup Kim*
- **72.4** Deep³: Leveraging Three Levels of Parallelism for Efficient Deep Learning.....885 *Bita Darvish Rouhani, Azalia Mirhoseini, Farinaz Koushanfar*
- **72.5** Exploring Heterogeneous Algorithms for Accelerating Deep Convolutional Neural Networks on FPGAs.....891 *Qingcheng Xiao, Yun Liang, Liqiang Lu, Shengen Yan, Yu-Wing Tai*
- **72.6** A Fast and Power Efficient Architecture to Parallelize LSTM Based RNN for Cognitive Intelligence Applications.....897

 Peng Ouyang, Shouyi Yin, Shaojun Wei
- **73.1** Power and Area Efficient Hold Time Fixing by Free Metal Segment Allocation.....903 Wei-Lun Chiu, Iris Hui-Ru Jiang, Chien-Pang Lu, Yu-Tung Chang
- **73.2** LibAbs: An Efficient and Accurate Timing Macro-Modeling Algorithm for Large Hierarchical Designs.....909 *Tin-Yin Lai, Tsung-Wei Huang, Martin D.F. Wong*
- **73.3** LSTA: Learning-Based Static Timing Analysis for High-Dimensional Correlated On-Chip Variations.....915 *Song Bian, Michihiro Shintani, Masayuki Hiromoto, Takashi Sato*
- **73.4** A Clock Skewing Strategy to Reduce Power and Area of ASIC Circuits.....921 *Niranjan Kulkarni, Aykut Dengi, Sarma Vrudhula*
- **73.5** A Spectral Graph Sparsification Approach to Scalable Vectorless Power Grid Integrity Verification.....927 *Zhiqiang Zhao, Zhuo Feng*

73.6 Convergence-Boosted Graph Partitioning Using Maximum Spanning Trees for Iterative Solution of Large Linear Circuits.....933 *Ya Wang, Wenrui Zhang, Peng Li, Jian Gong*

74.1 Retiming of Two-Phase Latch-Based Resilient Circuits.....939 *Hsiao-Lun Wang, Minghe Zhang, Peter A Beerel*

74.2 Graph-Based Logic Bit Slicing for Datapath-Aware Placement.....945 Chau-Chin Huang, Bo-Qiao Lin, Hsin-Ying Lee, Yao-Wen Chang, Kuo-Sheng Wu, Jun-Zhi Yang

74.3 SABER: Selection of Approximate Bits for the Design of Error Tolerant Circuits.....951 Deepashree Sengupta, Farhana Sharmin Snigdha, Jiang Hu, Sachin S Sapatnekar

74.4 Closing the Accuracy Gap of Static Performance Analysis of Asynchronous Circuits.....957 *Cheng-Yu Shih, Chun-Hong Shih, Jie-Hong (Roland) Jiang*

74.5 LiveSynth: Towards an Interactive Synthesis Flow.....963 *Rafael Trapani Possignolo, Jose Renau*

74.6 An Ultra-Low Power Address-Event Sensor Interface for Energy-Proportional Time-to-Information Extraction.....969

Alfio Di Mauro, Francesco Conti, Luca Benini

75.1 Pauli Frames for Quantum Computer Architectures.....975 Leon Riesebos, Xiang Fu, Savvas Varsamopoulos, Carmen G. Almudever, Koen Bertels

75.2 Fast Embedding of Constrained Satisfaction Problem to Quantum Annealer with Minimizing Chain Length.....981

Juexiao Su, Lei He

75.3 Hierarchical Reversible Logic Synthesis Using LUTs.....987 *Mathias Soeken, Martin Roetteler, Nathan Wiebe, Giovanni De Micheli*

75.4 Detailed Placement for Two-Dimensional Directed Self-Assembly Technology.....993 *Zhi-Wen Lin, Yao-Wen Chang*

75.5 Design Methodology for Thin-Film Transistor Based Pseudo-CMOS Logic Array with Multi-Layer Interconnect Architecture.....999

Qinghang Zhao, Yongpan Liu, Wenyu Sun, Jiaqing Zhao, Hailong Yao, Xiaojun Guo, Huazhong Yang

75.6 Hardware ODE Solvers Using Stochastic Circuits.....1005 Siting Liu, Jie Han

- **76.1** A Novel ReRAM-Based Main Memory Structure for Optimizing Access Latency and Reliability.....1011 Yang Zhang, Dan Feng, JingNing Liu, Wei Tong, Bing Wu, Caihua Fang
- **76.2** Boosting the Performance of 3D Charge Trap NAND Flash with Asymmetric Feature Process Size Characteristic.....1017
 Shuo-Han Chen, Yen-Ting Chen, Hsin-Wen Wei, Wei-Kuan Shih
- **76.3** Disturbance Aware Memory Partitioning for Parallel Data Access in STT-RAM.....1023 Shouyi Yin, Zhicong Xie, Shaojun Wei
- **76.4** Group Scissor: Scaling Neuromorphic Computing Design to Large Neural Networks.....1029 *Yandan Wang, Wei Wen, Beiye Liu, Donald Chiarulli, Helen Li*
- **76.5** Adaptation of Enhanced TSV Capacitance as Membrane Property in 3D Brain-Inspired Computing System.....1035 *Md Amimul Ehsan, Hongyu An, Zhen Zhou, Yang Yi*

76.6 Rescuing Memristor-Based Neuromorphic Design with High Defects.....1041 *Chenchen Liu, Miao Hu, John Paul Strachan, Helen Li*