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Technical Papers

Session 1	Spintronic I
Date/Time	Tuesday, 25 July 2017 / 10:15 – 11:15

A Novel SRAM - STT-MRAM Hybrid Cache Implementation Improving Cache Performance
Guillaume Patrigeon, Sophiane Senni, Lionel Torres, Odilia Coi and Pascal Benoit

Compact Modeling of High Spin Transfer Torque Efficiency Double-Barrier Magnetic Tunnel Junction
Guanda Wang, Yue Zhang, Zhizhong Zhang, Jiang Nan, Zhenyi Zheng, Yu Wang, Lang Zeng, Youguang Zhang and Weisheng Zhao

Session 2	Neural networks I
Date/Time	Tuesday, 25 July 2017/ 11:15 – 12:15

SkyNet: Memristor-based 3D IC for Artificial Neural Networks
Sachin Bhat, Sourabh Kulkarni, Jiajun Shi, Mingyu Li and Csaba Andras Moritz

Mixing Circuit based on Neural Associative Memories and Nanoelectronic 1S1R Cells
Arne Heittmann and Tobias G. Noll

Spatio-temporal Learning with Arrays of Analog Nanosynapses
Christopher H. Bennett, Damien Querlioz and Jacques-Olivier Klein

Session 3	Poster Pitch
Date/Time	Tuesday, 25 July 2017 / 13:00 – 13:30

Design and Operational Assessment of an Intra-Cell Hybrid L2 Cache
Fabrizio Lombardi, Weiqiang Liu, Jie Han and Linbin Chen

L^{3}EP: Low Latency, Low Energy Program-and-Verify for Triple-Level Cell Phase Change Memory
Ali Alsuwaiyan and Kartik Mohanram

Transient Model with Interchangeability for Dual-Gate Ambipolar CNTFET Logic Design
Xuan Hu and Joseph S. Friedman

A Compact 8-bit Adder Design using In-Memory Memristive Computing: Towards Solving the Feynman Grand Challenge
Sumit Kumar Jha, Sunny Raj and Dwaipayan Chakraborty

Reconfigurable Processing In Memory Architecture based on Spin Orbit Torque MRAM
Liang Chang, Zhaohao Wang, Youguang Zhang and Weisheng Zhao

Automated Synthesis of Compact Multiplier Circuits for in-Memory Computing using ROBDDs
Amad Ul Hassen

Linear Regression based Multi-State Logic Decomposition Approach for Efficient Hardware Implementation
Wafi Danesh and Mostafizur Rahman

Verilog-A Compact Model of a ME-MTJ Based XNOR/NOR Gate
Nishtha Sharma, Andrew Marshall and Jonathan Bird

Session 4	Concept papers I
Date/Time	Tuesday, 25 July 2017 / 14:30 – 15:45

Proposal for Novel Magnetic Memory Device with Spin Momentum Locking Materials
Xiaowan Qin, Lang Zeng, Tianqi Gao, Deming Zhang, Mingzhi Long, Youguang Zhang and Weisheng Zhao

Frequency Modulation of Spin Torque Nano Oscillator with Voltage Controlled Magnetic Anisotropy Effect
Zuodong Zhang, Lang Zeng, Tianqi Gao, Deming Zhang, Xiaowan Qin, Mingzhi Long, Youguang Zhang, Haiming Yu and Weisheng Zhao

Memcapacitive Reservoir Computing
Dat Tran, S.J. and Christof Teuscher

CASPER - Configurable Design Space Exploration of Programmable Architectures for Machine Learning using Beyond Moore Devices
Dilip Vasudevan, George Michelogiannakis , David Donofrio and John Shalf

Fine-Grained 3D Reconfigurable Computing Fabric with RRAM
Mingyu Li, Jiajun Shi, Sachin Bhat and Csaba Andras Moritz

Session 5	Devices and circuits I
Date/Time	Tueday, 25 July 2017 / 16:00 – 16:40

Low Cost Multi-Error Correction for 3D Polyhedral Memories
Mihai Lefter, Thomas Marconi, George Razvan Voicu and Sorin Dan Cotofana

Low-Power Multiplexer Designs Using Three-Independent-Gate Field Effect Transistors
Edouard Giacomin, Jorge Romero Gonzalez and Pierre-Emmanuel Gaillardon

Session 6	Spintronic II
Date/Time	Wednesday, 26 July 2017 / 09:00 – 10:15

A Logic-in-Memory Design with 3-Terminal Magnetic Tunnel Junction Function Evaluators for Convolutional Neural Networks
Sumit Dutta, Saima A. Siddiqui, Felix Büttner, Luqiao Liu, Caroline A. Ross and Marc A. Baldo

High Performance and Energy-Efficient In-Memory Computing Architecture based on SOT-MRAM
Zhezhi He, Shaahin Angizi, Farhana Parveen and Deliang Fan

Polymorphic Spintronic Logic Gates for Hardware Security Primitives - Device Design and Performance Benchmarking
S.Rakheja and N.Kani

Session 7	Neural networks II
Date/Time	Wednesday, 26 July 2017 / 10:30 – 11:50

Fully-Connected Single-Layer STT-MTJ-based Spiking Neural Network under Process Variability
Elena Ioana Vatajelu and Lorena Anghel

Non-Temporal Logic Performance of an Atomic Switch Network
Kelsey Scharnhorst, Walt Woods, Christof Teuscher, Adam Stieg and James Gimzewski

Approximate Vector Matrix Multiplication Implementations for Neuromorphic Applications using Memristive Crossbars
Walt Woods and Christof Teuscher

Session 8	Concept papers II
Date/Time	Wednesday, 26 July 2017 / 12:30 – 13:15

Epsilon-greedy Strategy for Online Dicitionary Learning with Realistic Memristor Array Constriants
Fuxi Cai and Wei D. Lu

Hybrid Neural Network using Binary RRAM Devices
Mohammed A. Zidan, Yeonjoo Jeong and Wei D. Lu

Naive Bayesian Inference of Handwritten Digits using a Memristive Associative Memory
Mohammad M.A. Taha and Christof Teuscher

Session 9	Memories
Date/Time	Wednesday, 26 July 2017 / 13:15 – 14:15

Architecture, Design and Technology Guidelines for Crosspoint Memories
A. Levisse, P. Royer, B. Giraud, J.P. Noel, M. Moreau and J.M. Portal

Ultra High Density 3D SRAM Cell Design in Stacked Horizontal Nanowire (SN3D) Fabric
Naveen Macha, Sandeep Geedipally and Mostafizur Rahman

Session 10	Devices and circuits II
Date/Time	Wednesday, 26 July 2017 / 14:30 – 16:20

AOI-Based Data-Centric Circuits for Near-Memory Processing
Fabrizio Lombardi and Salin Junsangsri

Power-Delivery Network in 3D ICs: Monolithic 3D vs. Skybridge 3D CMOS
Jiajun Shi, Mingyu Li and Csaba Andras Moritz

Energy Efficient Computation using Injection Locked Bias-Field Free Spin-Hall Nano-Oscillator Array with Shared Heavy Metal
Karthik Yogendra, Minsuk Koo and Kaushik Roy

A self-calibrating sense amplifier fora true random number generator using hybrid FinFET-Straintronic MTJ
Sudipta Bhuin, Joseph Sweeney, Samuel Pagliarini, Ayan K.Biswas and Lawrence Pileggi