

2017 Euromicro Conference on Digital System Design (DSD 2017)

**Vienna, Austria
30 August – 1 September 2017**



**IEEE Catalog Number: CFP17291-POD
ISBN: 978-1-5386-2147-9**

**Copyright © 2017 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP17291-POD
ISBN (Print-On-Demand):	978-1-5386-2147-9
ISBN (Online):	978-1-5386-2146-2

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

2017 Euromicro Conference on Digital System Design

DSD 2017

Table of Contents

Message from the General Chairs	xiii
Message from the Program Chairs	xiv
DSD 2017 Committees	xvi
Program Committee	xvii
Additional Reviewers	xxiv
Keynotes	xxv

LPA: Low-Power Architectures and Design Methods

Building a Better Random Number Generator for Stochastic Computing	1
<i>Florian Neugebauer, Ilia Polian, and John P. Hayes</i>	
Rapid Estimation of Power-Management Unit Overhead from System-Level Specification	9
<i>Dominik Macko</i>	
Loop Overhead Reduction Techniques for Coarse Grained Reconfigurable Architectures	14
<i>Kanishkan Vadivel, Mark Wijtvliet, Roel Jordans, and Henk Corporaal</i>	
Autonomous Power Management for Embedded Systems Using a Non-linear Power Predictor	22
<i>Sidarta Azevedo Lobo De Carvalho, Daniel Carvalho Da Cunha, and Abel Guilhermino Da Silva-Filho</i>	

SMVS: Specification, Modeling, Verification and Simulation Methods and Tools

An Aspect and Transaction Oriented Programming, Design and Verification Language (PDVL)	30
<i>Tobias Strauch</i>	
Optimizing Memory Access Performance Using Hardware Assisted Virtualization in Retargetable Dynamic Binary Translation	40
<i>Antoine Faravelon, Olivier Gruber, and Frédéric Pétrot</i>	

Static Write Buffer Cache Modeling to Increase Host-Compiled Simulation Accuracy	47
<i>Hector Posadas, Luis Díaz, and Eugenio Villar</i>	
Assertion-Based Verification for SoC Models and Identification of Key Events	54
<i>Laurence Pierre and Martial Chabot</i>	

RTHP: Advanced Applications, Real-Time and High-Performance Design

An Architecture for Online-Diagnosis Systems Supporting Compressed Communication	62
<i>Seungbum Jo, Markus Lohrey, Damian Ludwig, Simon Meckel, Roman Obermaisser, and Simon Plasger</i>	
A Hardware/Software Codesign for the Chemical Reactivity of BRAMS	70
<i>Carlos Alberto Oliveira De Souza Junior, Erinaldo Da Silva Pereira, and Eduardo Marques</i>	
Nepton Processor for Real-Time Computation of Conductance-Based Neuronal Networks	78
<i>Marcel Beuler, Alexander Krum, Werner Bonath, and Hartmut Hillmer</i>	
System-Aware Performance Monitoring Unit for RISC-V Architectures	86
<i>Tobias Scheipel, Fabian Mauroner, and Marcel Baunach</i>	
SPEED: Open-Source Framework to Accelerate Speech Recognition on Embedded GPUs	94
<i>Syed Mohammad Asad Hassan Jafri, Ahmed Hemani, and Leonardo Intesa</i>	
EventIRQ: An Event Based and Priority Aware IRQ Handling for Multi-tasking Environments	102
<i>Fabian Mauroner and Marcel Baunach</i>	
Design of an On-chip System for the SET Pulse Width Measurement	111
<i>Marko Andjelkovic, Vladimir Petrovic, Miljana Nenadovic, Anselm Breitenreiter, Milose Krstic, and Rolf Kraemer</i>	
Acceleration Techniques for System-Hyper-Pipelined Soft-Processors on FPGAs	119
<i>Tobias Strauch</i>	

DSM: Design and Synthesis Methods

Application Specific Behavioral Synthesis Design Space Exploration: Artificial Neural Networks. A Case Study	129
<i>Benjamin Carrion Schafer, David Aledo, and Félix Moreno</i>	
Composition of Switching Lattices and Autosymmetric Boolean Function Synthesis	137
<i>Anna Bernasconi, Valentina Ciriani, Luca Frontini, and Gabriella Trucco</i>	
Performance Targeted Minimization of Incompletely Specified Finite State Machines for Implementation in FPGA Devices	145
<i>Adam Klimowicz</i>	

A Feedback-Based Design Space Exploration Subsystem for the Automation of Architectures Synthesis on Proprietary FPGA Toolchains	151
<i>Alessandro Pappalardo, Giuseppe Natale, and Marco Domenico Santambrogio</i>	
Analysis and Visualization of Product Memory Layout in IP-XACT	155
<i>Esko Pekkarinen, Mikko Teuho, and Timo D. Hämäläinen</i>	
SAT-Based Generation of Optimum Function Implementations with XOR Gates	163
<i>Petr Fišer, Ivo Háleček, and Jan Schmidt</i>	

SNOC: Systems-on-a-Chip and Networks-on-a-Chip

Scalable and Power-Efficient Implementation of an Asynchronous Router with Buffer Sharing	171
<i>Charles Effiong, Gilles Sassatelli, and Abdoulaye Gamatie</i>	
Packet Classification with Limited Memory Resources	179
<i>Michal Kekely and Jan Korenek</i>	
A Distributed NUCA Architecture Using an Efficient NoC Multicasting Support	184
<i>Hela Belhadj Amor, Abbas Sheibanyrad, and Frédéric Pérot</i>	
A Programmable Inbound Transfer Processor for Active Messages in Embedded Multicore Systems	192
<i>Yves Durand, Christian Bernard, Romain Lemaire, Cesar Fuguet Tortolero, and Emilie Garat</i>	
Automatic Control Flow Generation for OpenVX Graphs	198
<i>Merten Popp, Stef van Son, and Orlando Moreira</i>	

AHSA: Architectures and Hardware for Security Applications

Higher-Order Side-Channel Protected Implementations of KECCAK	205
<i>Hannes Gross, David Schaffnerath, and Stefan Mangard</i>	
Lightweight Software Encryption for Embedded Processors	213
<i>Thomas Hiscock, Olivier Savry, and Louis Goubin</i>	
A Design Strategy for Digit Serial Multiplier Based Binary Edwards Curve Scalar Multiplier Architectures	221
<i>Apostolos P. Fournaris, Charalambos Dimopoulos, and Odysseas Koufopavlou</i>	
Hardware-Secured Configuration and Two-Layer Attestation Architecture for Smart Sensors	229
<i>Thomas Ulz, Thomas Pieber, Christian Steger, Sarah Haas, Rainer Matischek, and Holger Bock</i>	
Side Channel Evaluation of PUF-Based Pseudorandom Permutation	237
<i>Durga Prasad Sahoo, Phuong Ha Nguyen, Debapriya Basu Roy, Debdeep Mukhopadhyay, and Rajat Subhra Chakraborty</i>	

How Microprobing Can Attack Encrypted Memory	244
<i>Sergei Skorobogatov</i>	
Role of Laser-Induced IR Drops in the Occurrence of Faults: Assessment and Simulation	252
<i>Raphael Andreoni Camponogara Viera, Jean-Max Dutertre, Rodrigo Possamai Bastos, and Philippe Maurine</i>	
Influence of Fault-Tolerance Techniques on Power-Analysis Resistance of Cryptographic Design	260
<i>Jan Řiha, Vojtěch Miškovský, Hana Kubátová, and Martin Novotný</i>	
Thermal Sensor Based Hardware Trojan Detection in FPGAs	268
<i>Lampros Pyrgas, Filippas Pirpilidis, Alikí Panayiotarou, and Paris Kitsos</i>	
Analysis and Inner-Round Pipelined Implementation of Selected Parallelizable CAESAR Competition Candidates	274
<i>Sanjay Deshpande and Kris Gaj</i>	

AHSA-Posters

Counterfeit IC Detection By Image Texture Analysis	283
<i>Pallabi Ghosh and Rajat Subhra Chakraborty</i>	
Run-Time Effect by Inserting Hardware Trojans, in Combinational Circuits	287
<i>Fotios Kounelis, Nicolas Sklavos, and Paris Kitsos</i>	
Exploiting Quantum Gates in Secure Computation	291
<i>Maryam Ehsanpour, Stelvio Cimato, Valentina Ciriani, and Ernesto Damiani</i>	
IoT Components LifeCycle Based Security Analysis	295
<i>Johan Marconot, Florian Pebay-Peyroula, and David Hély</i>	

DTFT: Dependability, Testing and Fault Tolerance in Digital Systems

Necessity of Fault Tolerance Techniques in Xilinx Kintex 7 FPGA Devices for Space Missions: A Case Study	299
<i>Louis van-Harten, Roel Jordans, and Hamid Pourshaghagh</i>	
SAT-Based ATPG for Zero-Aliasing Compaction	307
<i>Robert Hülle, Petr Fišer, and Jan Schmidt</i>	
A Functional Test Framework to Observe MPSoC Power Management Techniques in Virtual Platforms	315
<i>Sören Schreiner, Maher Fakih, Kim Grüettner, Duncan Graham, Wolfgang Nebel, and Salvador Peiró Frasquet</i>	
PCG: Partially Clock-Gating Approach to Reduce the Power Consumption of Fault-Tolerant Register Files	323
<i>Alireza Namazi and Meisam Abdollahi</i>	

Setup for an Experimental Study of Radiation Effects in 65nm CMOS	329
<i>Bernhard Fritz, Andreas Steininger, Vaclav Simek, and Varadan Savulimedu Veeravalli</i>	
Reliability Analysis and Improvement of FPGA-Based Robot Controller	337
<i>Jakub Podivinsky, Jakub Lojda, Ondrej Cekan, Richard Panek, and Zdenek Kotasek</i>	
Thermal Effect on Performance, Power, and BTI Aging in FinFET-Based Designs	345
<i>Warin Sootkaneung, Suppachai Howimanporn, and Sasithorn Chookaew</i>	

DTFT-Posters

On Dependability Assessment of Fault Tolerant Systems by Means of Statistical Model Checking	352
<i>Josef Strnadel</i>	
A Probabilistic Context-Free Grammar Based Random Test Program Generation	356
<i>Ondrej Cekan and Zdenek Kotasek</i>	
Dependability Prediction Involving Temporal Redundancy and the Effect of Transient Faults	360
<i>Martin Daňhel, Filip Štěpánek, and Hana Kubátová</i>	
LORAP: Low-Overhead Power and Reliability-Aware Task Mapping Based on Instruction Footprint for Real-Time Applications	364
<i>Alireza Namazi, Meisam Abdollahi, Saeed Safari, and Siamak Mohammadi</i>	

ASAIT: Architectures and Systems for Automotive and Intelligent Transportation

A 3D Time-of-Flight Mixed-Criticality System for Environment Perception	368
<i>Josef Steinbaeck, Allan Tengg, Gerald Holweg, and Norbert Druml</i>	
A Subplatooning Strategy for Safe Braking Maneuvers	375
<i>Dharshan Krishna Murthy and Alejandro Masrur</i>	
On the Benefits of Multicores for Real-Time Systems	383
<i>Selma Saidi</i>	
FPGA-Centric High Performance Embedded Computing: Challenges and Trends	390
<i>Rabie Ben Atitallah and Karim M. A. Ali</i>	

SDIS: System Design for Intelligent Systems

A Survey on Open-Source Flight Control Platforms of Unmanned Aerial Vehicle	396
<i>Emad Ebeid, Martin Skriver, and Jie Jin</i>	
A Scalable Cloud Computing Infrastructure for Geospatial Data Analytics for Change Detection	403
<i>Rune Hylsberg Jacobsen, Jacob Høxbroe Jeppesen, Kim Fibiger Laursen, John Skovsgaard, Henrik Nymann Jensen, and Thomas Skjødeberg Toftegaard</i>	

Evaluating the Impact of Communication Network Performance on Supervisory Supermarket Control	411
<i>Jacob T. Madsen, Tomasz Minko, Tatiana K. Madsen, and Hans-Peter Schwefel</i>	

MCSDIA: Mixed Criticality System Design, Implementation and Analysis

Modular Development and Certification of Dependable Mixed-Criticality Systems	419
<i>Asier Larrucea, Imanol Martinez, Carlos Fernando Nicolas, Jon Perer, and Roman Obermaisser</i>	
Mixed Time-Criticality Process Interferences Characterization on a Multicore Linux System	427
<i>Federico Reghenzani, Giuseppe Massari, and William Fornaciari</i>	

MCSDIA-Posters

Model-Based Function Mapping and Bandwidth Reservation for Mixed-Critical Adaptive Systems	435
<i>Mahmoud Hussein, Ansgar Radermacher, and Reda Nouacer</i>	
Boosting Guaranteed Performance in Wormhole NoCs with Probabilistic Timing Analysis	440
<i>Mladen Slijepcevic, Carles Hernandez, Jaume Abella, and Francisco J. Cazorla</i>	

ASHWPA: Advanced Systems in Healthcare, Wellness and Personal Assistance

The HELICoiD Project: Parallel SVM for Brain Cancer Classification	445
<i>Emanuele Torti, Camilla Cividini, Alessandro Gatti, Giovanni Danese, Francesco Leporati, Himar Fabelo, Samuel Ortega, and Gustavo Marrero Callicò</i>	
Hardware Platforms Benchmark For Real-Time Polyp Detection	451
<i>Quentin Angermann, Aymeric Histace, Maroua Hammami, Mehdi Terosiet, Lionel Faurlini, and Olivier Romain</i>	
Wireless and Portable System for the Study of in-vitro Cell Culture Impedance Spectrum by Electrical Impedance Spectroscopy	456
<i>Edwin De Roux, M. Terosiet, F. Kölbl, J. Chrun, P.H. Aubert, P. Banet, M. Boissière, E. Pauthe, A. Histace, and O. Romain</i>	
Towards a Mobile Health Platform with Parallel Processing and Multi-sensor Capabilities	462
<i>Florian Glaser, Philipp Schönle, Pascale Meier, Jonathan Bösser, Noé Brun, Thomas Burger, Schekeb Fateh, Giovanni Rovere, Luca Benini, and Qiuting Huang</i>	

EPDSD: European Projects in Digital System Design

Towards a Safe Software Development Environment	470
<i>Mahmoud Hussein, Reda Nouacer, and Ansgar Radermacher</i>	
MANGO: Exploring Manycore Architectures for Next-GeneratiOn HPC Systems	478
<i>José Flich, Giovanni Agosta, Philipp Ampletzer, David Atienza Alonso, Carlo Brandolese, Etienne Cappe, Alessandro Cilardo, Leon Dragić, Alexandre Dray, Alen Duspara, William Fornaciari, Gerald Guillaume, Ynse Hoornenborg, Arman Iranfar, Mario Kovač, Simone Libutti, Bruno Maitre, José Maria Martínez, Giuseppe Massari, Hrvoje Mlinarić, Ermis Papastefanakis, Tomás Picornell, Igor Piljić, Anna Pupykina, Federico Reghenzani, Isabelle Staub, Rafael Tornero, Marina Zapater, and Davide Zoni</i>	
Paving the Way Towards a Highly Energy-Efficient and Highly Integrated Compute Node for the Exascale Revolution: The ExaNoDe Approach	486
<i>Alvise Rigo, Christian Pinto, Kevin Pouget, Daniel Raho, Denis Dutoit, Pierre-Yves Martinez, Chris Doran, Luca Benini, Iakovos Mavroidis, Manolis Marazakis, Valeria Bartsch, Guy Lonsdale, Antoniu Pop, John Goodacre, Annaik Colliot, Paul Carpenter, Petar Radojković, Dirk Pleiter, Dominique Drouin, and Benoît Dupont de Dinechin</i>	
The MegaM@Rt2 ECSEL Project: MegaModelling at Runtime — Scalable Model-Based Framework for Continuous Development and Runtime Validation of Complex Systems	494
<i>Wasif Afzal, Hugo Bruneliere, Davide Di Ruscio, Andrey Sadovkyh, Silvia Mazzini, Eric Cariou, Dragos Truscan, Jordi Cabot, Daniel Field, Luigi Pomante, and Pavel Smrz</i>	
Security & Trusted Devices in the Context of Internet of Things (IoT)	502
<i>Nicolas Sklavos, Ioannis D. Zaharakis, Achilles Kameas, and Angeliki Kalapodi</i>	
The Next Generation of Exascale-Class Systems: The ExaNeSt Project	510
<i>Roberto Ammendola, Andrea Biagioni, Paolo Cretaro, Ottorino Frezza, Francesca Lo Cicero, Alessandro Lonardo, Michele Martinelli, Pier Stanislao Paolucci, Elena Pastorelli, Francesco Simula, Piero Vicini, Giuliano Taffoni, Jose A. Pascual, Javier Navaridas, Mikel Luján, John Goodacree, Nikolaos Chrysos, and Manolis Katevenis</i>	

Main-Posters

Exploiting Kant and Kimura's Matrix Inversion Algorithm on FPGA	516
<i>André Bannwart Perina, Paulo Matias, Eduardo Marques, Vanderlei Bonato, and João Miguel Gago Pontes De Brito Lima</i>	
Designing a Synthetic Aperture Radar's Data Formatting and Antenna Gyro Stabilizing Module	520
<i>Ricardo de Porras Bernácer</i>	

Two-Phase Interarrival Time Prediction for Runtime Resource Management	524
<i>Mina Niknafs, Ivan Ukhov, Petru Eles, and Zebo Peng</i>	
Low-Cost Sub-5W Processors for Edge HPC	529
<i>Pedro Trancoso and Michalis Efstathiou</i>	
A Methodology for Predicting Application-Specific Achievable Memory Bandwidth for HW/SW-Codesign	533
<i>Matthias Göbel, Ahmed Elhossini, and Ben Juurlink</i>	
Adaptive Reliability for Fault Tolerant Multicore Systems	538
<i>Ihsen Alouani, Thomas Wild, Andreas Herkersdorf, and Smail Niar</i>	
High-Performance General-Purpose Arithmetic Operations Using the Massive Parallel DNA-Based Computation	543
<i>Mercedeh Sanjabi, Ali Jahanian, and Maryam Tahmasebi</i>	
Optimal Placement of Heterogeneous Uncore Component in 3D Chip-Multiprocessors	547
<i>Aniseh Dorostkar, Arghavan Asad, Mahmood Fathy, and Farah Mohammadi</i>	
Author Index	552