

2017 47th European Solid-State Device Research Conference (ESSDERC 2017)

**Leuven, Belgium
11-14 September 2017**



**IEEE Catalog Number: CFP17543-POD
ISBN: 978-1-5090-5979-9**

**Copyright © 2017 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP17543-POD
ISBN (Print-On-Demand):	978-1-5090-5979-9
ISBN (Online):	978-1-5090-5978-2
ISSN:	1930-8876

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

ESSDERC 2017 Table of Contents

A1L-A Joint Plenary 1: Françoise Chombar, Melexis - Engineering a Safe, Clean & Comfortable Future

Date: Tuesday, September 12, 2017
Time: 09:00 - 09:40
Room: Vesalius
Chair(s): Georges Gielen; *KU Leuven*

Engineering a Safe, Clean & Comfortable FutureNo paper
Françoise Chombar
Melexis, Belgium

A2L-A Joint Plenary 2: Peter Real, Analog Devices - Navigating without a Moore's Law Compass

Date: Tuesday, September 12, 2017
Time: 09:40 - 10:20
Room: Vesalius
Chair(s): Georges Gielen; *KU Leuven*

Navigating Without a Moore's Law CompassNo paper
Peter Real
Analog Devices Inc, Ireland

B1L-A Joint Plenary 3: Hans Stork, ON Semiconductor - Smart Power for Automotives

Date: Wednesday, September 13, 2017
Time: 08:45 - 09:25
Room: Vesalius
Chair(s): Jo De Boeck; *imec*

Smart Power for AutomotivesNo paper
Johannes Stork
ON Semiconductor, United States

C1L-A Joint Plenary 4: Tetsuo Endoh, Tohoku University – Spintronics Applications: STT-MRAM & Non Volatile Logic

Date: Thursday, September 14, 2017
Time: 09:00 - 09:40
Room: Vesalius
Chair(s): Jo De Boeck; *imec*

Spintronics Applications: STT-MRAM and Non Volatile LogicNo paper
Tetsuo Endoh
Tohoku University, Japan

A5L-F ESSDERC Keynote 1: Ian Young - Principles & Trends in Quantum Nano-Electronics & Nano-Magnetics for Beyond-CMOS Computing

Date: Tuesday, September 12, 2017
Time: 15:50 - 16:30
Room: AP01.30
Chair(s): Marc Heyns; *imec*

Principles and Trends in Quantum Nano-Electronics and Nano-Magnetics for Beyond-CMOS Computing 1

Ian A. Young, Dmitri E. Nikonov
Intel Corp., United States

B3L-F ESSDERC Keynote 2: Siva Sivaram - Storage Class Memories: Desire Meets Reality

Date: Wednesday, September 13, 2017
Time: 13:30 - 14:10
Room: AP01.30
Chair(s): Bogdan Govoreanu; *imec*

Storage Class Memories: Desire Meets RealityNo paper

Siva Sivaram
Western Digital Corporation, United States

C3L-F ESSDERC Keynote 3: David DiVincenzo - Control Systems for Quantum Computers

Date: Thursday, September 14, 2017
Time: 13:30 - 14:10
Room: AP01.30
Chair(s): Guido Groeseneken; *imec*

Control Systems for Quantum ComputersNo paper

David DiVincenzo
RWT Aachen, Germany

A3L-F Resistive RAM

Date: Tuesday, September 12, 2017
Time: 11:00 - 12:20
Room: AP01.30
Chair(s): Thomas Mikolajick; *NaMLab gGmbH*
Paolo Pavan; *Università di Modena e Reggio Emilia*

22% Higher Performance, 2x SCM Write Endurance Heterogeneous Storage with Dual Storage Class Memory and NAND Flash 6

Chihiro Matsui, Ken Takeuchi
Chuo University, Japan

Study of Error Repeatability and Recovery in 40nm TaOx ReRAM 10

Takashi Inose¹, Seiichi Aritome¹, Ryutaro Yasuhara², Satoshi Mishima², Ken Takeuchi¹
¹*Department of Electrical, Electronic, and Communication Engineering, Chuo University, Tokyo, Japan, Japan;* ²*Panasonic Semiconductor Solutions Co., Ltd., 1 Kotari-yakemachi, Nagaokakyo, Kyoto, Japan, Japan*

Optimization of Writing Scheme on 1T1R RRAM to Achieve Both High Speed and Good Uniformity..... 14

Shan Wang, Huaqiang Wu, Bin Gao, Ning Deng, Dong Wu, He Qian
Tsinghua University, China

Analyzing Inference Robustness of RRAM Synaptic Array in Low-Precision Neural Network..... 18

Rui Liu¹, Heng-Yuan Lee², Shimeng Yu¹
¹*Arizona State University, United States;* ²*Electronics and Optoelectronics Research Laboratory, Industrial Technology Research Institute, Taiwan*

A3L-G Cross-Domain Compact Modelling

Date: Tuesday, September 12, 2017

Time: 11:00 - 12:20

Room: AV00.17

Chair(s): Wlodek Grabinski; 0

Cristell Maneux; *Laboratoire de l'Intégration du Matériau au Système*

INVITED: SPICE Modeling in Verilog-A: Successes and Challenges 22

Colin McAndrew

NXP Semiconductors, United States

SPICE Modeling of Light Induced Current in Silicon with 'Generalized' Lumped Devices 26

Chiara Rossi², Pietro Buccella², Camillo Stefanucci¹, Jean-Michel Sallese²

¹*AMS, AG, Schloss Premstaetten, Austria;* ²*École Polytechnique Fédérale de Lausanne (EPFL), Switzerland*

Total Ionizing Dose Effects on Analog Performance of 28 nm Bulk MOSFETs 30

Chun-Min Zhang³, Farzan Jazaeri³, Alessandro Pezzotta³, Claudio Bruschini³, Gulio

Borghello², Serena Mattiazzo¹, Andrea Baschiroto⁴, Christian Enz³

¹*Department of Information Engineering, University of Padova, Italy;* ²*EP-ESE Group, CERN and University of Udine, Switzerland;* ³*Integrated Circuits Laboratory, École Polytechnique Fédérale de Lausanne, Switzerland;* ⁴*Microelectronic Group, INFN Milano-Bicocca and University of Milano-Bicocca, Italy*

A3L-H Focus Session: Beyond CMOS Devices I

Date: Tuesday, September 12, 2017

Time: 11:00 - 12:20

Room: AV02.17

Chair(s): Joachim Knoch; *Rheinisch-Westfälische Technische Hochschule Aachen*
Thomas Zimmer; *Laboratoire de l'Intégration du Matériau au Système*

1/f Noise in 3D Vertical Gate-All-Around Junction-Less Silicon Nanowire

Transistors 34

Chhandak Mukherjee¹, Julien Pezard², Guilhem Larrieu², Cristell Maneux¹

¹IMS Laboratory, University of Bordeaux, France; ²LAAS-CNRS, Université de Toulouse
CNRS, INP, Toulouse, France

Random Telegraph Signal Noise in Tunneling Field-Effect Transistors with S

Below 60 mV/decade..... 38

Markus Hellenbrand, Elvedin Memišević, Johannes Svensson, Erik Lind, Lars-Erik
Wernersson

Lund University, Sweden

Experimental Characterization of the Static Noise Margins of Strained Silicon

Complementary Tunnel-FET SRAM 42

Gia Vinh Luong¹, Sebastiano Strangio², Andreas Tiedemann¹, Patrick Bernardy¹, Stefan
Trellenkamp¹, Pierpaolo Palestri², Siegfried Mantl¹, Qing-Tai Zhao¹

¹Forschungszentrum Juelich, Germany; ²University of Udine, Italy

A4L-F Alternative Device Simulations

Date: Tuesday, September 12, 2017

Time: 14:00 - 15:20

Room: AP01.30

Chair(s): Francois Triozon; *Commissariat à l'Energie Atomique et aux Energies Alternatives*
Fabian Bufler; *Synopsys, Inc.*

INVITED: Advances in the Understanding of Microscopic Switching Mechanisms in ReRAM Devices..... 46

Benoît Sklénard¹, Philippe Blaise¹, Boubacar Traoré², Alberto Dragoni¹, Cécile Nail¹,
Elisa Vianello¹

¹CEA LETI, France; ²Institut des Sciences Chimiques de Rennes, France

Modeling the Effect of Surface Roughness on the Performance of Line Tunnel Fets 50

Saurabh Sant, Andreas Schenk

Integrated Systems Laboratory, ETH Zurich, Switzerland

Material Selection and Device Design Guidelines for Two-Dimensional Material Based TFETs 54

Tarun Agarwal³, Bart Soree³, Iuliana Radu¹, Praveen Raghavan¹, Gianluca Fiori⁴, Marc
Heyns³, Wim Dehaene²

¹imec, Belgium; ²KU Leuven, Belgium; ³KU Leuven/imec, Belgium; ⁴Univ of Pisa, Italy

A4L-G Parameter Extraction

Date: Tuesday, September 12, 2017

Time: 14:00 - 15:20

Room: AV00.17

Chair(s): Thierry Poiroux; *Commissariat à l'Energie Atomique et aux Energies Alternatives*
Marco Bellini; *ABB Group*

Nanometer CMOS Characterization and Compact Modeling at Deep-Cryogenic Temperatures 58

Rosario Marco Incandela¹, Lin Song², Harald Homulle¹, Fabio Sebastiano¹, Edoardo Charbon¹, Andrei Vladimirescu¹

¹*Delft University of Technology, Netherlands*; ²*Tsinghua University, China*

Cryogenic Characterization of 28 nm Bulk CMOS Technology for Quantum Computing 62

Arnout Beckers³, Farzan Jazaeri³, Andrea Ruffino¹, Claudio Bruschini², Andrea Baschiroto⁴, Christian Enz³

¹*EPFL AQUA, Switzerland*; ²*EPFL AQUA-ICLAB, Switzerland*; ³*EPFL ICLAB, Switzerland*; ⁴*INFN Milano Bicocca, Italy*

A New Method for Junctionless Transistors Parameters Extraction..... 66

Renan Trevisoli², Rodrigo Doria², Michelly de Souza², Sylvain Barraud¹, Marcelo Pavanello²

¹*CEA, LETI, Minatec Campus, France*; ²*Centro Universitário FEI, Brazil*

Avalanche Compact Model Featuring SiGe HBTs Characteristics Up to BVCBO 70

Mathieu Jaoul⁵, Didier Céli⁴, Cristell Maneux³, Michael Schröter², Andreas Pawlak¹

¹*Dresden University of Technology, Germany*; ²*Dresden University of Technology, University of California, Germany*; ³*IMS Bordeaux, France*; ⁴*STMicroelectronics, France*; ⁵*STMicroelectronics, IMS, France*

A4L-H Focus Session: Beyond CMOS Devices II

Date: Tuesday, September 12, 2017

Time: 14:00 - 15:20

Room: AV02.17

Chair(s): Joachim Knoch; *Rheinisch-Westfälische Technische Hochschule Aachen*
Thomas Zimmer; *Laboratoire de l'Intégration du Matériau au Système*

Utilizing I-V Non-Linearity and Analog State Variations in ReRAM-Based Security

Primitives 74

Gina Cristina Adam¹, Hussein Nili³, Jeesson Kim², Brian Douglas Hoskins³, Omid Kavehei², Dmitri Strukov³

¹*National Institute for R&D in Microtechnologies, Bucharest, Romania;* ²*RMIT University, Australia;* ³*University of California Santa Barbara, United States*

Negative Capacitance Field Effect Transistors: Capacitance Matching and Non-Hysteretic Operation 78

Ali Saeidi, Farzan Jazaeri, Francesco Bellando, Igor Stolichnov, Christian Enz, Adrian Ionescu

Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland

Buried Multi-Gate InAs-Nanowire FETs 82

Thomas Grap, Felix Riederer, Charu Gupta, Joachim Knoch
RWTH Aachen, Germany

A6L-G Modelling of Emerging Devices

Date: Tuesday, September 12, 2017

Time: 16:40 - 18:00

Room: AV00.17

Chair(s): Jean-Michel Sallese; *École polytechnique fédérale de Lausanne*
Daniel Tomaszewski; *Institute of Electron Technology*

Equivalent Circuit Model for the Electron Transport in 2D Resistive Switching

Material Systems..... 86

Enrique Miranda², Chengbin Pan¹, Marco Villena¹, Na Xiao¹, Jordi Suñe², Mario Lanza¹

¹Soochow University, China; ²Universitat Autònoma de Barcelona, Spain

Analytical Drain Current Model for Non-Ballistic Schottky-Barrier CNTFETs 90

Igor Bejenari, Michael Schroter, Martin Claus

Technische Universität Dresden, Germany

A General Circuit Model for Spintronic Devices Under Electric and Magnetic Fields..... 94

Meshal Alawein, Hossein Fariborzi

King Abdullah University of Science and Technology, Saudi Arabia

Compact Physical Model of a-IGZO TFTs for Circuit Simulation..... 98

Matteo Ghittorelli³, Fabrizio Torricelli³, Carmine Garripoli², Jan-Laurens van der Steen¹,
Gerwin Gelinck¹, Sahel Abdinia², Eugenio Cantatore², Zsolt Kovács-Vajna³

¹TNO, Netherlands; ²Tu/e, Netherlands; ³University of Brescia, Italy

A6L-H 2D Material Devices

Date: Tuesday, September 12, 2017
Time: 16:40 - 18:00
Room: AV02.17
Chair(s): Cees de Groot; *University of Southampton*
Gianluca Fiori; *Università di Pisa*

Complementary Black Phosphorous FETs by Workfunction Engineering of Pre-Patterned Au and Ag Embedded Electrodes..... 102

Nicolo Oliva, Emanuele Andrea Casu, Wolfgang Amadeus Vitale, Igor Stolichnov, Adrian Mihai Ionescu
EPFL, Switzerland

Tunneling Transistors Based on MoS₂/MoTe₂ Van der Waals Heterostructures..... 106

Yashwanth Balaji, Quentin Smets, Cesar J Lockhart de la Rosa, Anh Khoa Augustin Lu, Daniele Chiappe, Tarun Agarwal, Dennis Lin, Cedric Huyghebaert, Iuliana Radu, Dan Mocuta, Guido Groeseneken
imec, Belgium

Temperature Dependence of Contact Resistance for Gold-Graphene Contacts..... 110

Amit Gahoi, Satender Kataria, Max Christian Lemme
University of Siegen, Germany

Radical Oxidation Process for Hybrid SAM/HfO_x Gate Dielectrics in MoS₂ FETs 114

Takamasa Kawanago, Ryo Ikoma, Tomoaki Oba, Hiroyuki Takagi
Tokyo Institute of Technology, Japan

B2L-F Widebandgap Power Devices

Date: Wednesday, September 13, 2017

Time: 10:10 - 11:50

Room: AP01.30

Chair(s): Mikael Ostling; *KTH Royal Institute of Technology*
Susanna Reggiani; *Università di Bologna*

INVITED: CoolSiC(TM) and Major Trends in SiC Power Device Development 118

Roland Rupp

Infineon Technologies AG, Germany

Gated Base Structure for Improved Current Gain in SiC Bipolar Technology..... 122

Gunnar Malm, Hossein Elahipanah, Arash Salemi, Mikael östling

KTH, Sweden

On the Understanding of Cathode Related Trapping Effects in GaN-on-Si Schottky

Diodes 126

William Vandendaele, Thomas Lorin, Romain Gwoziecki, Yannick Baines, Jérôme Biscarrat, Marie-Anne Jaud, Charlotte Gillot, Matthew Charles, Marc Plissonnier, Gilles Reimbold

CEA-LETI, France

Temperature Dependent Substrate Trapping in AlGaIn/GaN Power Devices and the Impact on Dynamic Ron..... 130

Arno Stockman², Michael Uren⁴, Alaleh Tajalli⁵, Matteo Meneghini⁵, Benoit Bakeroot¹, Peter Moens³

¹CMST imec/Ghent University, Belgium; ²Ghent University, Belgium; ³ON Semiconductor, Belgium; ⁴University of Bristol, United Kingdom; ⁵University of Padova, Italy

B2L-G Advanced CMOS Characterization and Reliability

Date: Wednesday, September 13, 2017

Time: 10:10 - 12:10

Room: AV00.17

Chair(s): Erik Bury; *imec*
Maryline Bawedin; *Minatec*

INVITED: Material and Device Innovation Impact on Reliability for Scaled CMOS Technologies 134

Tanya Nigam, Andreas Kerber, Tian Shen, Rakesh Ranjan, Linjun Cao
GLOBALFOUNDRIES, United States

Carrier Lifetime Evaluation in FD-SOI Layers 140

Kyung Hwa Lee, Maryline Bawedin, Hyungjin Park, Mukta Singh Parihar, Sorin Cristoloveanu
IMEP-LAHC, France

Precise EOT Regrowth Extraction Enabling Performance Analysis of Low Temperature Extension First Devices 144

Jessy Micout², Quentin Raffay³, Xavier Garros¹, Mikael Casse¹, Jean Coignus¹, Luca Pasini¹, Cao-Minh Vincent Lu¹, Nils Rambal¹, Claire Fenouillet-Beranger¹, Laurent Brunet¹, Giovannii Romana⁴, Rémy Gassilloud¹, Perrine Batude¹, Maud Vinet¹, Gérard Ghibaudo³

¹CEA-LETI, France; ²CEA-LETI, IMEP-LAHC, France; ³IMEP-LAHC, France;

⁴STMicroelectronics, France

Back-Gate Bias Effect on UTBB-FDSOI Non-Linearity Performance 148

Babak Kazemi Esfeh³, Valeria Kilchytska³, Bertrand Parvais¹, N. Planes², M. Haond², Denis Flandre³, Jean-Pierre Raskin³

¹imec, Belgium; ²ST-Microelectronics, France; ³UCL, Belgium

Evolution of Oxygen Vacancies Under Electrical Characterization for HfOx-Based ReRAMs 152

Behnoush Attarimashalkoubek, Jury Sandrini, Elmira Shahrabi, Yusuf Leblebici
Microelectronic Systems Laboratory (LSM), EPFL, Switzerland

B2L-H Emerging Memory Technologies

Date: Wednesday, September 13, 2017

Time: 10:10 - 12:10

Room: AV02.17

Chair(s): Jerome Dubois; *NXP*
Dirk Wouters; *RWTH Aachen*

INVITED: Emerging Memory Technologies for High Density Applications..... 156

Giorgio Servalli

Micron Technology, Italy

Anti-Ferroelectric ZrO₂: An Enabler for Low Power Non-Volatile 1T-1C and 1T Random Access Memories..... 160

Milan Pesic², Michael Hoffmann², Claudia Richter², Stefan Slesazeck², Thomas

Kämpfe¹, Lukas Eng¹, Thomas Mikolajick³, Uwe Schroeder²

¹*IAPP/TU Dresden, Germany*; ²*NaMLab gGmbH, Germany*; ³*NaMLab gGmbH/TU Dresden, Germany*

From Planar to Vertical Capacitors : a Step Towards Ferroelectric V-FET Integration..... 164

Karine Florent², Simone Lavizzari¹, Luca Di Piazza¹, Mihaela Popovici¹, Goedele

Potoms¹, Tom Raymaekers¹, Guido Groeseneken², Jan Van Houdt²

¹*imec, Belgium*; ²*imec/KU Leuven, Belgium*

Doped GeSe Materials for Selector Applications..... 168

Naga Sruti Avasarala³, Bogdan Govoreanu², Karl Opsomer², Wouter Devulder², Sergiu

Clima², Christophe Detavernier¹, Marleen van der Veen², Jan Van Houdt³, Marc Heyns³,

Ludovic Goux², Gouri Sankar Kar²

¹*Ghent University, Belgium*; ²*imec, Belgium*; ³*imec, KU Leuven, Belgium*

Multilevel SOT-MRAM Cell with a Novel Sensing Scheme for High-Density Memory Applications..... 172

Behzad Zeinali, Mahsa Esmaeili, Jens Kargaard Madsen, Farshad Moradi

Aarhus University, Denmark

B4L-F FinFET and Nanowire Simulations

Date: Wednesday, September 13, 2017
Time: 14:20 - 15:40
Room: AP01.30
Chair(s): Bernd Meinerzhagen; *TU Braunschweig*
Mathieu Luisier; *ETHZ*

On the Ballistic Ratio in 14nm-Node FinFETs 176

Fabian Bufler, Kenichi Miyaguchi, Thomas Chiarella, Naoto Horiguchi, Anda Mocuta
imec, Belgium

Three-Dimensional Multi-Subband Simulation of Scaled FinFETs 180

Luca Donetti, Carlos Sampedro, Francisco García Ruiz, Andrés Godoy, Francisco Gámiz
Universidad de Granada, Spain

Study of Strained Effects in Nanoscale GAA Nanowire FETs Using 3D Monte Carlo Simulations..... 184

Muhammad Elmessary¹, Daniel Nagy², Manuel Aldegunde³, Antonio Garcia-Loureiro², Karol Kalna¹
¹*Swansea University, United Kingdom*; ²*Universidade de Santiago de Compostela, Spain*; ³*University of Notre Dame, United States*

Investigation of Electrically Gate-All-Around Hexagonal Nanowire FET (HexFET) for 5nm Node Logic and SRAM Applications..... 188

Jeffrey Smith², Kai Ni², Ram Krishna Ghosh², Jeff Xu¹, Mustafa Badaroglu¹, Pr Chidi Chidambaram¹, Suman Datta²
¹*Qualcomm, United States*; ²*University of Notre Dame, United States*

B4L-G Traps and Noise

Date: Wednesday, September 13, 2017

Time: 14:20 - 15:40

Room: AV00.17

Chair(s): Benjamin Iniguez; *Universitat Rovira i Virgili*
Sadayuki Yoshitomi; *Toshiba*

Modeling of Dynamic Trap Density Increase for Aging Simulation of Any MOSFET Circuits..... 192

Mitiko Miura-Mattausch³, Hidenori Miyamoto³, Hideyuki Kikuchiara³, Dondee Navarro³, Tapas K. Maiti³, Nezam Rohbani⁴, Chenyue Ma², Hans Juergen Mattausch³, Alexander Schiffmann¹, Alexander Steinmair¹, Ehrenfried Seebacher¹
¹ams, Austria; ²ASTRI, Hong Kong; ³Hiroshima University, Japan; ⁴Sharif University, Iran

Comprehensive Compact Electro-Thermal GaN HEMT Model..... 196

Muhammad Alshahed, Mina Dakran, Lars Heuken, Mohammed Alomari, Joachim Burghartz
IMS CHIPS, Germany

Trap-Assisted Carrier Transport Through the Multi-Stack Gate Dielectrics of HKMG nMOS Transistors: a Compact Model 200

Apoorva Ojha, Nihar Ranjan Mohapatra
IIT Gandhinagar, India

A New Verilog-A Compact Model of Random Telegraph Noise in Oxide-Based RRAM for Advanced Circuit Design..... 204

Francesco Maria Puglisi, Nicolò Zagni, Luca Larcher, Paolo Pavan
Università di Modena e Reggio Emilia, Italy

B4L-H 2D Material Integration

Date: Wednesday, September 13, 2017

Time: 14:20 - 15:40

Room: AV02.17

Chair(s): Thomas Ernst; *Commissariat à l'Energie Atomique et aux Energies Alternatives*
Max Lemme; *Universität Siegen*

INVITED: Ink-Jet Printed 2D Crystal Heterostructures 208

Francesco Bonaccorso

Istituto Italiano di Tecnologia, Italy

WS2 Transistors on 300 mm Wafers with BEOL Compatibility..... 212

Tom Schram², Quentin Smets², Benjamin Groven², Markus Heyne², Eddy Kunnen²,
Arame Thiam², Katia Devriendt², Annelies Delabie², Dennis Lin², Marcel Lux², Daniele
Chiappe², Inge Asselberghs², Stephan Brus², Cedric Huyghebaert², Safak Sayan², A.
Juncker¹, Matty Caymax², Iuliana Radu²

¹COVENTOR, France; ²imec, Belgium

200 mm Wafer Level Graphene Transfer by Wafer Bonding Technique 216

Mesut Inac¹, Grzegorz Lupina², Matthias Wietstruck², Marco Lisker², Mirko Fraschke²,
Andreas Mai², Fabio Coccetti³, Mehmet Kaynak²

¹Berlin Technical University, Germany; ²IHP, Germany; ³RF Microtech, Italy

C2L-E Focus Session: Neuromorphic Computing

Date: Thursday, September 14, 2017

Time: 10:00 - 12:00

Room: AV03.12

Chair(s): Cor Claeys; *imec*

INVITED: Neuromorphic Computing: Architectures and Applications.....No paper

Karlheinz Meier

University of Heidelberg, Germany

INVITED: RRAM: Does It Have the Potential for Neuromorphic ComputationNo paper

Praveen Raghavan

imec, Belgium

C2L-F Photonics / Microwave / Harsh Environment

Date: Thursday, September 14, 2017
Time: 10:20 - 12:00
Room: AP01.30
Chair(s): Denis Flandre; *Université catholique de Louvain*
Dana Cristea; *IMT Bucharest*

Epitaxial Growth and Diffusion Characteristics Analysis of Vertical Thin Poly-Si Channel Transfer Gate Structured Pixels for 3D CMOS Image Sensor 220

Sung-Kun Park², Donghyun Woo², Min-Ki Na², Pyong-Su Kwag², Ho-Ryeong Lee²,
Kyoung-Wook Ro², Kyung-Hwan Kim², Dong-Kyu Lee², Chris Hong², In-Wook Cho²,
Kyung-Dong Yoo¹

¹Hanyang University, Korea; ²SK hynix, Korea

Modelling, Design and Characterization of Schottky Diodes in 28nm Bulk CMOS for 850/1310/1550nm Fully Integrated Optical Receivers 224

Wouter Diels, Michiel Steyaert, Filip Tavernier
KULeuven, Belgium

Importance of Buffer Configuration in GaN HEMTs for High Microwave Performance and Robustness 228

Romain Pecheux, Riad Kabouche, Ezgi Dogmus, Astrid Linge, Etienne Okada, Malek Zegaoui, Farid Medjdoub
IEMN-CNRS, France

Shunt Capacitive Switches Based on VO₂ Metal Insulator Transition for RF Phase Shifter Applications 232

Emanuele Andrea Casu, Wolfgang Amadeus Vitale, Michele Tamagnone, Mariazel Maqueda Lopez, Nicolò Oliva, Anna Krammer, Andreas Schöler, Montserrat Fernandez-Bolaños, Adrian Mihai Ionescu
EPFL, Switzerland

Single Event Effects and Total Ionising Dose in 600V Si-on-SiC LDMOS Transistors for Rad-Hard Space Applications 236

Khaled Ben Ali³, Peter Gammon⁴, Chunwa Chan⁴, Fan Li⁴, Vasantha Pathirana¹, Tanya Trajkovic¹, Farzan Gity², Denis Flandre³, Valeriya Kilchytska³

¹Cambridge Microelectronics Limited, United Kingdom; ²Tyndall National Institute at University of Ireland, Ireland; ³Université catholique de Louvain, Belgium; ⁴University of Warwick, United Kingdom

C2L-G Advanced CMOS Technology

Date: Thursday, September 14, 2017

Time: 10:00 - 12:00

Room: AV00.17

Chair(s): Francois Andrieu; *Commissariat à l'Energie Atomique et aux Energies Alternatives*
Blandine Duriez; *TSMC*

PPAC Scaling Enablement for 5nm Mobile SoC Technology..... 240

Mustafa Badaroglu⁴, Jeff Xu⁴, John Zhu⁴, Da Yang⁴, Jerry Bao⁴, Sc Song⁴, Peijie Feng⁴,
Romain Ritzenthaler³, Hans Mertens³, Geert Eneman³, Naoto Horiguchi³, Jeffrey Smith⁵,
Suman Datta⁵, David Kohen², Po-Wen Chan¹, Keagan Chen¹, Chidi Chidambaram⁴

¹*Applied Materials, United States*; ²*ASM International, Belgium*; ³*imec, Belgium*;

⁴*Qualcomm Technologies Inc., Belgium*; ⁴*Qualcomm Technologies Inc., United States*;

⁵*University of Notre Dame, United States*

INVITED: Hybrid InGaAs/SiGe CMOS Circuits with 2D and 3D Monolithic Integration 244

Veeresh Deshpande, Herwig Hahn, Vladimir Djara, Eamon O'Connor, Daniele Caimi,
Marilyne Sousa, Jean Fompeyrine, Lukas Czornomaz
IBM Research GmbH, Switzerland

Tunable ESD Clamp for High-Voltage Power I/O Pins of a Battery Charge Circuit in Mobile Applications 248

Mirko Scholz, Geert Hellings, Shih-Hung Chen, Dimitri Linten
imec, Belgium

Guidelines for Intermediate Back End of Line (BEOL) for 3D Sequential Integration 252

Claire Fenouillet-Beranger¹, Sylvain Beaurepaire¹, Fabien Deprat¹, Alexandre Ayeres de Sousa¹, Laurent Brunet¹, Perrine Batude¹, Paul Besombes¹, Marie-Pierre Samson²,
Fabrice Nemouchi¹, François Andrieu¹, Romain Famulok¹, Nils Rambal¹, Viorel Balan¹,
Vincent Jousseau¹, Vincent Delaye¹, Xavier Federspiel², Maud Vinet¹, O. Rozeau¹, B. Previtali¹, G. Rodriguez¹, P. Rodriguez¹, Z. Saghi¹, C. Guerin¹, F. Ibars², F. Proud², D. Nougier², D. Ney², H. Dansas¹

¹*CEA/LETI, France*; ²*STMicroelectronics, France*

Device Circuit and Technology Co-Optimisation for FinFET Based 6T SRAM Cells Beyond N7 256

Mohit Gupta², Pieter Weckx¹, Stefan Cosemans¹, Pieter Schuddinck¹, Rogier Baert¹,
Dmitry Yakimets¹, Doyoung Jang¹, Yasser Sherazi¹, Praveen Raghavan¹, Alessio Spessot¹, Anda Mocuta¹, Wim Dehaene²

¹*imec, Belgium*; ²*KU Leuven/imec, Belgium*

C2L-H Microfluidics and TFTs

Date: Thursday, September 14, 2017

Time: 10:00 - 12:00

Room: AV02.17

Chair(s): Montserrat Fernandez-Bolanos; *École Polytechnique Fédérale de Lausanne*
Joachim Burghartz; *IMS Chips*

INVITED: Microfluidic Technology: New Opportunities to Develop Physiologically Relevant in vitro Models 260

Séverine Le Gac

University of Twente, Netherlands

Development of Ultrasensitive Extended-Gate Ion-Sensitive-Field-Effect-Transistor Based on Industrial UTBB FDSOI Transistor 264

Getenet Tesega Ayele³, Stephane Monfray⁴, Frederic Boeuf⁴, Jean-Pierre Cloarec¹, Serge Ecoffey³, Dominique Drouin³, Etienne Puyoo², Abdelkader Souifi²

¹Ecole Central de Lyon, France; ²INSA Lyon, France; ³Sherbrooke University, Canada;

⁴STMicroelectronics, France

Ultrathin Lateral Unidirectional Bipolar-Type Insulated-Gate Transistor as pH Sensor 268

Qinghua Han¹, Anran Gao¹, Keyvan Narimani¹, Yuelin Wang², Tie Li², Siegfried Mantl¹, Qing-Tai Zhao¹

¹Forschungszentrum Jülich, Germany; ²Shanghai Institute of Microsystem and Information Technology, China

A Novel Approach for Scalable Sensor Arrays Using Cantilever Field-Effect Transistors 272

Andreas Hessel, Stefan Scholz, Alexander Pelger, Albert Pfander, Joachim Knoch
RWTH Aachen University, Germany

ESD Characterization of a-IGZO TFTs on Si and Foil Substrates 276

Nian Wang³, Shih-Hung Chen¹, Geert Hellings¹, Kris Myny¹, Soeren Steudel¹, Mirko Scholz¹, Roman Boschke², Dimitri Linten¹, Guido Groeseneken²

¹imec, Belgium; ²imec, KULeuven, Belgium; ³KULeuven, imec, Belgium

C4L-F Modelling and Measurement of Alternative Material Devices

Date: Thursday, September 14, 2017
Time: 14:20 - 15:40
Room: AP01.30
Chair(s): Denis Rideau; *STMicroelectronics*
Massimo Rudan; *Università di Bologna*

INVITED: Dopant Diffusion and Segregation, Si-Ge Interdiffusion and Defect Engineering in SiGe Devices 280

Guangrui Xia
University of British Columbia, Canada

Physical Modeling of the Hysteresis in MoS₂ Transistors 284

Theresia Knobloch², Gerhard Rzepa², Yury Yuryevich Illarionov², Michael Waltl², Franz Schanovsky¹, Markus Jech², Bernhard Stampfer², Marco Mercurio Furchi³, Thomas Müller³, Tibor Grasser²

¹*Global TCAD Solutions, Bösendorferstraße 1/12, 1010 Wien, Austria;* ²*Institute for Microelectronics, TU Wien, Gußhausstraße 27–29/E360, 1040 Wien, Austria;* ³*Institute for Photonics, TU Wien, Gußhausstraße 27–29/E387, 1040 Wien, Austria*

Impact of Impurities, Interface Traps and Contacts on MoS₂ MOSFETs: Modelling and Experiments 288

Gioele Mirabelli, Farzan Gity, Scott Monaghan, Paul Hurley, Ray Duffy
Tyndall National Institute, University College Cork, Ireland

C4L-G High Mobility Materials and Nanowires

Date: Thursday, September 14, 2017

Time: 14:20 - 15:40

Room: AV00.17

Chair(s): Lukas Czornomaz; *IBM Zurich*
Nadine Collaert; *imec*

Electron Mobility in Thin In_{0.53}Ga_{0.47}As Channel..... 292

Eduard Cartier, Amlan Majumdar, Ko-Tao Lee, Takashi Ando, Martin M Frank, John Rozen, Keith A Jenkins, Cheng-Wei Cheng, John Bruley, Marinus Hopstaken, Pranita Kerber, Jeng-Bang Yau, Xiao Sun, Renee T Mo, Chun-Chen Yeh, Effendi Leobandung, Vijay Narayanan, C. Liang
IBM Corporation, United States

Understanding of Slow Traps Generation in Plasma Oxidation GeO_x/Ge MOS Interfaces with ALD High-K Layers 296

Mengnan Ke, Mitsuru Takenaka, Shinichi Takagi
the University of Tokyo, Japan

Isolation of Nanowires Made on Bulk Wafers by Ground Plane Doping 300

Romain Ritzenthaler, Hans Mertens, An de Keersgieter, Jerome Mitard, Dan Mocuta, Naoto Horiguchi
imec, Belgium

In-Depth Electrical Characterization of Carrier Transport in Ambipolar Si-NW Schottky-Barrier FETs 304

Dae-Young Jeon², Tim Baldauf⁵, So Jeong Park³, Sebastian Pregl⁴, Larysa Baraban¹, Gianaurelio Cuniberti¹, Thomas Mikolajick⁴, Walter M. Weber⁴

¹*Institute for Materials Science and Max Bergmann Center of Biomaterials, Germany;*

²*KIST, Jeonbuk, Korea;* ³*Korea University, Korea;* ⁴*Namlab gGmbH, Germany;*

⁵*University of Applied Sciences Dresden, Germany*

C4L-H Focus Session: Quantum Computing

Date: Thursday, September 14, 2017

Time: 14:20 - 15:40

Room: AV02.17

Chair(s): Iuliana Radu; *imec*

INVITED: Superconducting Qubit Research at ChalmersNo paper

Jonas Bylander

Chalmers University, Sweden

INVITED: A 'Spins Inside' Quantum ProcessorNo paper

Juan Pablo Dehollain

TU Delft, Netherlands