

2017 Austrochip Workshop on Microelectronics (Austrochip 2017)

**Linz, Austria
12 October 2017**



IEEE Catalog Number: CFP17AUS-POD
ISBN: 978-1-5386-3584-1

**Copyright © 2017 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP17AUS-POD
ISBN (Print-On-Demand):	978-1-5386-3584-1
ISBN (Online):	978-1-5386-3583-4

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

2017 Austrochip Workshop on Microelectronics

Austrochip 2017

Table of Contents

Message from the Organizing Committeevii
Workshop Organization.....	.viii
Patrons.....	.ix
Technical Co-Sponsors.....	.x

Device Modelling and Verification

Analysis of Semiconductor Process Variations by Means of Hierarchical Median Polish	1
<i>Benjamin Willsch, Julia Hauser, Stefan Dreiner, Andreas Goehlich, Holger Kappert, and Holger Vogt</i>	
DC/AC Compact Modeling of TFETs for Circuit Simulation of Logic Cells Based on an Analytical Physics-Based Framework	6
<i>Fabian Horst, Atieh Farokhnejad, Michael Graef, Fabian Hosenfeld, Gia Vinh Luong, Chang Liu, Qing-Tai Zhao, Francois Lime, Benjamin Iniguez, and Alexander Kloes</i>	

RF Integrated Circuit Design

A Compact, Low Power and High Sensitivity E-Band Frequency Divider SiGe HBT MMIC	11
<i>Aleksey Dyskin, Parisa Harati, and Ingmar Kallfass</i>	
CMOS Open-Loop Local Quadrature Phase Generator for 5G Applications	15
<i>Michael Kalcher and Daniel Gruber</i>	
Receiver Chip in 0.6µm BiCMOS with AGC and LVDS Output Driver	18
<i>Bernhard Goll, Robert Swoboda, and Horst Zimmermann</i>	
A Circuit Technique for Blocker-Induced Modulated Spur Cancellation in 4G LTE Carrier Aggregation Transceivers	23
<i>Silvester Sadjina, Dufrene Krzysztof, Ram Sunil Kanumalli, Mario Huemer, and Harald Pretl</i>	
A Review of Ultra-Low-Power and Low-Cost Transceiver Design	29
<i>Tim Schumacher, Markus Stadelmayer, Thomas Faseth, and Harald Pretl</i>	

Digital Circuit Design and System Verification

A FPGA-Based Demonstrator for Safety-Critical Applications	35
<i>Christian Fibich, Peter Röessler, Stefan Tauner, Martin Matschnig, and Herbert Taucher</i>	
Using Python Tools to Assist Mixed-Signal ASIC Design and Verification Methodologies	41
<i>Evangelos Logaras and Andreas Weitzer</i>	

Analog and Mixed-Signal Circuit Design

Implementation of a Charge-Controlled Stimulation Method in a Monolithic Integrated CMOS-Chip for Excitation of Retinal Neuron Cells	47
<i>Reinhard Viga, Peter Walter, Rainer Kokozinski, and Anton Grabmaier</i>	
Measurement and Comparison of Several Pass Transistor Logic Styles in a 350nm Technology	53
<i>Andreas Rauchenecker and Timm Ostermann</i>	
Implementation of an Integrated Differential Readout Circuit for Transistor-Based Physically Unclonable Functions	58
<i>Benjamin Willsch, Kai-Uwe Müller, Qi Zhang, Julia Hauser, Stefan Dreiner, Alexander Stanitzki, Holger Kappert, Rainer Kokozinski, and Holger Vogt</i>	
Survey on Integrated High-Power Low-Emission Output Stages for Drivers of Low-Frequency Resonant Loads	64
<i>Herbert Hackl, Mario Auer, and Ricardo Erckert</i>	
Author Index	70