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2017 30th IEEE International System-on-Chip Conference (SOCC)

Tuesday, September 5

Tuesday, September 5, 09:00 - 10:30

Tutorial 1A: Time Sensitive Networks for Industry 4.0

Thomas Leyrer, Texas Instruments
Room: Tegernsee

Tutorial 1B: Propelling Breakthrough Embedded Microprocessors by Means of Integrated Photonics

Dr. Davide Bertozzi, University of Ferrara, Italy, and Dr. Sébastien Rumley, Columbia University, NY, USA
Room: Chiemsee

Tuesday, September 5, 10:30 - 10:45

Coffee Break

Tuesday, September 5, 10:45 - 12:15

Tutorial 2A: Low Power Circuit Optimization for IoT

Dr. Michael Pronath, MunEDA GmbH
Room: Tegernsee

Tutorial 2B: FDSOI Design Experience and Recommendations

Herbert Preuthen, Jürgen Dirks, GLOBALFOUNDRIES Munich
Room: Chiemsee

Tuesday, September 5, 12:15 - 14:00

Lunch

Tuesday, September 5, 14:00 - 15:30

Tutorial 3A: Reliability for Industrial and Automotive Markets

Subhadeep Ghosh, Dr. Scott Martin, and Shane Stelmach, Texas Instruments
Room: Tegernsee

Tutorial 3B: IBM Q - Introduction into Quantum Computing (with live demo)

Dr. Albert Frisch, IBM R&D Lab, Böblingen, Germany
Room: Chiemsee

Tuesday, September 5, 15:30 - 15:45

Coffee Break

Tuesday, September 5, 15:45 - 17:15

Tutorial 4A: Design Automation for Labs-on-Chip: A New "Playground" for SoC Designers

Dr. Robert Wille, Johannes Kepler University, Linz, Austria, and Dr. Bing Li, Technical University of Munich, Germany
Room: Tegernsee

Tutorial 4B: The Importance of Benchmarking for charge-based and Beyond CMOS Devices

Dr. Andrew Marshall and Nishtha Sharma, University of Texas, Dallas
Room: Chiemsee

Wednesday, September 6, 08:30 - 08:45

Opening Remarks

Jürgen Becker, SOCC 2017 Conference Chair
Rooms: Tegernsee, Chiemsee, Königssee

Wednesday, September 6, 08:45 - 09:00

Technical Program Overview

Helen Li, SOCC 2017 Technical Program Co-Chair
Rooms: Tegernsee, Chiemsee, Königssee

Wednesday, September 6, 09:00 - 10:00

Wednesday Keynote I

FDSOI and FINFET for SoC developments
Gerd Teepe, Director Marketing for Europe, CMOS Platforms Business Unit, Globalfoundries
Rooms: Tegernsee, Chiemsee, Königssee

Wednesday, September 6, 10:00 - 10:15

Coffee Break

Wednesday, September 6, 10:15 - 11:15

Wednesday Keynote II

Advanced Technology for Automotive Cockpits, Industrial Human-Machine-Interface and IoT Systems - Optimization of Technology - Architecture - Design
Ron Martino, Vice President, i.MX Application Processor Product Line, NXP Semiconductor Corp., Austin, TX, USA
Rooms: Tegernsee, Chiemsee, Königssee

Wednesday, September 6, 11:30 - 12:45

W1A: Memories

Page:

Room: Tegernsee

Chair: Hai (Helen) Li (Duke University, USA)

W1B: Application Specific Designs

Rooms: Chiemsee, Königssee

Chair: Amlan Ganguly (Rochester Institute of Technology, USA)

Wednesday, September 6, 12:45 - 14:00

Lunch

Wednesday, September 6, 14:00 - 15:40

W2A: Analog-to-Digital Converters and Low-Noise Amplifiers

Room: Tegernsee

Chair: Ching-Yuan Yang (National Chung Hsing University, Taiwan)

35 14:00 A Low-pass Continuous-time Delta-Sigma Interface Circuit for Wideband MEMS Gyroscope Readout ASIC

Youngtae Yang, Jaehoon Jun and Suhwan Kim (Seoul National University, Korea)

40 14:25 A 13.5bit 1.6mW 3rd Order CT SD ADC for Integrated Capacitance Sensor Interface

Javed S Gaggatur and Gaurab Banerjee (Indian Institute of Science, India)

45 14:50 A Low Power, Programmable 12-bit Two Step SAR-Flash ADC for Signal Processing Applications

Krishna Kumar Movva (Birla Institute of Technology and Science - Pilani, Hyderabad, India); MB Srinivas (BML Munjal University, India); Mahesh Kumar Adimulam (Birla Institute of Technology and Science - Pilani, Hyderabad Campus, India)

51 15:15 Low-Noise High Input Impedance 8-Channels Chopper-Stabilized EEG Acquisition System

Guoxing Wang and Zhengnan Yan (Shanghai Jiao Tong University, P.R. China); Mohamed Atef (Assiut University & SJTU University, Egypt); Yong Lian (Shanghai Jiao Tong University, P.R. China)

W2B: Design Methodologies for SoCs

Rooms: Chiemsee, Königssee

Chair: Vivek Nautiyal (ARM Inc, USA)

56 14:00 Pin Accessibility Evaluating Model for Improving Routability of VLSI Designs

Hong-Yan Su (National Chiao Tung University, Taiwan); Shinichi Nishizawa (Saitama University, Japan); Yan-Shiun Wu (National Chiao Tung University, Taiwan); Jun Shiomi (Kyoto University, Japan); Yih-Lang Li (National Chiao Tung University, Taiwan); Hidetoshi Onodera (Kyoto University, Japan)

62 14:25 Hybrid Multi-swarm Optimization Based NoC Synthesis
Muhammad Obaidullah and Gul N. Khan (Ryerson University, Canada)

68 14:50 Multifractal On-Chip Traffic Generation Under TLM
Jose E Bueno and Wang Chau (University of Sao Paulo, Brazil)

74 15:15 Automated, Inter-Macro Channel Space Adjustment and Optimization for Faster Design Closure
Praveen Kumar and Alexander Fell (IIIT Delhi, India); Sachin Mathur (ST Microelectronics, India)

Wednesday, September 6, 15:40 - 16:00

Coffee Break

Wednesday, September 6, 16:00 - 17:40

W3A: Design of Reconfigurable and Multiprocessor Systems

Room: Tegernsee
Chair: Tolga Soyata (SUNY Albany, USA)

80 16:00 Placement Algorithm for Mixed-Grained Reconfigurable Architecture with Dedicated Carry Chain
Koki Honda, Takashi Imagawa and Hiroyuki Ochi (Ritsumeikan University, Japan)

86 16:25 Robust Throughput Boosting for Low Latency Dynamic Partial Reconfiguration
Alberto Nannarelli (Technical University of Denmark, Denmark); Marco Re, Gian Carlo Cardarilli, Luca Di Nunzio, Marco Spaziani Brunella, Rocco Fazzolari and Francesco Carbonari (University of Rome "Tor Vergata", Italy)

91 16:50 Radiation Tolerance Demonstration of High-Speed Scrubbing on an Optically Reconfigurable Gate Array
Takumi Fujimori and Minoru Watanabe (Shizuoka University, Japan)

96 17:15 A Linux-based Support for Developing Real-Time Applications on Heterogeneous Platforms with Dynamic FPGA Reconfiguration
Marco Pagani, Alessio Balsini, Alessandro Biondi, Mauro Marinoni and Giorgio Buttazzo (Scuola Superiore Sant'Anna, Italy)

W3B: Special Session: Secure Multi-Processors Systems-on-Chip for Critical Applications

Rooms: Chiemsee, Königssee

Chair: Bing Li (Technical University of Munich, Germany)

102 16:00 Introduction to Hardware-oriented Security for MPSoCs

Ilia Polian (University of Passau, Germany); Francesco Regazzoni (University of Lugano, Switzerland); Johanna Sepulveda (TU Munich, Germany)

108 16:25 On the Security Evaluation of the ARM TrustZone Extension in a Heterogeneous SoC

EL Mehdi Benhani and Cédric Marchand (University Jean Monnet, France); Lilian Bossuet (University of Lyon, France); Alain Aubert (LTSI, Université Jean Monnet, France)

114 16:50 Securing FPGA SoC Configurations Independent of Their Manufacturers

Nisha Jacob, Jakob Wittmann, Johann Heyszl and Robert Hesselbarth (Fraunhofer Institute for Applied and Integrated Security (AISEC), Germany); Florian Wilde and Michael Pehl (Technische Universität München, Germany); Georg Sigl (Institute for Security in Information Technology, TU München, Germany); Kai Fischer (Siemens AG, Germany)

120 17:15 Cache Attacks and Countermeasures for NTRUEncrypt on MPSoCs: Post-quantum Resistance for the IoT

Johanna Sepulveda (TU Munich, Germany); Andreas Zankl (Fraunhofer AISEC, Germany); Oliver Mischke (Infineon, Germany)

Wednesday, September 6, 17:45 - 19:45

WP: Poster Session & Reception

Rooms: Chiemsee, Königssee, Starnberger See

126 A 0.13um CMOS Integrated Circuit for Electrical Impedance Spectroscopy from 1kHz to 10GHz

Ronny García-Ramírez (Instituto Tecnológico de Costa Rica); Alfonso Chacón-Rodríguez and Renato Rimolo-Donadio (Instituto Tecnológico de Costa Rica, Costa Rica)

Thursday, September 7

Thursday, September 7, 08:30 - 09:30

Thursday Keynote I

The triangle of Power Density, Circuit Degradation and Reliability

Jörg Henkel, Chair for Embedded Systems CES, Karlsruhe Institute of Technology (KIT), Germany

Rooms: Tegernsee, Chiemsee, Königssee

Thursday, September 7, 09:30 - 10:30

Thursday Keynote II

The Path to Global Connectivity - Wireless Communication enters the Next Generation
Josef Hausner, Division Vice President R&D IP Strategy, Intel Mobile Communications, Germany
Rooms: Tegernsee, Chiemsee, Königssee

Thursday, September 7, 10:30 - 10:45

Coffee Break

Thursday, September 7, 10:45 - 12:00

T1A: Power Management and Harvesting

Room: Tegernsee

211 10:45 Realization of Buck Converter with Adaptive Variable-Frequency Control
Ching-Yuan Yang (National Chung Hsing University, Taiwan)

215 11:10 Supercapacitor-Based Embedded Hybrid Solar/Wind Harvesting System Architectures
Mohamadhadi Habibzadeh (SUNY Albany, USA); Moeen Hassanalieragh (University of Rochester, USA); Tolga Soyata (SUNY Albany, USA); Gaurav Sharma (University of Rochester, USA)

221 11:35 MobiCore: An Adaptive Hybrid Approach for Power-Efficient CPU Management on Android Devices
Lucie Broyde and Kent Nixon (University of Pittsburgh, USA); Xiang Chen (George Mason University, USA); Hai (Helen) Li and Yiran Chen (Duke University, USA)

Thursday, September 7, 10:45 - 12:25

T1B: Special Session: Data Analytics Driven Design for Yield, Manufacturability and Reliability: Where Machine Learning Meets Design Automation

Rooms: Chiemsee, Königssee

Chair: Johanna Sepulveda (TU Munich, Germany)

227 10:45 Accelerating Chip Design with Machine Learning: From Pre-Silicon to Post-Silicon
Cheng Zhuo (Zhejiang Univ, P.R. China); Bei Yu (Chinese University of Hong Kong, Hong Kong)

233 11:10 Lithography Hotspot Detection: From Shallow to Deep Learning
Haoyu Yang, Yajun Lin, Bei Yu and Evangeline Young (Chinese University of Hong Kong, Hong Kong)

239 11:35 Generative Adversarial Network Based Scalable On-chip Noise Sensor Placement
Jinglan Liu and Yukun Ding (University of Notre Dame, USA); Jianlei Yang (Beihang University, P.R. China); Ulf Schlichtmann (Technical University of Munich, Germany); Yiyu Shi (University of Notre Dame, USA)

243 12:00 Application of Machine Learning Methods in Post-Silicon Yield Improvement
Baris Yigit, Grace Li Zhang and Bing Li (Technical University of Munich, Germany); Yiyu Shi (University of Notre Dame, USA); Ulf Schlichtmann (Technical University of Munich, Germany)

Thursday, September 7, 12:25 - 13:30

Lunch

Thursday, September 7, 13:30 - 15:10

T2A: Analog and RF Circuits

Room: Tegernsee

Chair: MB Srinivas (BML Munjal University, India)

249 13:30 A Constant Bandwidth Switched-Capacitor Programmable-Gain Amplifier Utilizing Adaptive Miller Compensation Technique
Hyunjong Kim, Yujin Park, Han Yang and Suhwan Kim (Seoul National University, Korea)

253 13:55 Opto-Electrical Analog Front-End with Rapid Power-On and 0.82 pJ/bit for 28 Gb/s in 14 nm FinFET CMOS

Thursday, September 7, 15:10 - 15:30

Coffee Break

Thursday, September 7, 15:30 - 17:00

Panel Discussion: Autonomy, Technology, Safety - Where will automotive electronics go in the next decade?

Rooms: Tegernsee, Chiemsee, Königssee
Chair: Mircea Stan (University of Virginia, USA)

PANELISTS: Knut Hufeld/Infineon, Dominik Reinhardt/BMW, Rakshith Amarnath/Bosch, Jürgen Becker/KIT, Andreas Herkersdorf/TU München, Norbert Schuhmann/FhG-IIS

Thursday, September 7, 19:00 - 22:00

Conference Anniversary Banquet

On Wallberg mountain / Tegernsee

Friday, September 8

Friday, September 8, 08:30 - 09:10

Friday Plenary

The Memory Challenge in Computing Systems: a Survey
Norbert Wehn, Chair for Microelectronic System Design, University of Kaiserslautern, Germany
Rooms: Tegernsee, Chiemsee

Friday, September 8, 09:10 - 10:50

F1A: Networks on Chip

Rooms: Tegernsee, Chiemsee

Chair: Mostafa Khamis (Mentor Graphics, Egypt)

292 09:10 Providing Throughput Guarantees in Mixed-criticality Networks-on-Chip

Sebastian Tobuschat and Rolf Ernst (TU Braunschweig, Germany)

298 09:35 System-Level Simulator for Process Variation Influenced Synchronous and Asynchronous NoCs

Sayed Taha (Beni-suef Univrsity, Egypt); Ali A. ElMoursy (University of Sharjah, United Arab Emirates); Magdy A. El-Moursy (Mentor Graphics Corporation & Electronics Research Institute, Egypt); Hesham Hamed (ElMinia University, Egypt)

304 10:00 Fairness-Oriented Switch Allocation for Networks-on-Chip

Zicong Wang, Xiaowen Chen, Chen Li and Yang Guo (National University of Defense Technology, P.R. China)

310 10:25 Router-Level Performance Driven Dynamic Management in Hierarchical Networks-on-Chip

Mingmin Bai (University of Louisiana at Lafayette, USA); Dan Zhao (Old Dominion University, USA); Magdy Bayoumi (University of Louisiana at Lafayette, USA)

F1B: Algorithms, Models and Simulation for Systems

Room: Königssee

Chair: Bei Yu (Chinese University of Hong Kong, Hong Kong)

316 09:10 Application Specific Component-Service-Aware Trace Generation on Android-QEMU

Hao-Lun Wei, Chung-Ta King and Bhaskar Das (National Tsing Hua University, Taiwan); Mei-Chiao Peng, Chen-Chieh Wang, Hsun-Lun Huang and Juin-Ming Lu (Industrial Technology Research Institute, Taiwan)

322 09:35 A Unified HW/SW System-Level Simulation Framework for Next Generation Wireless System

Nana Sutisna, Leonardo Jr. Lanante, Yuhei Nagao, Masayuki Kurosaki and Hiroshi Ochi (Kyushu Institute of Technology, Japan)

328 10:00 A Graph Based Synthesis Procedure for Linear Analog Function
Mousumi Bhanja and Baidyanath Ray (Indian Institute of Engineering, Science and Technology, Shibpur, India)

334 10:25 A Study on the Energy-Precision Tradeoffs on Commercially Available Processors and SoCs with an EPI Based Energy Model
Jeremy Schlachter (Ecole Polytechnique Federale de Lausanne, Switzerland); Mike Fagan and Krishna Palem (Rice University, USA); Christian Enz (Ecole Polytechnique Federale de Lausanne, Switzerland)

Friday, September 8, 10:50 - 11:10

Coffee Break

Friday, September 8, 11:10 - 12:50

F2A: Low Power Design

Rooms: Tegernsee, Chiemsee

Chair: Eduardo Wachter (PUCRS, Brazil)

340 11:10 Approximate Compressed Sensing for Hardware-Efficient Image Compression
Sai Praveen Kadiyala, Siew Kei Lam and Vikram Kumar Pudi (Nanyang Technological University, Singapore)

346 11:35 Content-aware Line-based Power Modeling Methodology for Image Signal Processor
Chun-Wei Chen and Ming-Der Shieh (National Cheng Kung University, Taiwan); Juin-Ming Lu, Hsun-Lun Huang and Yao-Hua Chen (Industrial Technology Research Institute, Taiwan)

351 12:00 A Multi-Format Floating-Point Multiplier for Power-Efficient Operations
Alberto Nannarelli (Technical University of Denmark, Denmark)

357 12:25 Energy-Efficient Wireless Interconnection Framework for Multichip Systems with In-package Memory Stacks
Md Shahriar Shamim, Meraj Ahmed, Naseef Mansoor and Amlan Ganguly (Rochester Institute of Technology, USA)

F2B: On-chip Fabrics

Room: Königssee

Chair: Chung-Ta King (National Tsing Hua University, Taiwan)

363 11:10 PDA-HyPAR: Path-Diversity-Aware Hybrid Planar Adaptive Routing Algorithm for 3D NoCs

Jindun Dai (Waseda University & Shanghai Jiao Tong University, Japan); Xin Jiang (Graduate School of Information Production and Systems, Waseda University, Japan); Takahiro Watanabe (The Graduate School of Information, Production and Systems Of Waseda University, Japan)

369 11:35 System Management Recovery Protocol for MPSoCs

Vinicius Fochi, Luciano Caimi, Marcelo Ruaro, Eduardo Wachter and Fernando Gehm Moraes (PUCRS, Brazil)

375 12:00 Haar-based Interconnect Coding for Energy Effective Medium/Long Range Data Transport

Nicoleta Cucu-Laurenciu and Sorin Cotofana (Delft University of Technology, The Netherlands)

381 12:25 A Decomposition-Based System Level Synthesis Method for Heterogeneous Multiprocessor Architectures

György Rácz and Péter Arató (Budapest University of Technology and Economics, Hungary)