

# **2017 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC 2017)**

**Abu Dhabi, United Arab Emirates  
23-25 October 2017**



**IEEE Catalog Number: CFP17LSI-POD  
ISBN: 978-1-5386-2881-2**

**Copyright © 2017 by the Institute of Electrical and Electronics Engineers, Inc.  
All Rights Reserved**

*Copyright and Reprint Permissions:* Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

***\*\*\* This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP17LSI-POD
ISBN (Print-On-Demand):	978-1-5386-2881-2
ISBN (Online):	978-1-5386-2880-5
ISSN:	2324-8432

**Additional Copies of This Publication Are Available From:**

Curran Associates, Inc  
57 Morehouse Lane  
Red Hook, NY 12571 USA  
Phone: (845) 758-0400  
Fax: (845) 758-2633  
E-mail: [curran@proceedings.com](mailto:curran@proceedings.com)  
Web: [www.proceedings.com](http://www.proceedings.com)

CURRAN ASSOCIATES INC.  
**proceedings**  
.com

## Table of Contents

Table of Contents

Welcome from the General and Program Chairs .

Committees

Additional Reviewers

List of Volunteers

Internet of Things at UAE

PhD Forum

Keynote Abstracts

Targeting Inter Set Write Variation to Improve the Lifetime of Non-Volatile Caches using fellow sets.....	1
<i>Sukarn Agarwal and Hemangee K. Kapoor</i>	
Low-Overhead Asymmetric Frequency Control for On-Chip Network Interconnects .....	7
<i>Pedro Campos, Nizar Dahir, Martin Trefzer, Andy M. Tyrrell and Gianluca Tempesti</i>	
Power-aware and Cost-efficient State Encoding in Non-volatile memory based FPGAs ....	13
<i>Yuan Xue, Abraham McIlvaine and Chengmo Yang</i>	
Intelligent Embedded and Real-Time ANN-based Motor Control for Multi-Rotor Unmanned Aircraft Systems.....	19
<i>George Michael, Nectarios Efstathiou, Kyriacos Mantis, Theocharis Theocharides and Danilo Pau</i>	
Extending OpenVX for Model-based Design of Embedded Vision Applications.....	25
<i>Stefano Aldegheri and Nicola Bombieri</i>	
Energy-aware Task Scheduling for Near Real-time Periodic Tasks on Heterogeneous Multicore Processors .....	31
<i>Takashi Nakada, Hiroyuki Yanagihashi, Kunimaro Imai, Hiroshi Ueki, Takashi Tsuchiya, Masanori Hayashikoshi and Hiroshi Nakamura</i>	
On the In-field Testing of Spare Modules in Automotive Microprocessors .....	37
<i>Davide Piumatti, Paolo Bernardi, Ernesto Sanchez, Simone Regis, Segio De Luca and Alessandro Sansonetti</i>	
Restoration protocol: Lightweight and secure devices authentication based on PUF .....	43
<i>Brisbane Ovilla-Martinez and Lilian Bossuet</i>	
Implementation and Analysis of Hotspot Mitigation in Mesh NOCs by Cost-Effective Deflection Routing Technique .....	49
<i>Reshma Raj R. S., Abhijit Das and John Jose</i>	

Non-Regression Approach for the Behavioral Model Generator in Mixed-Signal System Verification .....	55
<i>Ling-Yen Song, Chun Wang, Chien-Nan Liu, Yun-Jing Lin, Meng-Jung Lee, Yu-Lan Lo and Shu-Yi Kao</i>	
A sub-W Bio-potential Front End in 65nm CMOS.....	60
<i>Yonatan Kifle, Hani Saleh, Baker Mohammad and Mohammed Ismail</i>	
Applying IJTAG-Compatible Embedded Instruments for Lifetime Enhancement of Analog Front-Ends of Cyber-Physical Systems.....	64
<i>Hans G. Kerkhoff, Ghazanfar Ali, Ahmed Ibrahim, Jerrin Pathrose and Jinbo Wan</i>	
A New Approach For Constructing Logic Functions After ECO.....	70
<i>Amir Masoud Gharehbaghi and Masahiro Fujita</i>	
Exploring the Use of the Finite Element Method for Electromigration Analysis in Future Physical Design.....	76
<i>Matthias Thiele, Steve Bigalke and Jens Lienig</i>	
Multiple Reset Domains Verification Using Assertion Based Verification .....	82
<i>Islam Ahmed, Khaled Nouh and Amr Abbas</i>	
Process-Aware Side Channel Monitoring for Embedded Control System Security.....	88
<i>David Paul-Pena, Prashanth Krishnamurthy, Ramesh Karri and Farshad Khorrami</i>	
DFS Covert Channels on Multi-Core Platforms.....	94
<i>Murugappan Alagappan, Jeyavijayan Rajendran, Milos Doroslovacki and Guru Venkataramani</i>	
Pushing the Limits Further: Sub-Atomic AES.....	100
<i>Markus Stefan Wamser and Georg Sigl</i>	
Prediction Horizon vs. Efficiency of Optimal Dynamic Thermal Control Policies in HPC Nodes.....	106
<i>Daniele Cesarini, Andrea Bartolini and Luca Benini</i>	
Early Bird Sampling: a Short-Paths Free Error Detection-Correction Strategy for Data-Driven VOS .....	112
<i>Andrea Calimera, Roberto Giorgio Rizzo, Valentino Peluso, Jun Zhou and Xin Liu</i>	
Level-shifter-less Approach for Multi-VDD Design to use Body Bias Control in FD-SOI...118	
<i>Kimiyoshi Usami, Shunsuke Kogure, Yusuke Yoshida, Ryo Magasaki and Hideharu Amano</i>	
Robust, Self-Timed Power on Reset Circuit for Low Voltage Applications.....	124
<i>Vivek Nautiyal, Lalit Gupta, Sagar Dwivedi, Gaurav Singla, Jitendra Dasani and Martin Kinkade</i>	
A 2VDD-Enabled Fully-Integrated Low-Dropout Regulator with Fast Transient Response.130	
<i>Shuangxing Zhao, Chenchang Zhan and Guigang Cai</i>	
Single charge-pump generating high positive and negative voltages driving common load..134	
<i>Vikas Rana, Marco Pasotti and Fabio Desantis</i>	
Methodologies for Layout Decomposition and Mask Optimization: A Systematic Review..140	
<i>Yuzhe Ma, Xuan Zeng and Bei Yu</i>	

Redundant Via Insertion in SADP Process with Cut Merging and Optmization .....	141
<i>Youngsoo Song, Jinwook Jung and Youngsoo Shin</i>	
Special session (Embedded Tutorial); Title: Memristive devices for computing: Beyond CMOS and Beyond von Neumann .....	142
<i>Said Hamdioui</i>	
A 86 nA and sub-1 V CMOS voltage reference without resistors and special devices .....	143
<i>Yanhan Zeng, Xin Zhang and Hong-Zhou Tan</i>	
A Low-Offset Dynamic Comparator with Area-Efficient and Low-Power Offset Cancellation .....	148
<i>Xiaopeng Zhong, Amine Bermak and Chi-Ying Tsui</i>	
$\Sigma - \Delta$ BasedForce – FeedbackCapacitiveMicro – machinedSensors : ExtendingtheInputSignalRange .....	154
<i>Ayman Ismail and Ayman Elsayed</i>	
Analyzing the Behavior of FinFET SRAMs with Resistive Defects .....	160
<i>Thiago Copetti, Guilherme Medeiros, Leticia Poehls and Tiago Balen</i>	
Library Pruning and Sigma Corner Libraries for Power Efficient Variation Tolerant Processor Pipelines .....	166
<i>Mini Jayakrishnan, Kim Tae-Hyoung and Alan Chang</i>	
Improving post-silicon error detection with topological selection of trace signals .....	172
<i>Binod Kumar, Kanad Basu, Ankit Jindal, Masahiro Fujita and Virendra Singh</i>	
Enabling Efficient System Design Using Vertical Nanowire Transistor Current Mode Logic	178
<i>Joonseop Sim, Mohsen Imani, Yeseong Kim and Tajana Simunic Rosing</i>	
Defect-Aware Synthesis for Reconfigurable Single-Electron Transistor Arrays .....	184
<i>Juinn-Dar Huang, Yi-Hang Chen and Jia-Shin Lu</i>	
A Wearable Neuro-Degenerative Diseases Detection System based on Gait Dynamics .....	190
<i>Wala Saadeh, Muhammad Awais Bin Altaf and Saad Adnan Butt</i>	
A Low Power, Programmable Bias Inverter Quantizer (BIQ) Flash ADC .....	196
<i>Mahesh Kumar Adimulam, krishna kumar movva, Amit Kapoor and Srinivas M.B</i>	
Low-Jitter Plain Vanilla CMOS CDR with Half-Rate Linear PD and Half Rate Frequency Detector .....	202
<i>Solomon Serunjogi, Mihai Sanduleanu and Mahmoud Rasras</i>	
A Pulsed Decimal Technique for Single-channel, Dynamic Signaling for IoT Applications .	208
<i>Shahzad Muzaffar and Ibrahim Elfadel</i>	
Template based synthesis for high performance computing .....	214
<i>Masahiro Fujita, Wang Qin hao and Yusuke Kimura</i>	
Synthesis of Multi-variate Stochastic Computing Circuits .....	220
<i>Kyounghoon Kim and Kiyoungh Choi</i>	
Continuous Authentication of UAV Flight Command Data using Behaviometrics .....	226
<i>Abdulhadi Shoufan</i>	

A Multiple Valued Logic Approach for the Synthesis of Garbled Circuits.....	232
<i>Stelvio Cinato, Valentina Ciriani, Ernesto Damiani and Maryam Ehsanpour</i>	
Evolution of Logic Locking.....	237
<i>Muhammad Yasin and Ozgur Sinanoglu</i>	