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2017 Silicon Nanoelectronics Workshop

June 4 – 5, 2017

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		L. Hutin ¹ , B. Bertrand ¹ , R. Maurand ² , M. Urdampilleta ³ , B. Jadot ³ , H. Bohuslavskyi ^{1,2} , L. Bourdet ² , Y.-M. Niquet ² , X. Jehl ² , S. Barraud ¹ , C. Bäuerle ³ , T. Meunier ³ , M. Sanquer ² , S. De Franceschi ² , M. Vinet ¹	
		¹ <i>CEA, LETI</i> , ² <i>CEA INAC-PHELIQS</i> , ³ <i>Institut Néel</i>	
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		¹ <i>CEA, LETI</i> , ² <i>CEA, INAC-PHELIQS</i> , ³ <i>STMicroelectronics</i>	

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		Z. Dong, Z. Zhou, Z.F. Li, C. Liu, Y.N. Jiang, P. Huang, L.F. Liu, X.Y. Liu, J.F. Kang <i>Institute of Microelectronics, Peking University</i>	
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		Zheng Zhou, Peng Huang, Yuning Jiang, Zhe Chen, Chen Liu, Lifeng Liu, Xiaoyan Liu and Jinfeng Kang <i>Institute of Microelectronics, Peking University</i>	
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		Takahide Oya ¹ and Takahiro Shinada ² ¹ <i>Graduate School of Engineering, Yokohama National University,</i> ² <i>Center for Innovative Integrated Electronics System, Tohoku University</i>	
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Session 9: Panel Session

16:10-17:40

Topics: **Reinvent silicon device for next generation computing**

Moderator: Masaharu Kobayashi, *University of Tokyo*

Panelists: Nadine Collaert, *IMEC*

Deji Akinwande, *University of Texas at Austin*

Akira Fujiwara, *NTT Basic Research Laboratories*

Louis Hutin, *LETI*

Heike Riel, *IBM Zurich*

17:40 **Closing remarks**