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2017 Silicon Nanoelectronics Workshop

June 4 – 5, 2017
Rihga Royal Hotel Kyoto, Kyoto, Japan

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Session 2: Modeling and characterization of advanced devices

Session 4: Variability and process control

Session 5: Posters

16:50-18:30

16:50 Poster introductions (1 min each)

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Session 6: Plenary and 3D/heterogeneous integrations

10:10 Break

Session 7: 2D materials and devices

Session 8: Architectures for non-von Neumann computing

Session 9: Panel Session

16:10-17:40

Topics: **Reinvent silicon device for next generation computing**

Moderator: Masaharu Kobayashi, *University of Tokyo*

Panelists: Nadine Collaert, *IMEC*
Deji Akinwande, *University of Texas at Austin*
Akira Fujiwara, *NTT Basic Research Laboratories*
Louis Hutin, *LETI*
Heike Riel, *IBM Zurich*

17:40 **Closing remarks**