

2017 IEEE 26th Asian Test Symposium (ATS 2017)

**Taipei City, Taiwan
27 – 30 November 2017**



IEEE Catalog Number: CFP17067-POD
ISBN: 978-1-5386-3516-2

**Copyright © 2017 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP17067-POD
ISBN (Print-On-Demand):	978-1-5386-3516-2
ISBN (Online):	978-1-5386-2437-1
ISSN:	1081-7735

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

2017 IEEE 26th Asian Test Symposium

ATS 2017

Table of Contents

Foreword.....	x
Organizing Committee.....	xi
Program Committee.....	xii
Steering Committee.....	xiv
Reviewers.....	xv
Tutorials.....	xvi
Keynote Addresses.....	xviii
Invited Talk.....	xxiv
Sponsors.....	xxvi

Session 1A: PhD Thesis Award Contest

Trace Based Design for Debug for Post-silicon Validation	N/A
<i>Yun Cheng and Huawei Li</i>	
Testing and Synthesis of Reversible Logic Circuit	N/A
<i>Bikromaditya Mondal and Susanta Chakraborty</i>	
Field Test for Ensuring the Functional Safety of Automotive System	N/A
<i>Hanan T. Al-Awadhi and Hiroshi Takahashi</i>	
Power Side-channel Analysis Based Hardware Trojan Detection through Circuit Partitioning	N/A
<i>Fakir Sharif Hossain and Michiko Inoue</i>	

Session 1B: Interconnect Test and Measurement

An Enhanced Boundary Scan Architecture for Inter-Die Interconnect Leakage Measurement in 2.5D and 3D Packages	5
<i>Pok Man Preston Law, Cheng-Wen Wu, Long-Yi Lin, and Hao-Chiao Hong</i>	
On-Chip Ring Oscillator Based Scheme for TSV Delay Measurement	11
<i>Songwei Pei, Alrashdi Ahmed Rabehb, and Song Jin</i>	

Testing of Interconnect Defects in Memory Based Reconfigurable Logic Device (MRLD)	17
<i>Senling Wang, Yoshinobu Higami, Hiroshi Takahashi, Masayuki Sato, Mitsunori Katsu, and Shoichi Sekiguchi</i>	

Session 1C: Test Compression

Test Pattern Compression for Probabilistic Circuits	23
<i>Chih-Ming Chang, Kai-Jie Yang, James Chien-Mo Li, and Hung Chen</i>	
Test Compression with Single-Input Data Spreader and Multiple Test Sessions	28
<i>Chang-Wen Chen, Yi-Cheng Kong, and Kuen-Jong Lee</i>	
Test Compaction with Dynamic Updating of Faults for Coverage of Undetected Transition Fault Sites	34
<i>Irith Pomeranz</i>	

Session 2A: Hardware Security

A New Active IC Metering Technique Based on Locking Scan Cells	40
<i>Aijiao Cui, Xuesen Qian, Gang Qu, and Huawei Li</i>	
Tree-Based Logic Encryption for Resisting SAT Attack	46
<i>Yung-Chih Chen</i>	
Intra-Die-Variation-Aware Side Channel Analysis for Hardware Trojan Detection	52
<i>Fakir Sharif Hossain, Tomokazu Yoneda, Michihiro Shintani, Michiko Inoue, and Alex Orailoglo</i>	
On Securing Scan Design from Scan-Based Side-Channel Attacks	58
<i>Satyadev Ahlawat, Darshit Vaghani, Jaynarayan Tudu, and Virendra Singh</i>	

Session 2B: Circuits and Systems Reliability-Enhancement Techniques

An Incremental Aging Analysis Method Based on Delta Circuit Simulation Technique	64
<i>Si-Rong He, Nguyen Cao Qui, Yu-Hsuan Kuo, and Chien-Nan Jimmy Liu</i>	
Post-Silicon Test Flow for Aging Prediction	70
<i>Zih-Huan Gao, Hau Hsu, Ting-Shuo Hsu, and Jing-Jia Liou</i>	
Cloud-Based PVT Monitoring System for IoT Devices	76
<i>Guan-Hao Lian, Shi-Yu Huang, and Wei-Yi Chen</i>	
A Critical Charge Model for Estimating the SET and SEU Sensitivity: A Muller C-Element Case Study	82
<i>Marko Andjelkovic, Milos Krstic, Rolf Kraemer, Varadan Savulimedu Veeravalli, and Andreas Steininger</i>	

Session 2C: Techniques for Testing and Reliability

Design and Implementation of an EG-Pool Based FPGA Formatter with Temperature Compensation	88
<i>Yang-Kai Huang, Kuan-Te Li, Chih-Lung Hsiao, Chia-An Lee, Jiun-Lang Huang, and Terry Kuo</i>	
SAR TDC Architecture with Self-Calibration Employing Trigger Circuit	94
<i>Yuki Ozawa, Takashi Ida, Richen Jiang, Shotaro Sakurai, Seiya Takigami, Nobukazu Tsukiji, Ryoji Shiota, and Haruo Kobayashi</i>	
Bringing Fault-Tolerant GigaHertz-Computing to Space: A Multi-stage Software-Side Fault-Tolerance Approach for Miniaturized Spacecraft	100
<i>Christian M. Fuchs, Todor P. Stefanov, Nadia M. Murillo, and Aske Plaat</i>	
Identification of Efficient Clustering Techniques for Test Power Activity on the Layout	108
<i>Harshad Dhotre, Stephan Eggersgluß, and Rolf Drechsler</i>	

Session 3A: Special Session on Hardware-Oriented Security and Trust

Securing Infrastructure IP in Today's SoCs	N/A
<i>Yervant Zorian</i>	
Security Implications of Cyberphysical Flow-Based Microfluidic Biochips	115
<i>Jack Tang, Mohamed Ibrahim, Krishnendu Chakrabarty, and Ramesh Karri</i>	
How to Secure Scan Design Against Scan-Based Side-Channel Attacks?	121
<i>Wei Zhou, Aijiao Cui, Huawei Li, and Gang Qu</i>	

Session 3B: Scan Test

Structure-Oriented Test of Reconfigurable Scan Networks	127
<i>Dominik Ull, Michael Kochte, and Hans-Joachim Wunderlich</i>	
Compaction of a Transparent-Scan Sequence to Reduce the Fail Data Volume for Scan Chain Faults	133
<i>Irith Pomeranz</i>	
Architecture for Reliable Scan-Dump in the Presence of Multiple Asynchronous Clock Domains in FPGA SoCs	139
<i>Amitava Majumdar, Balakrishna Jayadev, Da Cheng, and Albert Lin</i>	
Scan Chain Grouping for Mitigating IR-Drop-Induced Test Data Corruption	145
<i>Yucong Zhang, Stefan Holst, Xiaoqing Wen, Kohei Miyase, Seiji Kajihara, and Jun Qian</i>	

Session 3C: Advanced Testing Techniques

Deterministic Path Delay Measurement Using Short Cycle Test Pattern	151
<i>Kentaro Kato</i>	
Cell-Aware ATPG to Improve Defect Coverage for FPGA IPs and Next Generation Zynq® MPSoCs	157
<i>Seetal Potluri, Aaron Mathew, Rambabu Nerukonda, Ismed Hartanto, and Shahin Toutounchi</i>	
Testing Clock Distribution Networks	163
<i>Sying-Jyan Wang, Hsiang-Hsueh Chen, Chin-Hung Lien, and Katherine Shu-Min Li</i>	
Test Coverage Analysis for Designs with Timing Exceptions	169
<i>Kun-Han Tsai and Srinivasan Gopalakrishnan</i>	

Session 4A: Special Session on Test and Reliability of Emerging Memories

Test and Reliability of Emerging Non-volatile Memories	175
<i>Said Hamdioui, Peyman Pouyan, Huawei Li, Ying Wang, Arijit Raychowdhur, and Insik Yoon</i>	

Session 4B: Debugging and Design Verification

Test and Debug Strategy for High Speed JESD204B Rx PHY	184
<i>Surya Piplani, Humberto Fonseca, Vivek Mohan Sharma, Daniele Cervini, and David Hardisty</i>	
Post Silicon Debugging of Electrical Bugs Using Trace Buffers	189
<i>Kentaro Iwat, Amir Masoud Gharehbaghi, Mehdi B. Tahoori, and Masahiro Fujita</i>	
On Evaluating and Constraining Assertions Using Conflicts in Absent Scenarios	195
<i>Huina Chao, Huawei Li, Xiaoyu Song, Tiancheng Wang, and Xiaowei Li</i>	

Session 4C: Yield Enhancement and Diagnosis

Yield Enhancement by Repair Circuits for Ultra-Fine Pitch Stacked-Chip Connections	201
<i>Keitaro Koga, Hiromitsu Awano, and Makoto Ikeda</i>	
Error-Tolerability Evaluation and Test for Images in Face Detection Applications	206
<i>Tong-Yu Hsieh, Tai-Ang Cheng, and Chao-Ru Chen</i>	
PADLOC: Physically-Aware Defect Localization and Characterization	212
<i>Soumya Mittal and R. D. (Shawn) Blanton</i>	

Session 5A: Advanced Diagnosis Techniques

Automatic Identification of Yield Limiting Layout Patterns Using Root Cause Deconvolution on Volume Scan Diagnosis Data	219
<i>Wu-Tung Cheng, Randy Klingenberg, Brady Benware, Wu Yang, Manish Sharma, Geir Eide, Yue Tian, Sudhakar M. Reddy, Yan Pan, Sherwin Fernandes, and Atul Chittora</i>	
Scan Chain Diagnosis Based on Unsupervised Machine Learning	225
<i>Yu Huang, Brady Benware, Randy Klingenberg, Huaxing Tang, Jayant Dsouza, and Wu-Tung Cheng</i>	
Using Cell Aware Diagnostic Patterns to Improve Diagnosis Resolution for Cell Internal Defects	231
<i>Huaxing Tang, Arvind Jain, Sanil Kumark Pillai, Dharmesh Joshi, and Shamitha Rao</i>	

Session 5B: Design for Testability

Automotive IC On-line Test Techniques and the Application of Deterministic ATPG-Based Runtime Test	237
<i>Yoichi Maeda, Jun Matsushima, and Ron Press</i>	
Open Defect Detection with a Built-in Test Circuit by IDDT Appearance Time in CMOS ICs	242
<i>Ayumu Kambara, Hiroyuki Yotsuyanagi, Daichi Miyoshi, Masaki Hashizume, and Shyue-Kung Lu</i>	
Design for Testability Technique of Reversible Logic Circuits Based on Exclusive Testing	248
<i>Joyati Mondal and Debesh Kumar Das</i>	

Session 5C: Memory Test and Reliability

Fault-Aware Page Address Remapping Techniques for Enhancing Yield and Reliability of Flash Memories	254
<i>Shyue-Kung Lu, Shu-Chi Yu, Masaki Hashizume, and Hiroyuki Yotsuyanagi</i>	
3D IC Memory BIST Controller Allocation for Test Time Minimization Under Power Constraints	260
<i>Yen-Chun Ko and Shih-Hsu Huang</i>	
A Heuristic Algorithm for Automatic Generation of March Tests	266
<i>Xiaole Cui, Yichi Luo, Qiujun Lin, and Xiaoxin Cui</i>	
Author Index	272