2017 Forum on Specification and Design Languages (FDL 2017)

Verona, Italy 18 – 20 September 2017



IEEE Catalog Number: ISBN:

CFP1726E-POD 978-1-5386-1152-4

Copyright © 2017 by the Institute of Electrical and Electronics Engineers, Inc. All Rights Reserved

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

*** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.

 IEEE Catalog Number:
 CFP1726E-POD

 ISBN (Print-On-Demand):
 978-1-5386-1152-4

 ISBN (Online):
 978-1-5386-4733-2

ISSN: 1636-9874

Additional Copies of This Publication Are Available From:

Curran Associates, Inc 57 Morehouse Lane Red Hook, NY 12571 USA Phone: (845) 758-0400

Fax: (845) 758-2633

E-mail: curran@proceedings.com Web: www.proceedings.com





Forum on specification & Design Languages

September 18-20 | Verona, Italy

Table of Contents

Session 1:	Modeling	and Simulation
------------	----------	----------------

- 1.1 Fault Analysis in Analog Circuits through Language Manipulation and Abstraction.....1
 Enrico Fraccaroli, Francesco Stefanni, Franco Fummi, Mark Zwolinski
- 1.2 Actor Fission Transformations for Executing Dataflow Programs on Manycores.....8
 Essayas Gebrewahid, Zain Ul-Abdin
- 1.3 Rethinking of I/O-Automata Composition.....16 Sarah Chabane, Rabea Ameur-Boulifa, Mohamed Mezghiche

Session 2: Languages and Design Methods for Timecritical Systems

- 2.1 Real-Time Ticks for Synchronous Programming.....23 Reinhard von Hanxleden, Timothy Bourke, Alain Girault
- 2.2 Symbolic Simulation of Dataflow Synchronous Programs with Timers.....31
 Guillaume Baudart, Timothy Bourke, Marc Pouzet
- 2.3 Compositional Timing-Aware Semantics for Synchronous Programming.....39
 Joaquin Aguado, Michael Mendler, Jia Jie Wang, Bruno Bodin, Partha Roop

Work in Progress Session

WiP.1 Error Propagation for Cascading Metamodels Applied on an Electric Drive Application.....N/A Christine Forster, Manuel Harrant, Jerome Kirscher, Linus Maurer, Georg Pelz



Forum on specification & Design Languages

September 18-20 | Verona, Italy

- WiP.2 From SQL to Database Processors: A Retargettable Query Planner.....N/A

 Arda Yurdakul
- WiP.3 Towards MARTE++: An Enhanced UML-based Language to Model and Analyse Real-Time and Embedded Systems for the IoT Age.....N/A

 Julio L. Medina, Eugenio Villar
- WiP.4 Scalar Replacement with Array Dataflow Analysis for Hardware Synthesis.....N/A

 Kenshu Seto

Session 4: Design and Validation Methodologies

- 4.1 Automatic Generation of Cycle-Accurate Simulink Blocks from HDL IPs.....47
 Stefano Centomo, Michele Lora, Antonio Portaluri, Francesco Stefanni, Franco Fummi
- 4.2 Towards Consistency Checking Between HDL and UPF Descriptions.....55
 Arthur Kalsing, Laurent Fesquet, Chouki Aktouf
- 4.3 Towards Early Validation of Firmware-Based Power Management Using Virtual Prototypes: A Constrained Random Approach.....61
 Vladimir Herdt, Hoang M. Le, Daniel Große, Rolf Drechsler

Session 5: Next generation Many-Cores

- 5.1 Language and Hardware Acceleration Backend for Graph Processing.....69
 Andrey Mokhov, Alessandro de Gennaro, Ghaith Tarawneh, Jonny Wray, Georgy Lukyanov, Sergey Mileiko, Joe Scott, Alex Yakovlev, Andrew Brown
- 5.2 Runtime Task Mapping for Lifetime Budgeting in Many-Core Systems.....76 Liang Wang, Xiaohang Wang, Ho-fung Leung, Terrence Mak



Forum on specification & Design Languages

September 18-20 | Verona, Italy

5.3 A Reconfigurable Bit-serial FFT/FIR Processor for Ultralow-power Applications.....N/A Yue Lu, Tom J. Kazmierski

Session 6: Design, Optimization, and Verification of Modern Industry Applications

- 6.1 Identifying Bottlenecks in Manufacturing Systems Using Stochastic Criticality Analysis.....84
 João Bastos, Bram van der Sanden, Olaf Donk, Jeroen Voeten, Sander Stuijk, Ramon Schiffelers, Henk Corporaal
- 6.2 ASIL Decomposition Using SMT.....92
 Mona Safar
- 6.3 Multi-Objective Optimization-based Development of Power Electronics for Automotive Applications.....N/A
 Jonas Stricker, Benno Köppl, Jérôme Kirscher, Thomas Nirmaier, Linus Maurer, Georg Pelz
- 6.4 An Emulation Framework for Closed Source Components in Multi-core Automotive Platforms.....N/A
 Ignacio Sañudo, Paolo Burgio, Marko Bertogna