

2018 19th International Symposium on Quality Electronic Design (ISQED 2018)

**Santa Clara, California, USA
13 – 14 March 2018**



**IEEE Catalog Number: CFP18250-POD
ISBN: 978-1-5386-1215-6**

**Copyright © 2018 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP18250-POD
ISBN (Print-On-Demand):	978-1-5386-1215-6
ISBN (Online):	978-1-5386-1214-9
ISSN:	1948-3287

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

TABLE OF CONTENTS

INTERNATIONAL SYMPOSIUM ON QUALITY ELECTRONIC DESIGN 2018

WELCOME to ISQED 2018	iii
ISQED Committees	iv
ISQED Best Papers of 2018	ix
General Information and Convention Center Floor Plan	xi
Program at a Glance	xiv
Keynote and Luncheon Speakers; Panel	xv
Embedded Tutorials	xix

SESSION 1A: Design Verification and Test

Chair: Vinod Viswanath, Real Intent

Co-Chair: Sreejit Chakravarty, Intel Corporation

Concolic Testing of SystemC Designs	1
Bin Lin ¹ , Kai Cong ² , Zhenkun Yang ² , Zhigang Liao ³ , Tao Zhan ⁴ , Christopher Havlicek ¹ , Fei Xie ¹ , ¹ Portland State University, ² Intel Corporation, ³ Virtual Device Technologies LLC, ⁴ Northwestern Polytechnical University	
A Droop Measurement Built-in Self-Test Circuit for Digital Low-Dropout Regulators	8
Aydin Dirican, Cagatay Ozmen, Martin Margala, University of Massachusetts Lowell	
Test Set Identification for Improved Delay Defect Coverage in the Presence of Statistical Delays	14
Pavan Kumar Javvaji, Basim Shanyour, Spyros Tragoudas, Southern Illinois University Carbondale	
Augmenting ESD and EOS Physical Analysis with Per Pin ESD and Leakage DFT	20
Horaira Abu, Salem Abdennadher, Benoit Provost, Harry Muljono, Intel Corporation	

SESSION 1B: System-level Design and Methodologies (SDM)

Chair: Rajesh Berigei, Consultant

Co-Chair: Jingtong Hu, University of Pittsburgh

Hybrid-Comp: A Criticality-Aware Compressed Last-Level Cache	25
Amin Jadidi ¹ , Mohammad Arjomand ² , Mahmut Kandemir ¹ , Chita Das ¹ , ¹ Pennsylvania State University, ² Georgia Institute of Technology	
Energy-Optimal Dynamic Voltage Scaling in Multicore Platforms with Reconfigurable Power Distribution Network	31
Juyeon Kim and Taewhan Kim, Seoul National University	
Optimizing Energy in a DRAM based Hybrid Cache	37
Jiacong He ¹ and Joseph Callenes-Sloan ² , ¹ University of Texas at Dallas, ² California Polytechnic State University	
Program Acceleration Using Nearest Distance Associative Search	43
Mohsen Imani, Daniel Peroni, Tajana Rosing, University of California San Diego	

SESSION 1C: Emerging Logic and Memory Technologies in IoT and Neuromorphic Architectures

Chair: Shih-Hung Chen, IMEC

Co-Chair: Jayita Das, Intel Corporation

Synthesis of Normally-Off Boolean Circuits: An Evolutionary Optimization Approach Utilizing Spintronic Devices	49
Arman Roohi, Ramtin Zand, Ronald F DeMara, University of Central Florida	

LUPIS: Latch-Up Based Ultra Efficient Processing In-Memory System	55
Joonseop Sim, Mohsen Imani, Woojin Choi, Yeseong Kim, Tajana Rosing, University of California San Diego	

Energy Efficient Neuromorphic Processing using Spintronic Memristive Device with Dedicated Synaptic and Neuron Terminology	61
Zoha Pajouhi, Intel Corporation	

A Bi-Memristor Synapse with Spike-Timing-Dependent Plasticity for On-Chip Learning in Memristive Neuromorphic Systems	69
Sagarvarma Sayyaparaju, Sherif Amer, Garrett S. Rose, University of Tennessee Knoxville	

SESSION 2A: Automated Analog and Digital Circuit Optimization

Chair: Srinu Krishnamoorthy, AMD

Co-Chair: Srinivas Katkooi, University of South Florida

Recognition of Regular Layout Structures	75
Yu-Cheng Chiang, Shr-Cheng Tsai, Rung-Bin Lin, Yuan Ze University	

A Simplified Methodology for Complex Analog Module Layout Generation	82
Pradeep Kumar Chawda, Texas Instruments, Inc	

Process Variation Aware D-Flip-Flop Design using Regression Analysis	88
Shinichi Nishizawa ¹ and Hidetoshi Onodera ² , ¹ Saitama University, ² Kyoto University	

Clock Buffer and Flip-flop Co-optimization for Reducing Peak Current Noise	94
Joohan Kim and Taewhan Kim, Seoul National University	

Parasitic-Aware g_m/I_D-Based Many-Objective Analog/RF Circuit Sizing	100
Tuotian Liao and Lihong Zhang, Memorial University of Newfoundland	

SESSION 2B: System-level Design and Methodologies (SDM)

Chair: Rajesh Berigei, Consultant

Co-Chair: Jingtong Hu, University of Pittsburgh

A Loop Structure Optimization Targeting High-level Synthesis of Fast Number Theoretic Transform	106
Kazushi Kawamura, Masao Yanagisawa, Nozomu Togawa, Waseda University	

A 4-PAM Interconnect in Network-on-Chip for High-Throughput and Latency-Sensitive Applications	112
Ahmad Mansour ¹ , Ahmed Elnaggar ¹ , Bassma Alabassy ² , Mostafa Khamis ² , Ahmed Shalaby ³ , ¹ Alexandria University, ² Mentor Graphics Corp., ³ Benha University	

Comparative Study and Prediction Modeling of Photonic Ring Network on Chip Architectures	119
Sara Karimi and Jelena Trajkovic, Concordia University	

Power and Performance Aware Memory-Controller Voting Mechanism	127
Milena Vratonjic ¹ , Harmander Singh ² , Gautam Kumar ³ , Roumi Mohamed ³ , Ashish Bajaj ³ , Ken Gainey ¹ , ¹ Qualcomm Atheros, Inc., ² Qualcomm Technologies Inc., ³ Qualcomm India Private Limited	

PDA-HyPAR: Path-Diversity-Aware Hybrid Planar Adaptive Routing Algorithm for 3D NoCs	131
Jindun Dai ^{1,2} , Renjie Li ² , Xin Jiang ³ , Takahiro Watanabe ² , ¹ Shanghai Jiao Tong University, ² Waseda University, ³ Kitakyushu College	

SESSION 2C: Poster Papers

Chair: Swaroop Ghosh, Pennsylvania State University

Network on Interconnect Fabric	138
Boris Vaisband, Adeel Bajwa, Subramanian Iyer, University of California, Los Angeles	

Efficient K Nearest Neighbor Algorithm Implementations for Throughput-Oriented Architectures ...	144
Jihyun Ryoo ¹ , Meena Arunachalam ² , Rahul Khanna ² , Mahmut Kandemir ¹ , ¹ Pennsylvania State University, ² Intel Corporation	

Body-Biasing Assisted V_{min} Optimization for 5nm-Node Multi-V_t FD-SOI 6T-SRAM	151
Jheng-Yi Chen, Ming-Yu Chang, Shi-Hao Chen, Jia-Wei Lee, Meng-Hsueh Chiang, National Cheng Kung University	
Measuring the Effectiveness of ISO26262 Compliant Self Test Library	156
Frederico Pratas, Thomas Dedes, Andrew Webber, Majid Bemanian, Itai Yarom, MIPS Tech LLC	
An Online Framework for Diagnosis of Multiple Defects in Scan Chains	162
Sarmad Tanwir ¹ , Michael Hsiao ¹ , Loganathan Lingappan ² , ¹ Virginia Tech, ² Intel Corporation	
Routing at Compile Time	169
Chun-Xun Lin, Tsung-Wei Huang, Martin Wong, University of Illinois at Urbana-Champaign	
Uncertainty Aware Mapping of Embedded Systems for Reliability, Performance, and Energy	176
Wenkai Guan, Milad Ghorbani Moghaddam, Cristinel Ababei, Marquette University	
On the Write Energy of Non-Volatile Resistive Crossbar Arrays with Selectors	184
Albert Ciprut and Eby G. Friedman, University of Rochester	
A Modified Method of Logical Effort for FinFET Circuits Considering Impact of Fin-Extension Effects	189
Archana Pandey ¹ , Pitul Garg ¹ , Shobhit Tyagi ¹ , Rajeev Ranjan ² , Anand Bulusu ¹ , ¹ Indian Institute of Technology Roorkee, ² Samsung Electronics	
Generic System-Level Modeling and Optimization for Beyond CMOS Device Applications	196
Victor Huang, Chenyun Pan, Azad Naeemi, Georgia Institute of Technology	
Terahertz Travelling Wave Amplifier Design using Ballistic Deflection Transistor	201
Huan Wang ¹ , Jean-François Millithaler ¹ , Ronald Knepper ² , Martin Margala ¹ , ¹ University of Massachusetts, ² Boston University	
Reliable Memory PUF Design for Low-Power Applications	207
Mohammad Saber Golanbari, Saman Kiamehr, Rajendra Bishnoi, Mehdi Tahoori, Karlsruhe Institute of Technology	
An ESD Transient Clamp with 494 pA Leakage Current in GP 65 nm CMOS Technology	214
Mahdi Elghazali, Manoj Sachdev, Ajoy Opal, University of Waterloo	
Enhancing Circuit Operation using Analog Floating Gates	221
Ujas Patel ¹ , Sai Govinda Rao Nimmalapudi ¹ , Harvey Stiegler ¹ , Andrew Marshall ¹ , Keith Jarreau ² , ¹ University of Texas at Dallas, ² Texas Instruments Inc	
An Automated Flow for Design Validation of Switched Mode Power Supply	227
Pradeep Kumar Chawda and Srikrishna Srinivasan, Texas Instruments Inc	
Dynamic NoC Platform for Varied Application Needs	232
Sidhartha Sankar Rout ¹ , Hemanta Kumar Mondal ² , Rohan Juneja ¹ , Sri Harsha Gade ¹ , Sujay Deb ¹ , ¹ Indraprastha Institute of Information Technology Delhi, ² University of Southern Brittany	

SESSION 3A.1: Design Verification and Test

Chair: Vinod Viswanath, Real Intent

Co-Chair: Sreejit Chakravarty, Intel Corporation

A Technique to Aggregate Classes of Analog Fault Diagnostic Data Based on Association Rule Mining	238
Ruslan Dautov ¹ and Sergey Mosin ² , ¹ Shenzhen University, ² Kazan Federal University	
Extracting Hardware Assertions Including Word-Level Relations over Multiple Clock Cycles	244
Mami Miyamoto and Kiyoharu Hamaguchi, Shimane University	

SESSION 3A.2: Automated Analog and Digital Circuit Optimization

Chair: Srinu Krishnamoorthy, AMD

Co-Chair: Srinivas Katkoori, University of South Florida

A Study on NBTI-induced Delay Degradation Considering Stress Frequency Dependence	251
Zuitoku Shin ¹ , Shumpei Morita ¹ , Song Bian ¹ , Michihiro Shintani ² , Masayuki Hiromoto ¹ , Takashi Sato ¹ , ¹ Kyoto University, ² Nara Institute of Science and Technology	
Verification Methodology to Guarantee Low Routing Resistance to Well Taps	257
Mohammed Fakhruddin, Kuok-Khian Lo, James Karp, Michael Hart, Min-Hsing Chen, Xilinx, Inc.	

SESSION 3B: High Performance / Low Power Logic Design

Chair: Kurt Schwartz, Texas Instruments, Inc.

Co-Chair: Jose Pineda de Gyvez, Eindhoven Univ of Technology

Ultra-Low Swing CMOS Transceiver for 2.5-D Integrated Systems	262
Przemyslaw Mrosczyk and Vasilis Pavlidis, The University of Manchester	
Back-Bias Generator for Post-Fabrication Threshold Voltage Tuning Applications in 22nm FD-SOI Process	268
Arif Siddiqi, Navneet Jain, Mahbub Rashed, Globalfoundries Inc	
Logic-based Row Redundancy Technique Designed in 7nm FinFET Technology for Embedded SRAMs	274
Vivek Nautiyal, Nishant Nukala, Fakhruddinali Bohra, Sagar Dwivedi, Jitendra Dasani, Satinderjit Singh, Gaurav Singla, Martin Kinkade Kinkade, ARM Inc	
A 125mV 2ns-Access-Time 16Kb SRAM Design based on a 6T Hybrid TFET-FinFET Cell	280
Hassan Afzali-Kusha, Alireza Shafaei, Massoud Pedram, University of Southern California	

SESSION 3C: IoT and Smart Sensors

Chair: Pradeep Chawda, Texas Instruments, Inc.

Co-Chair: Ali A. Shahi, Globalfoundries, Inc.

New AC Resistance Calculation of Printed Spiral Coils for Wireless Power Transfer	286
Gaorong Qian, Yuhua Cheng, Guoxiong Chen, Gaofeng Wang, Hangzhou Dianzi University	
An Automated Design Flow for Synthesis of Optimal Multi-layer Multi-shape PCB Coils for Inductive Sensing Applications	290
Pradeep Kumar Chawda, Texas Instruments, Inc	
When "things" Get Older: Exploring Circuit Aging in IoT Applications	296
Xinfei Guo, Vaibhav Verma, Patricia Gonzalez-Guerrero, Mircea Stan, University of Virginia	

SESSION 4A.1: Design Technology Co-Optimization

Chair: Aswin Mehta, Texas Instruments, Inc.

Co-Chair: Rajan Beera, Pall Corporation

(paper withdrawn)	N/A
--------------------------------	------------

SESSION 4A.2: Machine Learning on Conventional and Emerging Platforms

Chair: Yang (Cindy) Yi, Virginia Tech

Co-Chair: Aswin Mehta, Texas Instruments, Inc.

A Deep Learning Based Approach for Analog Hardware Implementation of Delayed Feedback Reservoir Computing System	308
Jialing Li, Kangjun Bai, Lingjia Liu, Yang Yi, Virginia Tech	

An Area and Energy Efficient Design of Domain-Wall Memory-Based Deep Convolutional Neural Networks using Stochastic Computing	314
Xiaolong Ma ¹ , Yipeng Zhang ¹ , Geng Yuan ¹ , Ao Ren ¹ , Zhe Li ¹ , Jie Han ² , Jingtong Hu ³ , Yanzhi Wang ¹ , ¹ Syracuse University, ² University of Alberta, ³ University of Pittsburgh	

A Path to Energy-efficient Spiking Delayed Feedback Reservoir Computing System for Brain-inspired Neuromorphic Processors	322
Kangjun Bai and Yang Yi, Virginia Tech	

SESSION 4B: High Performance / Low Power Logic Design

Chair: Jose Pineda de Gyvez, Eindhoven Univ of Technology

Co-Chair: Raviprakash Rao, Texas Instruments, Inc.

Low Power Latch Based Design with Smart Retiming	329
Kamlesh Singh ¹ , Hailong Jiao ^{1,2} , Jos Huisken ¹ , Hamed Fatemi ³ , José Pineda de Gyvez ³ , ¹ Eindhoven University of Technology, ² Peking University, ³ NXP Semiconductors	

Parallel implementation of Finite State Machines for Reducing the Latency of Stochastic Computing	335
Cong Ma and David Lilja, University of Minnesota Twin Cities	

A Post-Silicon Hold Time Closure Technique using Data-Path Tunable-Buffers for Variation-Tolerance in Sub-threshold Designs	341
Divya Akella Kamakshi, Xinfei Guo, Harsh Patel, Mircea Stan, Benton Calhoun, University of Virginia	

A Low-Power Configurable Adder for Approximate Applications	347
Tongxin Yang, Tomoaki Ukezono, Toshinori Sato, Fukuoka University	

SESSION 4C: IoT & Smart Sensors

Chair: Pradeep Chawda, Texas Instruments, Inc.

Co-Chair: Ali A. Shahi, Globalfoundaries, Inc.

Mathematical Derivation, Circuits Design and Clinical Experiments of Measuring Blood Flow Volume (BFV) at Arteriovenous Fistula (AVF) of Hemodialysis (HD) Patients Using a Newly-Developed Photoplethysmography (PPG) Sensor	353
Paul (C.P.) Paul ¹ , Pei-Yu Chiang ¹ , D.C. Tarng ² , C.Y. Yang ² , ¹ National Chiao Tung University, ² Taipei Veterans General Hospital	

A Wireless Multifunctional Monitoring System of Tower Body Running State Based on MEMS Acceleration Sensor	357
Linxi Dong, Haonan Wang, Gaofeng Wang, Weimin Qiu, Hangzhou Dianzi University	

Power Management Factors and Techniques for IoT Design Devices	364
Anupriya Prasad and Pradeep Chawda, Texas instruments, Inc	

Hierarchical Dynamic Goal Management for IoT Systems	370
Axel Jantsch ¹ , Arman Anzanpour ² , Hedyeh Kolerdi ¹ , Iman Azimi ² , Lydia Chaido Siafara ¹ , Amir M. Rahmani ^{1,3} , Nima TaheriNejad ¹ , Pasi Liljeberg ² , Nikil Dutt ³ , ¹ TU Wien, ² University of Turku, ³ University of California Irvine	

SESSION 5A: Machine Learning on Conventional and Emerging Platforms

Chair: Yang (Cindy) Yi, Virginia Tech

Co-Chair: Aswin Mehta, Texas Instruments, Inc.

Quantized Neural Networks with New Stochastic Multipliers	376
Bingzhe Li ¹ , MohammadHassan Najafi ¹ , Bo Yuan ² , David Lilja ¹ , ¹ University of Minnesota-Twin Cities, ² City University of New York	

High Performance Training of Deep Neural Networks Using Pipelined Hardware Acceleration and Distributed Memory	383
Raghav Mehta ¹ , Yuyang Huang ² , Mingxi Cheng ³ , Shrey Bagga ⁴ , Nishant Mathur ⁴ , Ji Li ⁴ , Jeffrey Draper ⁴ , Shahin Nazarian ⁴ , ¹ Mentor, ² NVIDIA, ³ Duke University, ⁴ University Of Southern California	

Deep Neural Network Acceleration Framework Under Hardware Uncertainty	389
Mohsen Imani, Pushen Wang, Tajana Rosing, University of California San Diego	
A Hardware-Friendly Algorithm for Scalable Training and Deployment of Dimensionality Reduction Models on FPGA	395
Mahdi Nazemi, Amir Erfan Eshratifar, Massoud Pedram, University of Southern California	

SESSION 5B: Hardware Security: PUF, Obfuscation, and Trojan Detection

Chair: Jon Nafziger, Texas Instruments, Inc.

Co-Chair: Jie Gu, Northwestern University

Securing FPGA-based Obsolete Component Replacement for Legacy Systems	401
Zhiming Zhang ¹ , Laurent Njilla ² , Charles Kamhoua ³ , Kevin Kwiat ² , Qiaoyan Yu ¹ , ¹ University of New Hampshire, ² Air Force Research Laboratory, ³ Army Research Laboratory	
High-Level Synthesis of Key Based Obfuscated RTL Datapaths	407
Sheikh Ariful Islam and Srinivas Katkoori, University of South Florida	
Double Error Cellular Automata-Based Error Correction with Skip-mode Compact Syndrome Coding for Resilient PUF Design	413
Anthony Mattar El Raachini, Hussein Alawieh, Adam Issa, Zainab Swaidan, Rouwaida Kanj, Ali Chehab, Mazen Saghir, American University of Beirut	
Design and Evaluation of Physical Unclonable Function for Inorganic Printed Electronics	419
Ahmet Turan Erozan ¹ , Mohammad Saber Golanbari ¹ , Rajendra Bishnoi ¹ , Jasmin Aghassi-Hagmann ^{1,2} , Mehdi Tahoori ¹ , ¹ Karlsruhe Institute of Technology, ² Offenburg University of Applied Sciences	

SESSION 5C: Demystifying Self-driving Cars

Chair: Jayita Das, Intel Corporation

Co-Chair: Swatilekha Saha, Cypress Semiconductor

Near-Future Traffic Evaluation based Navigation for Automated Driving Vehicles Considering Traffic Uncertainties	425
Kuen-Wey Lin ¹ , Masanori Hashimoto ² , Yih-Lang Li ¹ , ¹ National Chiao Tung University, ² Osaka University	
Low Cost and Power CNN/Deep Learning Solution for Automated Driving	432
Mihir Mody, Desappan Kumar, Pramod Swami, Manu Mathew, Soyeb Nagori, Texas Instruments, Inc	
Resource Constrained Cellular Neural Networks for Real-time Obstacle Detection using FPGAs	437
Xiaowei Xu ^{1,2} , Tianchen Wang ¹ , Qing Lu ¹ , Yiyu Shi ¹ , ¹ University of Notre Dame, ² Huazhong University of Science and Technology	