

2018 13th International Conference on Design & Technology of Integrated Systems In Nanoscale Era (DTIS 2018)

**Taormina, Italy
9-12 April 2018**



**IEEE Catalog Number: CFP1893A-POD
ISBN: 978-1-5386-5292-3**

**Copyright © 2018 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP1893A-POD
ISBN (Print-On-Demand):	978-1-5386-5292-3
ISBN (Online):	978-1-5386-5291-6

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

TABLE OF CONTENTS

ANALOG FAULT SIMULATION AUTOMATION AT SCHEMATIC LEVEL WITH RANDOM SAMPLING TECHNIQUES	1
<i>L. Wu, M. Hussain, S. Abughannam, W. Muller, C. Scheytt, W. Ecker</i>	
METHODOLOGY FOR IMPROVED EVENT-DRIVEN SYSTEM-LEVEL SIMULATION OF AN RF TRANSCEIVER SUBSYSTEM FOR WIRELESS SOCS.....	5
<i>F. Speicher, C. Beyerstedt, M. Scholl, T. Saalfeld, V. Bonehi, M. Schrey, R. Wunderlich, S. Heinen</i>	
A NOVEL HARDWARE-ACCELERATED REAL-TIME TASK SCHEDULER BASED ON ROBUST EARLIEST DEADLINE ALGORITHM	9
<i>L. Kohutka, V. Stopjakova</i>	
DYNAMIC PARTIAL RECONFIGURATION VERIFICATION USING ASSERTION BASED VERIFICATION	11
<i>I. Ahmed, H. Mostafa, A. Mohieldin</i>	
MEMRISTOR BASED ADAPTIVE IMPEDANCE AND FREQUENCY TUNING NETWORK	13
<i>C. Palson, D. Krishna, J. Mathew, J. Babita, M. Ottavi, V. Gupta</i>	
A FULLY CONTACTLESS WAFER-LEVEL TESTING FOR UHF RFID TAG WITH ON-CHIP ANTENNA	15
<i>A. Finocchiario, G. Girlando, A. Motta, A. Pagani, G. Palmisano</i>	
INCREASING RELIABILITY OF SAFETY CRITICAL APPLICATIONS THROUGH FUNCTIONAL BASED SOLUTIONS	21
<i>E. Sanchez</i>	
THE TEST COST REDUCTION BENEFITS OF COMBINING A HIERARCHICAL DFT METHODOLOGY WITH EDT CHANNEL SHARING - A CASE STUDY	22
<i>B. Lu, S. Sha, J. Wang, Z. Zhang, F. Meng, D. Hsu, R. Fisette</i>	
TRADING-OFF RELIABILITY AND PERFORMANCE IN FPGA-BASED RECONFIGURABLE HETEROGENEOUS SYSTEMS	26
<i>A. Vallero, A. Carelli, S. Di Carlo</i>	
PARALLEL SOFTWARE-BASED SELF-TEST SUITE FOR MULTI-CORE SYSTEM-ON-CHIP: MIGRATION FROM SINGLE-CORE TO MULTI-CORE AUTOMOTIVE MICROCONTROLLERS.....	32
<i>A. Floridia, D. Piumatti, E. Sanchez, S. De Luca, A. Sansonetti</i>	
IS APPROXIMATE COMPUTING SUITABLE FOR SELECTIVE HARDENING OF ARITHMETIC CIRCUITS?.....	38
<i>B. Deveautour, A. Virazel, P. Girard, S. Pravossoudovitch, V. Gherman</i>	
UNIFIED FIELD MULTIPLIER FOR ECC: INHERENT RESISTANCE AGAINST HORIZONTAL SCA ATTACKS	44
<i>I. Kabin, Z. Dyka, D. Kreiser, P. Langendoerfer</i>	
SECCS: SECURE CONTEXT SAVING FOR IOT DEVICES	48
<i>E. Valea, M. Da Silva, G. Di Natale, M.-L. Flottes, S. Dupuis, B. Rouzeyre</i>	
TWO DIMENSIONAL FFT ARCHITECTURE BASED ON RADIX-4³ ALGORITHM WITH EFFICIENT OUTPUT REORDERING	50
<i>S. Kala, S. Nalesh, J. Babita, J. Mathew, M. Ottavi</i>	
AN AUTOMATIC APPROACH TO INTEGRATION TESTING FOR CRITICAL AUTOMOTIVE SOFTWARE	52
<i>J. Sini, A. Mugoni, M. Violante, A. Quario, C. Argiri, F. Fusetti</i>	
SETUP AND EXPERIMENTAL RESULTS ANALYSIS OF COTS CAMERA AND SRAMS AT THE ISIS NEUTRON FACILITY	54
<i>M. Ottavi, D. Asciolla, T. Fiorucci, E. Grosso, C. Marzullo, A. Scaramella, S. Stramaccioni, A. Zibecchi, C. Andreani, G. Cardarilli, C. Cazzaniga, L. Di Nunzio, R. Fazzolari, M. Re, P. Reviriego, G. Furano, R. Senesi</i>	
DEVICE AND CIRCUIT MODELS OF INALN/GAN D- AND DUAL-GATE E-MODE HEMTS FOR DESIGN AND CHARACTERISATION OF MONOLITHIC NAND LOGIC CELL	58
<i>A. Chvala, L. Nagy, J. Marek, J. Priesol, D. Donoval, A. Satka, M. Blaho, D. Gregusova, J. Kuzmik</i>	
AMMONIA SENSORS BASED ON IN SITU FABRICATED NANOCRYSTALLINE GRAPHENE FIELD-EFFECT DEVICES	64
<i>D. Noll, U. Schwalke</i>	
RECONFIGURABLE ELECTROSTATICALLY DOPED 2.5-GATE PLANAR FIELD-EFFECT TRANSISTORS FOR DOPANT-FREE CMOS	69
<i>T. Krauss, F. Wessely, U. Schwalke</i>	

ANALYTICAL MODELING OF RESPONSE TIME AND FULL WELL CAPACITY OF A PINNED PHOTO DIODE.....	73
<i>K. Ashkay, P. Pillai, B. Bhuvan</i>	
AN ENERGY-AUTONOMOUS WIRELESS SENSOR NETWORK DEVELOPMENT PLATFORM.....	79
<i>M. Grosso, S. Rinaudo, E. Patti, A. Acquaviva</i>	
A POWER-SUPPLY NOISE AWARE DYNAMIC TIMING ANALYSIS METHODOLOGY, BASED ON A STATISTICAL PREDICTION ENGINE.....	85
<i>M. Tsiampas, N. Evmorfopoulos, K. Daloukas, J. Moondanos, G. Stamoulis</i>	
A RESOURCE-EFFICIENT FFT/IFFT ARCHITECTURE FOR PRIME PLC SYSTEMS.....	91
<i>J. Yang, N. Tan, C.-K. Tzou</i>	
A CONFIGURABLE OPERATIONAL AMPLIFIER BASED ON OXIDE RESISTIVE RAMS.....	93
<i>H. Aziza, C. Dufaza, A. Perez</i>	
SIC PAIR GENERATION IN NEAR-OPTIMAL TIME WITH CARRY-LOOK AHEAD ADDERS.....	95
<i>I. Voyiatzis, C. Efstathiou</i>	
CROSS-PRODUCT FUNCTIONAL COVERAGE ANALYSIS USING MACHINE LEARNING CLUSTERING TECHNIQUES.....	97
<i>E. El Mandouh, A. Salem, M. Amer, A. Wassal</i>	
WIRELESS SEMG/FOOTSWITCH DRIVEN FPGA EMBEDDED DIGITAL PROCESSOR FOR DYNAMIC MFCV ESTIMATION.....	99
<i>G. Mezzina, D. De Venuto</i>	
EVALUATION OF A MEDIAN THRESHOLD BASED EEPROM-PUF CONCEPT IMPLEMENTED IN A HIGH TEMPERATURE SOI CMOS TECHNOLOGY.....	101
<i>B. Willsch, M. Heesen, J. Hauser, S. Dreiner, H. Kappert, H. Vogt</i>	
NUMERICAL APPROACH TO PREDICT POWER DEVICE RELIABILITY.....	107
<i>A. Sitta, S. Russo, G. Bazzano, D. Cavallaro, G. Greco, M. Calabretta</i>	
EVALUATION OF THE TEMPERATURE INFLUENCE ON SEU VULNERABILITY OF DICE AND 6T-SRAM CELLS.....	112
<i>E. Farjallah, J.-M. Armani, V. Gherman, L. Dilillo</i>	
TOWARDS A SCALABLE QUANTUM COMPUTER.....	117
<i>C. Almudever, N. Khammassi, L. Hutin, M. Vinet, M. Babaie, F. Sebastiano, E. Charbon, K. Bertels</i>	
A NOVEL MAC PROTOCOL FOR INDUSTRIAL WLAN: HARDWARE ASPECTS.....	118
<i>Z. Stamenkovic</i>	
PROGRAMMABLE LOGIC FOR SINGLE-OUTPUT FUNCTIONS.....	119
<i>I. Voyiatzis, C. Efstathiou, C. Sgouropoulou</i>	
GIVE ME YOUR BINARY, I'LL TELL YOU IF IT LEAKS.....	121
<i>A. Bouvet, N. Bruneau, A. Facon, S. Guilley, D. Marion</i>	
TOWARDS NOVEL FORMAT FOR REPRESENTATION OF POLYMORPHIC CIRCUITS.....	125
<i>A. Crha, V. Simek, R. Ruzicka</i>	
A 1KX32 BIT WDSRAM PAGE WITH RAPID WRITE ACCESS.....	127
<i>T. Simopoulos, T. Haniotakis, G. Alexion</i>	
OPTIMUM POLYMORPHIC CIRCUITS SYNTHESIS METHOD.....	129
<i>P. Fiser, V. Simek</i>	
LOW-ENERGY KEY EXCHANGE FOR AUTOMATION SYSTEMS.....	135
<i>D. Kreiser, Z. Dyka, I. Kabin, P. Langendoerfer</i>	
IMPACT OF DYNAMIC PARTIAL RECONFIGURATION ON CONNECT NETWORK-ON-CHIP FOR FPGAS.....	140
<i>R. Ahmed, H. Mostafa, A. Khalil</i>	
Author Index	