

2017 18th International Workshop on Microprocessor and SOC Test and Verification (MTV 2017)

**Austin, Texas, USA
11 – 12 December 2017**



**IEEE Catalog Number: CFP17MTV-POD
ISBN: 978-1-5386-3352-6**

**Copyright © 2017 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP17MTV-POD
ISBN (Print-On-Demand):	978-1-5386-3352-6
ISBN (Online):	978-1-5386-3351-9
ISSN:	1550-4093

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

2017 18th International Workshop on Microprocessor and SOC Test and Verification

MTV 2017

Table of Contents

Preface	vii
Acknowledgment	viii
Conference Organization	ix
Program Committee	x
Corporate Sponsors	xi

Test Generation and Verification

A Unified UVM Architecture for Flash-Based Memory	1
<i>Khaled Salah</i>	
SequenceLanguage: A Constraint Random MP-RIS Generation Framework	5
<i>Madhukarreddy Pappireddy and Bipin Ravi</i>	
Maintaining ISA Specifications in MicroTESK Test Program Generator	10
<i>Mikhail Chupilko, Alexander Kamkin, Artem Kotsyniak, Alexander Protsenko, Sergey Smolov, and Andrei Tatarnikov</i>	
Automation of Processor Verification Using Recurrent Neural Networks	15
<i>Martin Fajcik, Pavel Smrz, and Marcela Zachariasova</i>	
Anvil: Best in Class Multiprocessor Coherency Verification Tool	21
<i>Kaushik Gopalakrishnan and Bipin Ravi</i>	
Dynamic Exerciser Template Weighting in x86 Processor Verification	26
<i>Ahmed Wahba, Justin Hohnerlein, Farhan Rahman, and Li-C. Wang</i>	
Validation of Context Preserving Thread-Level Speculative Execution Using N-Queens: Comparison of Non-CPSE and CPSE-enabled Applications	32
<i>Jack Lawrence Mason</i>	
TLM Virtual Platform for Fast and Accurate Power Estimation	35
<i>Ahmed Abdel-Haleem and Magdy A. El-Moursy</i>	
Electromagnetic (EM) Crosstalk Failures and Symptoms in SoC Designs	39
<i>Anand Raman, Yorgos Koutsoyannopoulos, and Magdy Abadir</i>	

Security

iPUF: Interconnect PUF with Self-Masking Circuit for Performance Enhancement	45
<i>Liting Yu, Xiaoxiao Wang, Fahim Rahman, and Mark Tehranipoor</i>	
Hardware-Assisted Cybersecurity for IoT Devices	51
<i>Fahim Rahman, Mohammad Farmani, Mark Tehranipoor, and Yier Jin</i>	
A Security-Aware Pre-partitioning Technique for 3D Integrated Circuits	57
<i>Siroos Madani and Magdy Bayoumi</i>	
Identifying and Measuring Security Critical Path for Uncovering Circuit Vulnerabilities	62
<i>Wei Hu, Armaiti Ardeshiricham, and Ryan Kastner</i>	
Modeling and Analysis of Secure Processor Extensions Based on Actor Networks	68
<i>Mark Nelson and Peter-Michael Seidel</i>	
Author Index	74