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TECHNICAL PROGRAM: ORAL PAPERS

Session 1: Full Wave Modeling

Fast Direct Full-Wave Electromagnetic Analysis of Planar Circuits Embedded in Multilayered Media

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A Fully 3-D BIE Evaluation of the Resistance and Inductance of On-Board and On-Chip Interconnects

M. Huynen, D. De Zutter, D. Vande Ginste, *Electromagnetics Group/IDLab, Department of Information Technology, Ghent University/Imec, Gent, Belgium*

Session 2: Macromodeling

Multivariate Macromodeling with Stability and Passivity Constraints

A. Zanco, S. Grivet-Talocia, T. Bradde, M. De Stefano, *Dept. Electronics and Telecommunications, Politecnico di Torino, Italy*

Reduced-Order Model for Time-Domain Sensitivity Analysis of Active Circuits

B. Nouri, M. Nakhla, Department of Electronics, Carleton University, Ottawa, Canada

Circuit Synthesis of Blackbox Macromodels from S-Parameter Representation

J. Schutt-Ainé, Electrical and Computer Engineering. University of Illinois Urbana, USA

Session 3: Stochastic Analysis & Uncertainty Quantification

Uncertainty Quantification of SiP based Integrated Voltage Regulator

M. Larbi[1], H. M. Torun[1], M. Swaminathan[1], I. S. Stievano[2], F. G. Canavero[2], P. Besnier[3], *[1]Center for Co-Design of Chip, Package, System (C3PS), School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, US; [2]Dipartimento di Elettronica, Politecnico di Torino, Italy; [3]IETR, UMR CNRS 6164 : IETR, INSA de Rennes, France.*

Perturbative Statistical Assessment of PCB Differential Interconnects

X. Wu[1], P. Manfredi[2], F. Grassi[1], D. Vande Ginste[3], *[1]Dept. of Electronics, Information and Bioengineering, Politecnico di Milano, Italy, [2]Dept. of Electronics and Telecommunications, Politecnico di Torino, Italy, [3] Dept. of Information Technology, IDLab, Ghent University - imec, Belgium*

Modeling of Eye Diagram Height in High-Speed Links via Support Vector Machine

R. Trinchero, F. G. Canavero, *EMC Group, Department of Electronics and Telecommunications, Politecnico di Torino, Italy*

Parameterized Macromodeling of Stochastic Linear Systems for Frequency- and Time-Domain Variability Analysis

Y. Ye[1], D. Spina[1], G. Antonini[2], T. Dhaene[1], *[1]IDLab, Department of Information Technology, Ghent University - imec, Belgium; [2]UAq EMC Laboratory, Dipartimento di Ingegneria Industriale e dell'Informazione e di Economia, Universita degli Studi dell'Aquila, Italy.*

Machine Learning Methodology for Inferring Network S-parameters in the Presence of Variability

X. Ma, M. Raginsky, A. C. Cangellaris, *Department of Electrical and Computer Engineering University of Illinois, USA*

Session 4: Power Delivery Networks

Power Integrity Challenges of Re-desigining a Mobile SoC with Fully Integrated Voltage Regulator to IoT Applications,

Y. F. Shen, *Internet of Things Group, Intel Corporation, Chandler, USA*

An On-Chip Load Model for Off-Chip PDN Analysis Considering Interdependency Between Supply Voltage, Current Profile and Clock Latency

J. Chen [1], T. Kanamoto[2], H. Kando[3], M. Hashimoto[1], *[1]Osaka University Osaka, Japan; [2]Hirosaki University Aomori, Japan; [3]Murata Manufacturing Co., Ltd. Kyoto, Japan*

A Robust Power Delivery Design Strategy For Platform on DIMM

D. M. García-Mora[1], J. Kar[2], I. Mendez-Soriano[1], H. Morales-Espinosa[1], *[1]Datacenter Package and Power Solutions Intel Guadalajara Design Center Guadalajara, Mexico; [2]Datacenter Package and Power Solutions Intel Corporation Santa Clara, CA, USA.*

Optimizing Phase Settings of High-Frequency Voltage Regulators for Power Delivery Applications

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Optimization of On-Package Decoupling Capacitors Considering System Variables

A. Sanna, G. Graziosi, *Back-End Manufacturing and Technology R&D, STMicroelectronics, Agrate Brianza, Italy*

Session 5: Nano, Optical and Wireless Interconnects

Integrated Dipole Antennas and Propagation Channel on Siliconin Ka Band for WiNoC Applications

I. El Masri, T. Le Gouguec, P-M. Martin, R. Allanic, C. Quendo, *Lab-STICC/Université de Brest (UBO) UMR CNRS 6285 BREST, France*

Electrical properties of a graphene nanoplatelets composite as interposer for electronic packages

A. Maffucci[1], L. Ferrigno[1], M.D. Migliore[1], D. Pinchera[1], F. Schettino[1], F. Micciulla[2], S. Bellucci[2], S. Maksimenko[3], A. Paddubskay[3], *[1,2]D.I.E.I., University of Cassino and Southern Lazio, Cassino, Italy ; [3]Institute for Nuclear Problems, Belarusian State University, Minsk, Belarus*

A Comparison of Higher-Order Graded-Index MMI-Based Splitters in Thin Glass Sheets for PCB Integration

J-P. Roth, T. Kühler, E. Griese, *University of Siegen, Theoretical Electrical Engineering and Photonics H; Siegen, Germany*

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Suppression of Noise from Digital-to-Analog Coupling in Shielding Cavity

H-W. Chan, R-B. Wu, *EDAP Laboratory, Graduate Institute of Communication Engineering National Taiwan University, Taipei, Taiwan*

Miniaturized Wide-and Dual-Band Multilayer Electromagnetic Bandgap For Antenna Isolation and on-Package/PCB Noise Suppression

P. Bantavis, M. Le Roy, A. Perennec, R. Lababidi, D. Le Jeune, *Lab-STICC, UMR CNRS 6285, Université de Brest (UBO)/ENSTA-Bretagne, Brest, France*

Session 7: Equalization techniques

Direct Prediction of Linear Equalization Coefficients Using Raised Cosine Pulse Shaping in Frequency Domain

T. Wendt, T. Reuschel, C. Schuster, *Hamburg University of Technology, Institute of Electromagnetic Theory, Hamburg, Germany*

DDR5 Design Challenges

N. Bhagwath[1], R. Wolff[2], S. Ikeda[3], E. Fujine[4], R. Shibata[4], Y. Sugaya[3], M. Ono[3], *[1]Mentor Graphics, a Siemens Business, Fremont, USA; [2]Micron Technology Boise, USA ; [3]Socionext Yokohama, Japan ; [4]Socionext Kasugai, Japan*

An Eye Diagram Improvement Method using Simulation Annealing Algorithm

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Session 8: Measurements and characterization

Usage of ESD Detector Circuit for Analyzing Soft Failures in IC cores

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Modelling and Validation of High-Current Surface-Mount Current-Sense Resistor

J. Bačmaga[1], R. Blečić[2], R. Gillon[3], A. Barić[1], *[1]University of Zagreb, Faculty of Electrical Engineering and Computing, Zagreb, Croatia; [2] KU Leuven, ESAT-TELEMIC, Leuven, Belgium; [3]ON Semiconductor, Westerring Oudenaarde, Belgium*

Fast and Robust RF Characterization Method of Insulators used in High Speed Interconnects Networks

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In-Depth Characterization of a Dielectric Waveguide for mmW Transmission Line Applications

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Impact of Chip and Interposer PDN to Eye Diagram in High Speed Channels

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Impact of On-Chip Multi-Layered Inductor on Signal and Power Integrity of Underlying Power-Ground Net

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TECHNICAL PROGRAM: POSTER PAPERS

Impact of the Doped Areas Sizes in the Performances of Microwave SPST Switches Integrated in a Silicon Substrate

R. Allanic[1], D. Le Berre[1], Y. Quere[1], C. Quendo[1], D. Chouteau[2], V. Grimal[2], D. Valente[2], J. Billoue[2], *[1]Lab-STICC, Université de Brest (UBO) UMR CNRS 6285, Brest, France ; [2]Laboratoire GREMAN", Université de Tours, France.*

Eye Diagram Estimation and Equalizer Design Method for PAM4

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Powering a Remote Board and Sensors in an extreme environment - an optical solution

C. Diouf[1], L. Ghisa[1], R. Hamie[1], V. Quintard[1], M. Guegan[1], A. Perennou[1], L. Gautier[2], M. Tardivel[2], S. E. Barbot[2], F. Colas[2], *[1]Lab-STICC/ ENIB, UMR CNRS 6285 Brest, France, [2]IFREMER/RDT Centre de Brest, France*

Evaluation and Comparison of Mounted Inductance for Decoupling Capacitor

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CMOS Integrated 1 GHz Ring Oscillator with Injection-Locked Frequency Divider for Low Power PLL

J. Park, S. Chun, H. Choi, N. Kim, *School of ECE, Chungbuk National University Cheong-ju, Korea.*

Impedance Measurement in Operating Conditions for PLC Applications

S. Sabo[1], L. Pace [1], J-C. Le Bunetel[3], A-S. Descamps[2], C. Batard[2], N. Idir[1], O. Mahamane, *[1]University of Lille France, [2]University of Nantes France; [3]University of Tours, France*

Assessment of Coupled Transmission Lines Embedded Between Imperfectly Matched Differential Circuit Stages

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Analysis of PSIJ in the Presence of both Ground-Bounce and Transmission Media

J. Narayan Tripathi[1], A. Jain [2], M. Marinkovic[2], R. Achar[2], *[1]TD&P, STMicroelectronics, INDIA. [2]Department of Electronics, Carleton University, Ottawa, Canada.*

Simulation of Nonuniform Coupled Transmission Lines using approximated S-Parameters Model.

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