

# **2018 15th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD 2018)**

**Prague, Czech Republic  
2 – 5 July 2018**



**IEEE Catalog Number: CFP1810S-POD  
ISBN: 978-1-5386-5154-4**

**Copyright © 2018 by the Institute of Electrical and Electronics Engineers, Inc.  
All Rights Reserved**

*Copyright and Reprint Permissions:* Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

***\*\*\* This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP1810S-POD
ISBN (Print-On-Demand):	978-1-5386-5154-4
ISBN (Online):	978-1-5386-5153-7

**Additional Copies of This Publication Are Available From:**

Curran Associates, Inc  
57 Morehouse Lane  
Red Hook, NY 12571 USA  
Phone: (845) 758-0400  
Fax: (845) 758-2633  
E-mail: [curran@proceedings.com](mailto:curran@proceedings.com)  
Web: [www.proceedings.com](http://www.proceedings.com)

CURRAN ASSOCIATES INC.  
**proceedings**  
.com

# Table of Contents

<b>Welcome</b>	xiii
<b>Committees</b>	xv
<b>Social Events</b>	xix
<b>Plenaries</b>	xxi
<b>Regular Papers</b>	
<b>Session: Applications of Modeling and Design Techniques</b>	
<b>Bringing Analog Design Tools to Security: Modeling and Optimization of a Low Area Probing Detector</b> <i>A. Herrmann, M. Weiner, M. Pehl, H. Graeb</i> Technical University of Munich, Germany	1
<b>Reliability Based Hardware Trojan Design Using Physics-Based Electromigration Models</b> <i>C. Cook, S. Sadiqbatcha, Z. Sun, S. Tan</i> University of California at Riverside, United States	5
<b>Metamodel-Based Performance Evaluation for an Electromechanical Automotive System</b> <i>C. Forster, J. Kirscher</i> Infineon Technology, Germany	9
<b>Analysis and Modeling of a Novel SDR-based High-Precision Positioning System</b> <i>C. Talarico<sup>1</sup>, G. Piccinni<sup>2</sup>, G. Avitabile<sup>2</sup>, G. Coviello<sup>2</sup></i> <sup>1</sup> Gonzaga University, United States, <sup>2</sup> Politecnico di Bari, Italy	13
<b>Digital Architecture and ASIC Implementation of Wideband Delta DOR Spacecraft Onboard Tracker</b> <i>G. Cardarilli<sup>1</sup>, L. Di Nunzio<sup>1</sup>, R. Fazzolari<sup>1</sup>, M. Matta<sup>1</sup>, M. Re<sup>1</sup>, A. Nannarelli<sup>2</sup>, D. Gelfusa<sup>3</sup>, S. Lorenzo<sup>3</sup>, S. Spanò<sup>1</sup></i> <sup>1</sup> University of Roma Tor Vergata, Italy, <sup>2</sup> Danish Technical University Lyngby, Italy, <sup>3</sup> Thales Alenia Space, Italy	17
<b>Session: Variability and Test</b>	
<b>Accelerating Electromigration Wear-Out Effects Based on Configurable Sink-Structured Wires</b> <i>S. Sadiqbatcha, C. Cook, Z. Sun, S. Tan</i> University of California at Riverside, United States	21
<b>Variability Analysis Tool for CMOS Analog/RF Circuits: VariAnT</b> <i>E. Afacan, Y. Avci, O. Demirbas</i> Kocaeli University, Turkey	25

<b>Automated Massive RTN Characterization Using a Transistor Array Chip</b> <i>P. Saraza-Canflanca<sup>1</sup>, J. Diaz-Fortuny<sup>2</sup>, R. Castro-Lopez<sup>1</sup>, E. Roca<sup>1</sup>, J. Martin-Martinez<sup>2</sup>, R. Rodriguez<sup>2</sup>, M. Nafria<sup>2</sup>, F. Fernández<sup>1</sup>, A. Toro-Frias<sup>1</sup></i> <sup>1</sup> IMSE-CNM, Spain, <sup>2</sup> Universitat Autònoma de Barcelona, Spain	29
<b>Testability Analysis Based on Complex-Field Fault Modeling</b> <i>G. Fontana, F. Grasso, A. Luchetta, S. Manetti, M. Piccirilli, A. Reatti</i> University of Firenze, Italy	33
<b>The Reactance Transformation for Near Sidelobes Reduction: A Comparison of Windowing Techniques</b> <i>P. Burrascano<sup>1</sup>, S. Laureti<sup>1</sup>, M. Ricci<sup>2</sup></i> <sup>1</sup> University of Perugia, Italy, <sup>2</sup> University of Calabria, Italy	37
<b>Session: SMACD EDA Competition I</b>	
<b>An Analog/RF Circuit Synthesis and Design Assistant Tool for Analog IP: DATA-IP</b> <i>E. Kaya<sup>1</sup>, E. Afacan<sup>2</sup>, G. Dundar<sup>1</sup></i> <sup>1</sup> Bogazici University, Turkey, <sup>2</sup> Kocaeli University, Turkey	41
<b>Antenna Modeling Technique for Digital Communication Systems</b> <i>M. Almotery, M. Sobhy, J. Batchelor</i> University of Kent, United Kingdom	45
<b>SETA: A CAD Tool for Single Event Transient Analysis and Mitigation on Flash-based FPGAs</b> <i>S. Azimi<sup>1</sup>, B. Du<sup>1</sup>, L. Sterpone<sup>1</sup>, D. Merodio Codinachs<sup>2</sup>, L. Cattaneo<sup>3</sup></i> <sup>1</sup> Politecnico di Torino, Italy, <sup>2</sup> European Space Agency, Netherlands, <sup>3</sup> Microsemi, Italy	49
<b>Special Session: Latest Advances in Variability Impact on Devices and Circuits Functionality</b>	
<b>A Model Parameter Extraction Methodology Including Time-dependent Variability for Circuit Reliability Simulation</b> <i>J. Diaz-Fortuny<sup>1</sup>, P. Saraza-Canflanca<sup>2</sup>, A. Toro-Frias<sup>2</sup>, R. Castro-Lopez<sup>2</sup>, J. Martin-Martinez<sup>1</sup>, E. Roca<sup>2</sup>, R. Rodriguez<sup>1</sup>, F. Fernández<sup>2</sup>, M. Nafria<sup>1</sup></i> <sup>1</sup> Universitat Autònoma de Barcelona, Spain, <sup>2</sup> IMSE-CNM, Spain	53
<b>Voltage Adaptation Under Temperature Variation</b> <i>H. Amrouch<sup>1</sup>, B. Khaleghi<sup>2</sup>, J. Henkel<sup>1</sup></i> <sup>1</sup> Karlsruhe Institute of Technology, Germany, <sup>2</sup> University of California at San Diego, United States	57
<b>Lifetime Calculation Using a Stochastic Reliability Simulator for Analog ICs</b> <i>A. Toro-Frías<sup>1</sup>, P. Martín-Lloret<sup>1</sup>, J. Martin-Martinez<sup>2</sup>, R. Castro-Lopez<sup>1</sup>, R. Rodriguez<sup>2</sup>, E. Roca<sup>1</sup>, M. Nafria<sup>2</sup>, F. Fernández<sup>1</sup></i> <sup>1</sup> IMSE-CNM, Spain, <sup>2</sup> Universitat Autònoma de Barcelona, Spain	61
<b>Yield Approximation of Analog Integrated Circuits under Time-Dependent Variability</b> <i>T. Hillebrand, M. Taddiken, S. Paul, D. Peters-Drolshagen</i> University of Bremen, Germany	65
<b>Optimizing Datapaths for Near Threshold Computing</b> <i>M. Golanbari, M. Tahoori</i> Karlsruhe Institute of Technology, Germany	69
<b>Design Considerations of an Sram Array for the Statistical Validation of Time-Dependent Variability Models</b> <i>P. Saraza-Canflanca<sup>1</sup>, D. Malagon<sup>1</sup>, F. Passos<sup>1</sup>, A. Toro-Frías<sup>1</sup>, J. Nunez<sup>1</sup>, J. Diaz-Fortuny<sup>2</sup>, R. Castro-Lopez<sup>1</sup>, E. Roca<sup>1</sup>, J. Martin-Martinez<sup>2</sup>, R. Rodriguez<sup>2</sup>, M. Nafria<sup>2</sup>, F. Fernández<sup>1</sup></i> <sup>1</sup> IMSE-CNM, Spain, <sup>2</sup> Universitat Autònoma de Barcelona, Spain	73

**Session: Design with Non-Conventional and Emerging Devices****Design of Logic Gates by Using a Four-Gate Thin Film Transistor (FG TFT)***S. Ilik, F. Gencer, M. Yelten*

Istanbul Technical University, Turkey

77

**Inverting versus Non-Inverting Dynamic Logic for Two-Phase Latch-free Nanopipelines***H. Quintero, M. Jiménez, M. Avedillo, J. Nunez*

IMSE-CNM, Spain

81

**Memristive TaOx-based Median Filter Design for Image Processing Application***A. Sasi, A. Amirsoleimani, M. Ahmadi, A. Ahmadi*

University of Windsor, Canada

85

**Session: Machine Learning and Knowledge Based Design****Tunable Floating-Point for Embedded Machine Learning Algorithms Implementation***M. Franceschi<sup>1</sup>, A. Nannarelli<sup>2</sup>, M. Valle<sup>1</sup>*<sup>1</sup>University of Genova, Italy, <sup>2</sup>Technical University of Denmark, Denmark

89

**Approximate Fully Connected Neural Network Generation***T. Ayhan, M. Altun*

Istanbul Technical University, Turkey

93

**Modelling Switched-Capacitor DC-DC Converters with Signal Transition Graphs***D. Li, D. Shang, F. Xia, A. Yakovlev*

Newcastle University, United Kingdom

97

**A Novel Multiple Membership Function Generator for Fuzzy Logic Systems***R. Khayatzadeh, M. Yelten*

Istanbul Technical University, Turkey

101

**Session: Modeling****Parameter Extraction Method Using Hybrid Artificial Bee Colony Algorithm for an OFET Compact Model***N. Akkan<sup>1</sup>, M. Altun<sup>2</sup>, H. Sede<sup>1</sup>*<sup>1</sup>Yildiz Technical University, Turkey, <sup>2</sup>Istanbul Technical University, Turkey

105

**Compact Drain Current Model of Nanoscale FinFET Considering Short Channel Effect in Ballistic Transport Regime***M. Bae, C. Park, I. Yun*

Yonsei University, South Korea

109

**Three-Dimensional Modeling of Insulin Pen for Multi-Electrode Capacitive Sensing***M. Paun, C. Dehollain*

Swiss Federal Institute of Technology (EPFL), Switzerland

113

**Behavioral Switching Loss Modeling of Inverter Modules***K. Stoyka, R. Pessinatti Ohashi, N. Femia*

University of Salerno, Italy

117

**Modeling and Simulation of Digital Phase-Locked Loop in Simulink***N. Parkalian, M. Robens, C. Grewing, S. van Waasen, V. Christ, D. Liebau, P. Muralidharan, D. Nielinger, U. Yegin, A. Zambanini*

Juelich Forschungszentrum, Germany

121

**Session: Circuit Synthesis****Design Space Exploration of CMOS Cross-Coupled LC Oscillators via RF Circuit Synthesis***E. Afacan<sup>1</sup>, G. Dunder<sup>2</sup>*<sup>1</sup>Kocaeli University, Turkey, <sup>2</sup>Bogazici University, Turkey

125

<b>Design and Optimization of a Class-C/D VCO for Ultra-Low-Power IoT and Cellular Applications</b> <i>R. Martins<sup>1</sup>, N. Lourenço<sup>1</sup>, N. Horta<sup>1</sup>, J. Yin<sup>2</sup>, P. Mak<sup>2</sup>, R. Martins<sup>2</sup></i> <sup>1</sup> Instituto de Telecomunicações, Universidade de Lisboa, Portugal, <sup>2</sup> University of Macau, China	129
<b>On the Exploration of Promising Analog IC Designs via Artificial Neural Networks</b> <i>N. Lourenço, J. Rosa, R. Martins, H. Aidos, R. Póvoa, A. Canelas, N. Horta</i> Instituto de Telecomunicações, Universidade de Lisboa, Portugal	133
<b>Expected Improvement-Based Optimization Approach for the Optimal Sizing of a CMOS Operational Transconductance Amplifier</b> <i>N. Drira<sup>1</sup>, M. Kotti<sup>2</sup>, M. Fakhfakh<sup>2</sup>, P. Siarry<sup>3</sup>, E. Tlelo-Cuautle<sup>4</sup></i> <sup>1</sup> University of Gabès, Tunisia, <sup>2</sup> University of Sfax, Tunisia, <sup>3</sup> University of Paris-Est, France, <sup>4</sup> INAOE, Mexico	137
<b>Linearizing the Transconductance of an OTA Through the Optimal Sizing by Applying NSGA-II</b> <i>L. De La Fraga<sup>1</sup>, E. Tlelo-Cuautle<sup>2</sup></i> <sup>1</sup> Cinvestav, Mexico, <sup>2</sup> INAOE, Mexico	141
<b>Session: SMACD EDA Competition II</b>	
<b>Lithography Hotspots Detection Using Deep Learning</b> <i>V. Borisov, J. Scheible</i> Reutlingen University, Germany	145
<b>Impact Rating of Layout Parasitics in Mixed-Signal Circuits: Finding a Needle in a Haystack</b> <i>G. Gläser<sup>1</sup>, M. Grabmann<sup>1</sup>, D. Nuernbergk<sup>2</sup></i> <sup>1</sup> IMMS, Germany, <sup>2</sup> Melexis, Germany	149
<b>ToPoliNano and MagCAD: A Complete Framework for Design and Simulation of Digital Circuits Based on Emerging Technologies</b> <i>U. Garlando, F. Riente, D. Vergallo, M. Graziano, M. Zamboni</i> Politecnico di Torino, Italy	153
<b>ReSeMBleD Methods for Response Surface Model Behavioral Description</b> <i>M. Taddiken, S. Paul, D. Peters-Drolshagen</i> University of Bremen, Germany	157
<b>Special Session: New Solutions for Analog and Radio-Frequency Layout Synthesis</b>	
<b>Handling the Effects of Variability and Layout Parasitics in the Automatic Synthesis of LNAs</b> <i>F. Passos<sup>1</sup>, E. Roca<sup>1</sup>, R. Castro-Lopez<sup>1</sup>, F. Fernández<sup>1</sup>, R. Martins<sup>2</sup>, N. Lourenço<sup>2</sup>, R. Póvoa<sup>2</sup>, A. Canelas<sup>2</sup>, N. Horta<sup>2</sup></i> <sup>1</sup> IMSE-CNM, Spain, <sup>2</sup> Instituto de Telecomunicações, Universidade de Lisboa, Portugal	161
<b>ABSYNTH: A Comprehensive Approach for Full Front to Back Analog Design Automation</b> <i>A. Kammara, A. Koenig</i> Technical University of Kaiserslautern, Germany	165
<b>Spec-to-Layout Automation Flow for Buck Converters with Current-Mode Control in SOC Applications</b> <i>H. Hsu, W. Chen, L. Yeh, C. Liu</i> National Central University, Taiwan	169
<b>Classifying Analog and Digital Circuits with Machine Learning Techniques Toward Mixed-Signal Design Automation</b> <i>G. Liou, S. Wang, Y. Su, M. Lin</i> National Chung Cheng University, Taiwan	173

<b>Mismatch-Aware Placement of Device Arrays Using Genetic Optimization</b> <i>I. Nashaat<sup>1</sup>, I. Mohammed<sup>2</sup>, M. Dessouky<sup>3</sup>, H. Said<sup>4</sup></i> <sup>1</sup> Si-Vision, Egypt, <sup>2</sup> Mipex, Egypt, <sup>3</sup> Mentor Graphics Egypt, Egypt, <sup>4</sup> Ain Shams University, Egypt	177
<b>On Closing the Gap Between Pre-Simulation and Post-Simulation Results in Nanometer Analog Layouts</b> <i>P. Pan<sup>1</sup>, H. Huang<sup>1</sup>, C. Huang<sup>1</sup>, A. Patyal<sup>1</sup>, T. Yang<sup>2</sup>, H. Chen<sup>1</sup></i> <sup>1</sup> National Chiao Tung University, Taiwan, <sup>2</sup> TSMC, Taiwan	181
<b>Session: High Frequency</b>	
<b>A 20-dB Gain Two-Stage Low-Noise Amplifier with High Yield for 5-GHz Applications</b> <i>A. Canelas, R. Póvoa, R. Martins, N. Lourenço, J. Guilherme, N. Horta</i> Instituto de Telecomunicações, Universidade de Lisboa, Portugal	185
<b>Analytical Method for Ultra-Low Power UWB Low-Noise Amplifiers</b> <i>A. Elsayed<sup>1</sup>, M. Abutaleb<sup>1</sup>, M. Eladawy<sup>1</sup>, H. Ragai<sup>2</sup></i> <sup>1</sup> Helwan University, Egypt, <sup>2</sup> Ain Shams University, Egypt	189
<b>Temperature Performance of Meander-Type Inductor in Silicon Technology</b> <i>A. Pajkanovic<sup>1</sup>, G. Stojanovic<sup>2</sup></i> <sup>1</sup> University of Banja Luka, Bosnia and Herzegovina, <sup>2</sup> University of Novi Sad, Serbia	193
<b>An Universal Model for Milimeter-Wave Integrated Transformers</b> <i>J. Hermann, D. Bierbuesse, R. Negra</i> RWTH Aachen University, Germany	197
<b>On the Sparsification of the Reluctance Matrix in RLCK Circuit Transient Analysis</b> <i>C. Antoniadis, N. Evmorfopoulos, G. Stamoulis</i> University of Thessaly, Greece	201
<b>Session: Simulation</b>	
<b>Efficient Hotspot Thermal Simulation via Low Rank Model Order Reduction</b> <i>G. Floros, N. Evmorfopoulos, G. Stamoulis</i> University of Thessaly, Greece	205
<b>A Combinatorial Multigrid Preconditioned Iterative Method for Large Scale Circuit Simulation on GPUs</b> <i>D. Garyfallou, N. Evmorfopoulos, G. Stamoulis</i> University of Thessaly, Greece	209
<b>Statistical Simulations of Delay Propagation in Large Scale Circuits Using Graph Traversal and Kernel Function Decomposition</b> <i>J. Freeley, D. Mishaghi, T. Brazil, E. Blokhina</i> University College Dublin, Ireland	213
<b>LUT-Based Stochastic Modeling for Non-Normal Performance Distributions</b> <i>M. Taddiken, T. Hillebrand, S. Paul, D. Peters-Drolshagen</i> University of Bremen, Germany	217
<b>Advanced Modeling Methodology for Expedient RF SoC Verification and Performance Estimation</b> <i>F. Speicher, J. Meier, C. Beyerstedt, R. Wunderlich, S. Heinen</i> RWTH Aachen University, Germany	221
<b>Special Session: Modeling, Design and Control of Power Converters with Non Linear Passive Power Components</b>	

<b>Fast Converter Simulation Method Including Parasitic Nonlinear Capacitances</b> <i>E. Schmidt, T. Duerbaum</i> Friedrich-Alexander University of Erlangen-Nuremberg, Germany	225
<b>Pulse Compression for Ferrite Inductors Modeling in Moderate Saturation</b> <i>P. Burrascano<sup>1</sup>, G. Di Capua<sup>2</sup>, N. Femia<sup>2</sup>, S. Laureti<sup>1</sup>, M. Ricci<sup>3</sup></i> <sup>1</sup> University of Perugia, Italy, <sup>2</sup> University of Salerno, Italy, <sup>3</sup> University of Calabria, Italy	229
<b>Accurate Modeling of Inductors Working in Nonlinear Region in Switch-Mode Power Supplies with Different Load Currents</b> <i>A. Oliveri, M. Lodi, M. Storable</i> University of Genova, Italy	233
<b>A Temperature Dependent Non-Linear Inductor Model for a DC/DC Boost Converter</b> <i>D. Scirè<sup>1</sup>, S. Rosato<sup>1</sup>, G. Lullo<sup>1</sup>, G. Vitale<sup>2</sup></i> <sup>1</sup> University of Palermo, Italy, <sup>2</sup> CNR, Italy	237
<b>Loss Behavioral Modeling for Ferrite Inductors</b> <i>G. Di Capua, N. Femia, K. Stoyka</i> University of Salerno, Italy	241
<b>Geometric Form Factors-Based Power Transformers Design</b> <i>G. Di Capua, N. Femia</i> University of Salerno, Italy	245
<b>Session: Data Conversion and Signal Processing</b>	
<b>Controlled-Oscillator Optimization for Highly-Digital CMOS Time-Based Sensor-to-Digital Converter Architectures</b> <i>E. Sacco<sup>1</sup>, J. Marin<sup>1</sup>, J. Vergauwen<sup>2</sup>, G. Gielen<sup>1</sup></i> <sup>1</sup> Katholieke Universiteit Leuven, Belgium, <sup>2</sup> Melexis, Belgium	249
<b>Analysis and Simulation of Chopper Stabilization Techniques Applied to Delta-Sigma Converters</b> <i>A. Catania, A. Ria, S. Del Cesta, M. Piotta, P. Bruschi</i> University of Pisa, Italy	253
<b>New Reconfigurable Universal SISO Biquad Filter Implemented by Advanced CMOS Active Elements</b> <i>R. Sotner<sup>1</sup>, L. Langhammer<sup>1</sup>, O. Domansky<sup>1</sup>, J. Petrzela<sup>1</sup>, J. Jerabek<sup>1</sup>, T. Dostal<sup>2</sup></i> <sup>1</sup> Brno University of Technology, Czech Republic, <sup>2</sup> College of Polytechnics Jihlava, Czech Republic	257
<b>System of Standard Approximations for Optimum Frequency Filter Design</b> <i>K. Hajek</i> University of Defence Brno, Czech Republic	261
<b>Design and Error Analysis of Inductance Multiplier via Symbolic Algorithms</b> <i>J. Vavra<sup>1</sup>, D. Biolek<sup>1</sup>, Z. Kolka<sup>2</sup></i> <sup>1</sup> University of Defence Brno, Czech Republic, <sup>2</sup> Brno University of Technology, Czech Republic	265
<b>A Low-power, Bootstrapped Sample and Hold Circuit with Extended Input Range for Analog-to-Digital Converters in CMOS 0.18 <math>\mu\text{m}</math></b> <i>A. Mohammadi, M. Chahardori</i> Islamic Azad University, Iran	269
<b>Poster Session</b>	
<b>A Cell-Based Fractional-N Phase-Locked Loop Compiler</b> <i>C. Lee, S. Huang</i> National Tsing Hua University, Taiwan	273

<b>Mixed Design of SPAD Array Based TOF for Depth Camera and Unmanned Vehicle Applications</b>	
<i>W. Shi, A. Pan</i>	
Shenzhen University, China	277
<b>Modeling of Reference Injection Based Low-Power All-Digital Phase-Locked Loop for Bluetooth Low-Energy Applications in LabVIEW</b>	
<i>M. Rehman, N. Ahmad, I. Ali, S. Oh, A. Hejazi, K. Lee</i>	
Sungkyunkwan University, South Korea	281
<b>SC Filter Optimization Performance by Hybrid Simplex Algorithm</b>	
<i>J. Náhlík, J. Hospodka, O. Subrt</i>	
CTU in Prague, Czech Republic	285
<b>A Low Power Priority Encoding Technique with Address-Encoder and Reset-Decoder for an Improved Hierarchical Asynchronous Detector</b>	
<i>C. Lee, C. Kim, H. Lim, S. Kim, M. Song</i>	
Dongguk University, South Korea	289
<b>Kriging Metamodeling-Assisted Multi-Objective Optimization of CMOS Current Conveyors</b>	
<i>M. Kotti<sup>1</sup>, M. Fakhfakh<sup>2</sup>, E. Tlelo-Cuautle<sup>3</sup></i>	
<sup>1</sup> University of Sousse, Tunisia, <sup>2</sup> University of Sfax, Tunisia, <sup>3</sup> INAOE, Mexico	293
<b>2D Bifurcations and Chaos in Nonlinear Circuits: A Parallel Computational Approach</b>	
<i>W. Marszalek<sup>1</sup>, J. Sadecki<sup>2</sup></i>	
<sup>1</sup> Rutgers University, United States, <sup>2</sup> Opole University of Technology, Poland	297
<b>System-Level Behavioral Model of a 12-bit 1.5-bit per Stage Pipelined ADC Based on Verilog-AMS</b>	
<i>V. Ponce-Hinestroza<sup>1</sup>, V. Gonzalez-Diaz<sup>1</sup>, J. Castaneda Camacho<sup>1</sup>, G. Mino-Aguilar<sup>1</sup>, E. Bonizzoni<sup>2</sup></i>	
<sup>1</sup> Benemérita Universidad Autónoma de Puebla, Mexico, <sup>2</sup> University of Pavia, Italy	301
<b>Reconfiguring Passive Linear Systems</b>	
<i>C. Onete<sup>1</sup>, M. Onete<sup>2</sup></i>	
<sup>1</sup> NXP Semiconductors, Netherlands, <sup>2</sup> University of Limoges, France	305
<b>Author Index</b>	309