

2018 IEEE International Test Conference in Asia (ITC-Asia 2018)

**Harbin, China
15-17 August 2018**



**IEEE Catalog Number: CFP18UWH-POD
ISBN: 978-1-5386-5181-0**

**Copyright © 2018 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP18UWH-POD
ISBN (Print-On-Demand):	978-1-5386-5181-0
ISBN (Online):	978-1-5386-5180-3

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

2018 IEEE International Test Conference in Asia ITC-Asia 2018

Table of Contents

Foreword	ix
Organizing Committee	x
Steering Committee	xi
Program Committee	xii
Tutorials	xiv
Keynotes	xvii

Session 1A: ATPG

Generating Compact Test Patterns for Stuck-at Faults and Transition Faults in One ATPG Run	1
<i>Yi-Cheng Kung (National Cheng Kung University, Taiwan), Kuen-Jong Lee (National Cheng Kung University, Taiwan), and Sudhakar M. Reddy (University of Iowa, USA)</i>	
Efficient Cell-Aware Defect Characterization for Multi-bit Cells	7
<i>Ruifeng Guo (Synopsys Inc.), Brian Archer (Synopsys Inc.), Kevin Chau (Synopsys Inc.), and Xiaolei Cai (Synopsys Inc.)</i>	
Automatic Generation of In-Circuit Tests for Board Assembly Defects	13
<i>Harm van Schaaik (Prodrive Technologies), Martien Spierings (Prodrive Technologies), and Erik Jan Marinissen (IMEC)</i>	

Session 1B: Reliability

RRAM-Based Neuromorphic Hardware Reliability Improvement by Self-Healing and Error Correction	19
<i>Jia-Yun Hu (National Tsing Hua University (NTHU), Taiwan), Kuan-Wei Hou (National Tsing Hua University (NTHU), Taiwan), Chih-Yen Lo (Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan), Yung-Fa Chou (Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan), and Cheng-Wen Wu (National Tsing Hua University (NTHU), Taiwan)</i>	
MTTF-Aware Reliability Task Scheduling for PIM-Based Heterogeneous Computing System	25
<i>Desong Pang (Hefei University of Technology, Hefei), Dawen Xu (Hefei University of Technology, Hefei), Ying Wang (Institute of Computing Technology, Chinese Academy of Sciences, Beijing), and Huaguo Liang (Hefei University of Technology, Hefei)</i>	

DVFS Binning Using Machine-Learning Techniques .31.....	
<i>Keng-Wei Chang (National Chiao Tung University, Hsinchu, Taiwan), Chun-Yang Huang (National Chiao Tung University, Hsinchu, Taiwan), Szu-Pang Mu (National Chiao Tung University, Hsinchu, Taiwan), Jian-Min Huang (Independent), Shi-Hao Chen (Independent), and Mango C.-T. Chao (National Chiao Tung University, Hsinchu, Taiwan)</i>	

Session 2A: DFX & LBIST

Periodic Online LBIST Considerations for a Multicore Processor .37.....	
<i>Teresa McLaurin (Arm)</i>	
Implementing Design-for-Test Within a Tile-Based Design Methodology - Challenges and Solutions .43.....	
<i>Venkat Yellapragada (Xilinx), Suresh Raman (Xilinx), Banadappa Shivaray (Xilinx), Luc Romain (Mentor, A Siemens Business), Benoit Nadeau-Dostie (Mentor, A Siemens Business), Martin Keim (Mentor, A Siemens Business), Jean-François Côté (Mentor, A Siemens Business), Albert Au (Mentor, A Siemens Business), Giri Podichetty (Mentor, A Siemens Business), and Ashok Anbalan (Mentor, A Siemens Business)</i>	
Radiation Hardening by Design of a Novel Double-Node-Upset-Tolerant Latch Combined with Layout Technique .49.....	
<i>Aibin Yan (Anhui University), Zhile Chen (Anhui University), Zhengfeng Huang (Hefei University of Technology), Xiangsheng Fang (Hefei University of Technology), Maoxiang Yi (Hefei University of Technology), and Jing Guo (North University of China)</i>	

Session 2B: Verification & Validation

A Semi-Formal Technique to Generate Effective Test Sequences for Reconfigurable Scan Networks .55.....	
<i>Riccardo Cantoro (Politecnico di Torino), Aleksa Damjanovic (Politecnico di Torino), Matteo Sonza Reorda (Politecnico di Torino), and Giovanni Squillero (Politecnico di Torino)</i>	
An Automatic Approach to Evaluate Assertions' Quality Based on Data-Mining Metrics .61.....	
<i>Tara Ghasempouri (Tallinn University of Technology), Siavoosh Payandeh Azad (Tallinn University of Technology), Behrad Niazmand (Tallinn University of Technology), and Jaan Raik (Tallinn University of Technology)</i>	
Skew-Aware Functional Timing Analysis Against Setup Violation for Post-Layout Validation .67.....	
<i>Pin-Ru Jhao (National Chiao Tung University), Denny C.-Y. Wu (National Chiao Tung University), and Charles H.-P. Wen (National Chiao Tung University)</i>	

Session 3A: Hardware Security

Leveraging DRAM Refresh to Protect the Memory Timing Channel of Cloud Chip Multi-processors .73.....	
<i>Ying Wang (State Key Laboratory of Computer Architecture, Institute of Computing Technology Chinese Academy of Sciences), Wen Li (State Key Laboratory of Computer Architecture, Institute of Computing Technology Chinese Academy of Sciences), Huawei Li (State Key Laboratory of Computer Architecture, Institute of Computing Technology Chinese Academy of Sciences), and Xiaowei Li (State Key Laboratory of Computer Architecture, Institute of Computing Technology Chinese Academy of Sciences)</i>	
Grey Zone in Pre-Silicon Hardware Trojan Detection .79.....	
<i>Jing Ye (State Key Laboratory of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences; University of Chinese Academy of Sciences), Yipei Yang (State Key Laboratory of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences; University of Chinese Academy of Sciences), Yue Gong (State Key Laboratory of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences; University of Chinese Academy of Sciences), Yu Hu (State Key Laboratory of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences; University of Chinese Academy of Sciences), and Xiaowei Li (State Key Laboratory of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences; University of Chinese Academy of Sciences)</i>	
Small Trojan Testing Using Bounded Model Checking .85.....	
<i>Ying Zhang (Tongji University, Shanghai, China), Lu Yu (Tongji University, Shanghai, China), Huawei Li (Institute of Computing Technology, Chinese Academy of Sciences, China), and Jianhui Jiang (Tongji University, Shanghai, China)</i>	

Session 3B: Analog Test

Low-Distortion One-Tone and Two-Tone Signal Generation Using AWG Over Full Nyquist Region .91.....	
<i>Tomonori Yanagida (Gunma University), Shohei Shibuya (Gunma University), Kosuke Machida (Gunma University), Koji Asami (Gunma University), and Haruo Kobayashi (Gunma University)</i>	
Accurate Spectral Testing with Impure Test Stimulus for Multi-tone Test .97.....	
<i>Yuming Zhuang (Qualcomm Inc) and Degang Chen (Iowa State University)</i>	
Cost-Effective High Purity Signal Generator Using Pre-distortion .103.....	
<i>Yuming Zhuang (Qualcomm Inc) and Degang Chen (Iowa State University)</i>	

Session 4A: Test Cost & Test Quality

Industrial Case Studies of SoC Test Scheduling Optimization by Selecting Appropriate EDT Architectures .109.....	
<i>Guoliang Li (Advanced Micro Devices), Henry Zhao (Advanced Micro Devices), Qinfu Yang (Advanced Micro Devices), Jun Qian (Advanced Micro Devices), and Yu Huang (Mentor, A Siemens Business)</i>	

Good Die Prediction Modelling from Limited Test Items .115.....	
<i>Takeru Nishimi (Kyushu Institute of Technology), Yasuo Sato (Kyushu Institute of Technology), Seiji Kajihara (Kyushu Institute of Technology), and Yoshiyuki Nakamura (Renesas Electronics Corporation)</i>	
X-Sources Analysis for Improving the Test Quality .121.....	
<i>Kun-Han Tsai (Mentor, A Siemens Business)</i>	

Session 4B: Error Detection & Tolerance

Error Indication Signal Collapsing for Implication-Based Concurrent Error Detection .127.....	
<i>Chih-Hao Wang (National Sun Yat-sen University, Kaohsiung, Taiwan), Chi-Hsuan Ho (National Sun Yat-sen University, Kaohsiung, Taiwan), and Tong-Yu Hsieh (National Sun Yat-sen University, Kaohsiung, Taiwan)</i>	
A No-Reference Error-Tolerability Test Methodology for Image Processing Applications .133.....	
<i>Tong-Yu Hsieh (National Sun Yat-sen University, Kaohsiung, Taiwan) and Chao-Ru Chen (National Sun Yat-sen University, Kaohsiung, Taiwan)</i>	
A Hierarchical Approach for Devising Area Efficient Concurrent Online Checkers .139.....	
<i>Behrad Niazmand (Tallinn University of Technology), Siavoosh Payandeh Azad (Tallinn University of Technology), Tara Ghasempouri (Tallinn University of Technology), Jaan Raik (Tallinn University of Technology), and Gert Jervan (Tallinn University of Technology)</i>	

Special Session: Design for Secure Chips and Systems

Balancing Testability and Security by Configurable Partial Scan Design .145.....	
<i>Xi Chen (University of Maryland, College Park), Omid Aramoon (University of Maryland, College Park), Gang Qu (University of Maryland, College Park), and Aijiao Cui (Harbin Institute of Technology Shenzhen Graduate School)</i>	
A Comprehensive Security System for Digital Microfluidic Biochips .151.....	
<i>Chun-Yu Lin (National Tsing Hua University), Juinn-Dar Huang (National Chiao Tung University), Hailong Yao (Tsinghua University), and Tsung-Yi Ho (National Tsing Hua University)</i>	

Author Index 157.....	
-----------------------	--