

2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2018)

**Austin, Texas, USA
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Program

Monday, September 24

Light breakfast (Zlotnik Family Ballroom 4 & 5 pre-function) 7:30 – 8:30

Session 1: Plenary (Zlotnik Family Ballroom 4)

Chairperson

Victor Moroz (Synopsis, USA)

	8:30 – 8:40	<p>Welcome and Opening Remarks</p> <p>Leonard F. Register (SISPAD 2018 Conference General Chair, and The University of Texas at Austin, USA)</p>	
1.1	8:40 – 9:30	<p>Plenary Talk: Atomistic Simulations, Tools to Gain Fundamental Understanding in Materials And Device Properties</p> <p>Geoffrey Pourtois (IMEC, Belgium)</p>	N/A

Break with snacks (Zlotnik Family Ballroom 4 & 5 pre-function) 9:30 – 9:50

Session 2: Quantum Transport (Zlotnik Family Ballroom 4)

Chairpersons

Sayed Hasan (Intel, USA)

Pierpaolo Palestri (University of Udine, Italy)

2.1	9:50 – 10:10	<p>Simulation of Quantum Current in Double Gate MOSFETs: Vortices in Electron Transport</p> <p>P. B. Vyas¹, M. L. Van de Put², and M. V. Fischetti^{1,2} (¹Department of Electrical Engineering and ²Department of Materials Science and Engineering, The University of Texas at Dallas, USA)</p>	1
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Chairpersons

Geert Eneman (IMEC, Belgium)

Blanka Magyari-Kope (Stanford University, USA)

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3.2	10:10 – 10:30	Physics-based Modelling of MoS₂: The Layered Structure Concept N/A Gioele Mirabelli, Paul K. Hurley, and Ray Duffy (Tyndall National Institute, University College Cork, Ireland)
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Chairpersons

Daniel Connelly (Atomera, USA)

Myung-Hee Na (IBM, USA)

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Chairpersons

Geoffrey Pourtois (IMEC, Belgium)

Mathieu Luisier (ETH Zurich, Switzerland)

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Break with snacks (Zlotnik Family Ballroom 4 & 5 pre-function) 3:00 – 3:20

Session 6: Process Defects and Interconnects (Zlotnik Family Ballroom 4)

Chairpersons

Jürgen Lorenz (Fraunhofer IISB, Germany)
Harsono Simka (Samsung, USA)

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		Harsono Simka (Samsung, Austin, TX, USA)	
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Chairpersons

Seong-Dong Kim (SK Hynix, Korea)

Uihui Kwon (Samsung, Korea)

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Tuesday, September 25

Light Breakfast (Zlotnik Family Ballroom 4 & 5 pre-function) 7:30 – 8:30

Session 8: Plenary (Zlotnik Family Ballroom 4)

Chairperson

David Esseni (University of Udine, Italy)

	8:30 – 8:40	SISPAD 2019 announcement David Esseni (SISPAD 2019 Conference Chair and University of Udine, Italy)
8.1	8:40 – 9:30	Plenary Talk: Status of Integrated Reactor and Feature Scale Modeling for Plasma-based Semiconductor Fabrication N/A Mark Kushner (University of Michigan, USA)

Break with snacks (Zlotnik Family Ballroom 4 & 5 pre-function) 9:30 – 9:50

Session 9: Negative Capacitance FETs and Tunneling FETs (Zlotnik Family Ballroom 4)

Chairpersons

Daniel Connelly (Atomera, USA)

Juan Duarte (University of California, Berkeley, USA)

9.1	9:50 – 10:20	Invited Talk: Negative-Capacitance FinFETs: Numerical Simulation, Compact Modeling and Circuit Evaluation 123 J. P. Duarte, Y.-K. Lin, Y.-H. Liao, A. Sachid, M.-Y. Kao, H. Agarwal, P. Kushwaha, K. Chatterjee, D. Kwon, H.-L. Chang, S. Salahuddin, and C. Hu (Dept. of Electrical Engineering and Computer Science, University of California, Berkeley, USA)
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Session 10: Power Switches and Thermal Analysis (Zlotnik Family Ballroom 5)

Chairpersons

Aaron Thean (National University of Singapore, Singapore)

Anh-Tuan Pham (Samsung, USA)

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Chairpersons

Sudarshan Narayanan (GlobalFoundries, USA)

Lado Filipovic (Technical University, Wien, Austria)

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Chairpersons

Geert Eneman (IMEC, Belgium)

Andrea Ghetti (Micron, Italy)

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Break with snacks (Zlotnik Family Ballroom 4 & 5 pre-function) 2:20 – 2:40

Session 13: Transistor Design and Optimization (Zlotnik Family Ballroom 4)

Chairpersons

Phil Oldiges (IBM, USA)

Francis Benistant

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Session 14: Advanced Transport Modeling (Zlotnik Family Ballroom 5)

Chairpersons

Denis Rideau (STMicroelectronics, Inc., France)

William Vandenberghe (University of Texas at Dallas, USA)

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Conference Dinner (Zlotnik Family Ballroom 5)

6:30 – ... Plated Dinner

Wednesday, September 26

Light Breakfast (Zlotnik Family Ballroom 4 & 5 pre-function) 7:30 – 8:30

Session 15: Plenary (Zlotnik Family Ballroom 4)

Chairperson

Leonard F. Register (The University of Texas at Austin, USA)

- 15.1 8:30 – 9:20 **Plenary Talk: Novel Materials + Novel Integration = Novel Electronics**..... N/A
Aaron Thean (National University of Singapore, Singapore)

Break (Zlotnik Family Ballroom 4 & 5 pre-function) 9:20 – 9:40

Session 16: Advanced Technology Analysis (Zlotnik Family Ballroom 4)

Chairpersons

Jürgen Lorenz (Fraunhofer IISB, Germany)

Guangrui (Maggie) Xia (University of British Columbia, Vancouver, Canada)

- 16.1 9:40 – 10:10 **Invited Talk: Experiments and Modeling of Mass Transport Phenomena in SiGe Devices** N/A
Guangrui (Maggie) Xia (University of British Columbia, Vancouver, Canada)
- 16.2 10:10 – 10:30 **Topography Simulation of 4H-SiC-Chemical-Vapor-Deposition Trench Filling Including an Orientation-Dependent Surface Free Energy** 331
Kazuhiro Mochizuki, S. Ji, R. Kosugi, Y. Yonezawa, and H. Okumura (National Institute of Advanced Industrial Science and Technology (AIST), Japan)
- 16.3 10:30 – 10:50 **Steady-State Empirical Model for Electrical Activation of Silicon-Implanted Gallium Nitride** 336
Alexander Toifl¹, V. Simonka¹, A. Hossinger², S. Selberherr¹, and J. Weinbub¹
(¹Technical University of Vienna, Austria, ²Silvaco Europe, Cambridge, UK)
- 16.4 10:50 – 11:10 **Technique for Asymmetric Source/Drain Resistance Extraction on a Single Gate Length MOSFET** 340
Phil Oldiges¹, C. Zhang², X. Miao², M. Kang³, and T. Yamashita² (¹IBM Research, Yorktown Heights, NY, USA, ²IBM Research, Albany, NY, USA, ³Samsung, Albany, NY, USA)
- 16.5 11:10 – 11:30 **N7 FinFET Self-Aligned Quadruple Patterning Modeling** 344
Sylvan Baudot¹, S. Guissi², A.P. Milenin¹, J. Ervin², and T. Schram¹ (¹IMEC, Leuven, Belgium, ²Coventor, Villebon sur Yvette, France)
- 16.6 11:30 – 11:50 **Dynamical Space Partitioning for Acceleration of Parallelized Lattice Kinetic Monte Carlo Simulations** 348
Takeshi Nishimatsu¹, A. Payet², B. Lee³, Y. Kayama¹, K. Ishikawa¹, A. Schmidt², I. Jang², and D.S. Kim² (¹Samsung, Yokohama, Japan, ²Samsung, Hwaseong-si, Korea, ³Samsung, San Jose, CA, USA)

Session 17: Interaction of Transistors and Circuits (Zlotnik Family Ballroom 5)

Chairpersons

Philippe Matagne (IMEC, Belgium)

Azad Naeemi (Georgia Tech. University, Atlanta, USA)

17.1	9:40 – 10:10	Invited Talk: Performance Modeling and Circuit Design for Beyond-CMOS Devices N/A Azad Naeemi (Georgia Tech. University, Atlanta, USA)
17.2	10:10 – 10:30	A Compact Model of Drift and Diffusion Memristor Applied in Neuron Circuits Design 352 Ying Zhao, C. Fang, N.D. Lu, M. Liu, Q. Li, F. Zhang, and L. Li (Chinese Academy of Sciences, China)
17.3	10:30 – 10:50	New Physical Insight for Analog Application in PSP Bulk Compact Model 356 Sebastiene Martinie ¹ , O. Rozeau ¹ , T. Poiroux ¹ , J.C. Barbe ¹ , F. Gilibert ² , X. Montagner ² , S. El Ghoul ² , A. Juge ² , G.D.J. Smit ³ , and A. Scholten ³ (¹ CEA-LETI, Grenoble, France, ² STMicroelectronics, Crolles, France, ³ NXP Semiconductor, Netherlands)
17.4	10:50 – 11:10	Methodology to Generate Approximate Circuits to Reduce Process Induced Degradation in CNFET Based Circuits 360 Kaship Sheikhand L. Wei (University of Waterloo, ON, Canada)
17.5	11:10 – 11:30	Compact Modelling of Single Event Transient in Bulk MOSFET for SPICE: Application to Elementary Circuits 364 Neil Rostand ^{1,2} , S. Martinie ² , J. Lacord ² , O. Rozeau ² , O. Billoint ² , J.C. Barbe ² , T. Poiroux ² , and G. Hubert ¹ (¹ French Aerospace Lab (ONERA), Toulouse, France, ² CEA-LETI, Grenoble, France)
17.6	11:30 – 11:50	Well-Posed Verilog-A Compact Model for Phase Change Memory 369 S.R. Kulkarni ¹ , D.V. Kadetotad ² , J.S. Seo ² , and B. Rajendran ¹ (¹ New Jersey Institute of Technology, Newark, NJ, USA, ² Arizona State University, Tempe, AZ, USA)

Lunch (Tejas Dining Room) 11:50 – 1:00

Conference Ends