

2018 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S 2018)

**Burlingame, California, USA
15-18 October 2018**



**IEEE Catalog Number: CFP18SOI-POD
ISBN: 978-1-5386-7628-8**

**Copyright © 2018 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP18SOI-POD
ISBN (Print-On-Demand):	978-1-5386-7628-8
ISBN (Online):	978-1-5386-7627-1
ISSN:	2573-5926

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

Technical Program

MONDAY OCTOBER 15, 2018

SESSION 1: PLENARY I

Session Chairs : *Bruce Doris; IBM / Mostafa Emam; Incize*

- 1.1 Enabling Market Innovation through Differentiated FDSOI Technology** N/A
John Pellerin; Vice President, Technology & Yield Engineering, GlobalFoundries, USA (Plenary Speaker)
 - 1.2 Powering the Human Intranet** N/A
Jan Rabaey; Co-Director of Berkeley Wireless Research Center and Director of the FCRP Multiscale Systems Research Center, University of California, Berkeley, USA (Plenary Speaker)
 - 1.3 Left, Right or Up. Living in a 3D World** N/A
Joe Macri; Corporate Vice President and Product CTO, AMD, USA (Plenary Speaker)
-

SESSION 2: PLENARY II

Session Chairs : *Philippe Flattresse; Soitec / Paul Franzon; North Carolina State University*

- 2.1 The Memory Futures** N/A
Gurtej Sandhu; Senior Fellow and Vice President Micron Technology, USA (Plenary Speaker)
- 2.2 Components for High-Fidelity Solid State Quantum Computers** N/A
David DiVincenzo; Director of the Institute for Quantum Information , RWTH Aachen University, Germany (Plenary Speaker)
- 2.3 Material and Device Innovation for IoT, Automotive and Mobile Connectivity Applications** N/A
Thomas Piliszcuk; Executive Vice President, Marketing, Business Development and Global Sales, SOITEC, France (Plenary Speaker)

Technical Program

SESSION 3: 2.5 AND 3D TECHNOLOGY

Session Chairs : *Jin-Woo Han; NASA / Severine Cheramy; CEA-Leti*

- 3.1 2.5 Packaging Technologies for Space Applications N/A**
Douglas Sheldon; Jet Propulsion Lab, NASA, USA (Invited Speaker)
- 3.2 Multi-ANN Embedded System Based on a Custom D-DRAM 1**
Paul Franzon; North Carolina State University, USA (Invited Speaker)
L.B. Baker, P. Franzon; Fellow, IEEE
- 3.3 Finite Element Method (FEM) Simulation Based Analysis for Optimal Chip Layout of a 2.5D Flip Chip Package 3**
M. Nayini, D. Questad, M. Farooq; GLOBALFOUNDRIES, Hopewell Junction, New York, USA
- 3.4 High-Speed TSV Integration in an Active Silicon Photonics Interposer Platform 6**
L. Bogaerts, Z. El-Mekki, S. Van Huylenbroeck, P. Nolmans, N. Pantano, X. Sun, M. Rakowski, D. Velenis, P. Verheyen, S. Balakrishnan, P. De Heyn, B. Snyder, Y. Ban, S. Srinivasan, S. Lardenois, J. De Coster, M. Detalle, P. Absil, A. Miller, M. Pantouvaki, J. Van Campenhout; imec, Leuven, Belgium
-

SESSION 4: NCFET FOCUS SESSION I

Session Chairs : *Nuo Xu; Samsung / Genquan Han; Xidian University*

- 4.1 Negative Capacitance and Its Implication for Next Generation Transistors N/A**
Sayeeef Salahuddin; University of California, Berkeley, USA (Invited Speaker)
- 4.2 Negative Capacitance: next technology booster for digital computation and sensing near 100milliVolts? N/A**
Adrian Ionescu; École Polytechnique Fédérale Lausanne, Switzerland (Invited Speaker)
- 4.3 Technology Breakthrough by Ferroelectric HfO₂ for Ultralow Power Logic and Memory Applications N/A**
Masaharu Kobayashi; University of Tokyo, Japan (Invited Speaker)
-

SESSION 5: 3D TECHNOLOGY II

Session Chairs : *Andrew Carter; Teledyne Scientific and Imaging / Masahide Goto; NHK Science and Technology Research Laboratories*

- 5.1 3D Nanostructures by Stacking Patterned Membranes 9**
Henry Smith; Massachusetts Institute of Technology, USA (Invited Speaker)
H. I. Smith¹, J. J. Fucetola¹, C. P. Fucetola², K. A. Mirica³; ¹MIT, Cambridge, MA, USA; ²Sublimit Labs, Inc. Cambridge, MA, USA; ³Dartmouth College, Hanover, NH, USA

Technical Program

- 5.2 Heat Shunting by Innovative Source/Drain Contact to Enable Monolithic 3D Integration of InGaAs MOSFETs 11**
SH. Kim¹, S.K. Kim¹, SH Shin², J-H. Han¹, D-M. Geum¹, J-P. Shim¹, S. Lee¹, H.S. Kim¹, G. Ju¹, J.D. Song¹, M.A. Alam², H-j. Kim¹; ¹Korea Institute of Science and Technology (KIST), Korea, ²Department of ECE, Purdue University, West Lafayette, IN, USA
- 5.3 Key Challenges and Opportunities for 3D Sequential Integration 13**
Anne Vandooren; imec, Belgium (Invited Speaker)
A. Vandooren, L. Witters, J. Franco, A. Mallik, B. Parvais, Z. Wu, W. Li, E. Rosseel, A. Hikkavy, L. Peng, , N. Rassoul, G. Jamieson, F. Inoue, G. Verbinnen, K. Devriendt, L. Teugels, N. Heylen, E. Vecchio, T. Zheng, N. Waldron, J. Boemmels, De Heyn, D. Mocuta, J. Ryckaert, N. Collaert; imec, Leuven, Belgium
- 5.4 Impact of Low-Temperature Coolcube™ Process on the Performance of FDSOI Tunnel FETs 17**
C. Diaz-Llorente¹, J.-P. Colinge¹, C. Le Royer¹, M. Vinet¹, C.G. Theodorou², S. Cristoloveanu², G. Ghibaudo²; ¹Université Grenoble Alpes, CEA-Leti, Grenoble, France, ²IMEP-LaHC, Minatec, INP, Université Grenoble Alpes, Grenoble, France
- 5.5 Advanced 3D Nanophotonic-Nanoelectronic-Integrated-Circuits for Future Energy-Efficient and High-Throughput Computing Systems N/A**
SJ Ben Yoo; University of California, Davis, USA (Invited Speaker)
-

SESSION 6: LOW POWER CIRCUITS I

Session Chairs : *Philippe Flatresse; Soitec / Carlos Reita; CEA-Leti*

- 6.1 Quentin: an Ultra-Low-Power PULPissimo SoC in 22nm FDX 20**
Davide Rossi; Università di Bologna, Italy (Invited Speaker)
P.D. Schiavone¹, D. Rossi², A. Pullini¹, A. Di Mauro¹, F. Conti^{1,2}, L. Benini^{2,1}; ¹ETH Zürich, Switzerland, ²University of Bologna, Italy
- 6.2 ABB and DVFS for the SpiNNaker2 Neuromorphic MPSoC in 22FDX Technology N/A**
Sebastien Hoeppe; RACYICS/Technische Universität Dresden, Germany (Invited Speaker)
- 6.3 A 14.3pW Sub-Threshold 2T Gain-Cell eDRAM for Ultra-Low Power IoT Applications in 28nm FD-SOI 23**
R. Giterman, A. Teman and A. Fish; Faculty of Engineering, Bar-Ilan University, Ramat Gan, Israel
- 6.4 Exploration of Fine-Grain Body Bias Control in Many-Core Processor Arrays 25**
Bevan Baas; University of California, Davis, USA (Invited Speaker)
B. Bass, B. Bohnenstiehl and J. Cui; Department of Electrical and Computer Engineering, University of California, Davis, Davis, California, USA

Technical Program

TUESDAY OCTOBER 16, 2018

SESSION 7: RFSOI I

Session Chairs : *Mostafa Emam; CEA-Leti / John-Ellis Monaghan; GLOBALFOUNDRIES*

- 7.1 Fully Depleted SOI Technologies from Digital to RF and Beyond** 28
Jean-Pierre Raskin; Université catholique de Louvain, Belgium (Invited Speaker)
J.-P. Raskin; *Institute of Information and Communication Technologies, Electronics and Applied Mathematics (ICTEAM), Novain-la-Neuve, Belgium*
- 7.2 Device Layout Dimension Impact on Substrate Effective Resistivity** 31
M. Rack¹, L. Nyssens¹, J.-P. Raskin¹, D. Lederer², A. Paganini², M.B. Shinde², A. Beganovic²; ¹ *Université catholique de Louvain*, ² *GLOBALFOUNDRIES, USA*
- 7.3 New Specialty Silicon Technology for 5G and IOT Applications** N/A
Paul Hurwitz; TowerJazz, USA (Invited Speaker)
- 7.4 Process Dependency of RF performance in High Resistivity Trap-Rich SOI Substrate** ~~Withdrawn~~ N/A
D.F. Lim¹, K. Zheng¹, K. Bandy², L. Kang², J. Nxumalo², N. Lai², G. Chrisman², G. Pfeiffer², S. Kouassi¹, G. Freeman², C. Venkataramani¹; ¹ *GLOBALFOUNDRIES Fab 7, Singapore*, ² *GLOBALFOUNDRIES Fab 10, Hopewell Junction, New York, USA*
-

SESSION 8: NCFET FOCUS SESSION II

Session Chairs : *Nuo Xu; Samsung / Jamie Therani; Columbia University*

- 8.1 Steep Slope Hysteresis-free Negative Capacitance MoS₂ Transistors** N/A
Peide "Peter" Ye; Purdue University, USA (Invited Speaker)
- 8.2 Experimental Investigation of Fundamentals of Negative Capacitance FETs** 33
Genquan Han; Xidian University, China (Invited Speaker)
G.Han, J. Zhou, Y. Liu, J. Li, Y. Peng and Y. Hao; *State Key Discipline Laboratory of Wide Band Gap Semiconductor Technology, School of Microelectronics, Xidian University, Xi'an Shaanxi, China*
- 8.3 Steep Switching Transistors based on Abrupt Electronic Phase Transition** N/A
Nikhil Shukla; University of Virginia, USA (Invited Speaker)
-

SESSION 9: LOW POWER CIRCUITS II

Session Chairs : *Davide Rossi; University of Bologna / Alex Fish; Bar Ilan University*

- 9.1 Future Computing- the Neuromorphic Approach** N/A
Carlos Reita; CEA-Leti, France (Invited Speaker)

Technical Program

- 9.2 Improving the Security of a 6T SRAM using Body-Biasing in 28 nm FD-SOI** 35
R. Gitterman, O. Keren and A. Fish; *Bar-Ilan University, Ramat Gan, Israel*
- 9.3 Independent Body-Biasing of P-N Transistors in an 28nm UTBB FD-SOI ULP Near-Threshold Multi-Core Cluster** 37
A. Di Mauro², D. Rossi¹, A. Pullini², P. Flatresse³, L. Benini^{1,3}; ¹DEI, University of Bologna, Bologna, Italy, ²Integrated Systems Laboratory, Zurich, Switzerland, ³SOITEC, Parc Technologique des Fontaines Chemin des Franques, Crolles, France
- 9.4 Process Variation-Aware Datapath Employing Dual Mode Logic** 40
N. Shavit, I. Stanger, R. Taco, A. Fish; *Bar-Ilan University, Ramat-Gan, Israel*
- 9.5 Design of a Rectifier-Free Near-Threshold UHF Gen2 RFID Tag using Dual-Phase RF-only Logic** 43
K. Bhanushali¹, W. Zhao², and P. D. Franzon¹; ¹Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina, USA, ²Broadcom Limited., Irvine, California, USA
-

SESSION 10: TUNNELING TRANSISTORS

Session Chairs : *Peter Ye; Purdue University / Alan Seabaugh; University of Notre Dame*

- 10.1 Optimization of Intrinsic Auger-Assisted Tunneling for TFETs with Steep Subthreshold Slopes** 46
Jamie Teherani; Columbia University, USA (Invited Speaker)
J. T. Teherani; *Department of Electrical Engineering, Columbia University, New York, New York, USA*
- 10.2 Trap-Aware Compact Modeling and Power-Performance Assessment of III-V Tunnel FET** 48
Y. Xiang^{1,2}, D. Yakimets², S. Sant³, E. Memisevic⁴, M.G. Bardon², A.S. Verhulst², B. Parvais^{2,5}, A. Schenk³, L.-E. Wernersson⁴ and G. Groeseneken^{1,2}; ¹Katholieke Universiteit Leuven, Leuven, Belgium, ²imec, Leuven, Belgium, ³ETH Zürich, Zürich, Switzerland, ⁴Lund University, Lund, Sweden; ⁵Vrije Universiteit Brussel, Brussels, Belgium
- 10.3 Piezoelectric Field Effect Transistors with Sub-Thermal Swing** 51
Xiangwei Jiang; Chinese Academy of Science, China (Invited Speaker)
H. Wang¹, Y. Long¹, X. Jiang¹, G. Han²; ¹State Key Laboratory of Superlattices and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences Beijing, China, ²State Key Discipline Laboratory of Wide Band Gap Semiconductor Technology, School of Microelectronics, Xidian University, Xi'an, Shaanxi, China

Technical Program

- 10.4 First Experimental Confirmation of Ultralow Voltage Rectification by Super Steep Subthreshold Slope "PN-Body Tied SOI-FET" for High Efficiency RF Energy Harvesting and Ultralow Voltage Sensing 54**
S. Momose¹, J. Ida¹, T. Yamada¹, T. Mori¹, K. Itoh¹, K. Ishibashi² and Y. Arai³;
¹Division of Electrical Engineering, Kanazawa Institute of Technology, Nonoichi, Ishikawa, Japan, ²The University of Electro-Communications, Tokyo Japan, ³High Energy Accelerator Research Org., KEK, Tsukuba Japan
- 10.5 A New Sharp Switch Device Integrated in 28nm FD-SOI Technology 57**
T. Bédécarrats^{1,2,3}, C. Fenouillet-Béranger², S. Cristoloveanu³, P. Galy¹;
¹STMicroelectronics, Crolles, France, ²CEA-LETI, Grenoble, France, ³Univ. Grenoble Alpes, Grenoble, France
-

SESSION 11: RFSOI II

Session Chairs : *Shawn Thomas; GlobalWafers / Paul Hurwitz; TowerJazz Semiconductor*

- 11.1 PD-SOI: Enabling Adaptive RF Front-End Modules 60**
Piet Wambacq; imec, Belgium (Invited Speaker)
B. van Liempd¹, J. Craninckx¹, P. Wambacq^{1,2}; ¹imec, Leuven, Belgium, ²ETRO Dept., Vrije Universiteit Brussel, Brussels, Belgium
- 11.2 Digital Frequency Multiplier for LO Generation using 22nm FDSOI 62**
A. Balasubramaniyan and A. Bellaouar; *GLOBALFOUNDRIES, Richardson, Texas, USA*
- 11.3 28 FDSOI RF Figures of Merits and Parasitic Elements at Cryogenic Temperature 64**
B. Kazemi Esfeh¹, V. Kilchytska¹, N. Planes², M. Haond², D. Flandre¹, J.-P. Raskin¹;
¹CTEAM, Université catholique de Louvain, Louvain-la-Neuve, Belgium, ²ST, ST-Microelectronics, Crolles, France
- 11.4 45nm PD SOI FET Gate Resistance Optimization for mmw Applications 67**
D. Lederer, S. Jain, S. Saroop, A. Kumar, G. Freeman; *GLOBALFOUNDRIES, Hopewell Junction, New York, USA*
-

SESSION 12: RELIABILITY

Session Chairs : *Toshiro Hiramoto; University of Tokyo / Mike Alles; Vanderbilt University*

- 12.1 Characterizing Soft Error Rates of 65-nm SOTB and Bulk SRAMs with Muon and Neutron Beams 70**
Masanori Hashimoto; Osaka University, Japan (Invited Speaker)
M. Hashimoto¹, W. Liao¹, S. Manabe², Y. Watanabe²; ¹Department of Information Systems Engineering, Osaka University, Japan, ²Department of Advanced Energy Engineering Science, Kyushu University, Japan
- 12.2 Advantages and Disadvantages of SOI in Terms of Radiation Tolerance 72**
Kazuyuki Hirose; Institute of Space and Astronautical Science, JAXA, Japan (Invited Speaker)
K. Hirose and D. Kobayashi; *Institute of Space and Astronautical Science, JAXA, Kanagawa, Japan*

Technical Program

- 12.3 Threshold Dependence of Soft-Errors Induced by α Particles and Heavy Ions Flip Flops in a 65 nm Thin BOX FDSOI** 76
M. Ebara, K. Yamada, K. Kojima, J. Furuta, and K. Kobayashi; *Kyoto Institute of Technology, Japan*
- 12.4 The Study of Plasma Induced Damage on Silicon on Thin BOX** 79
Y. Yamamoto, K. Segi, S. Tsuda, H. Makiyama, T. Hasegawa, K. Maekawa, H. Shinkawata and T. Yamashita; *Device Technology Division, Advanced Device Technology Department Renesas Electronics Corporation Hitachinaka-shi Ibaraki, Japan*
- 12.5 Radiation-Hardened Flip-Flops with Small Area and Delay Overheads Using Guard-Gates in FDSOI Processes** 81
K. Yamada, J. Furuta, K. Kobayashi; *Kyoto Institute of Technology, Kyoto, Japan*
-

SESSION 13: LOW POWER CIRCUITS III

Session Chairs : *Philippe Flatresse; Soitec / Rossella Ranica; ST Microelectronics*

- 13.1 Near Threshold Circuit Building Blocks** N/A
Dennis Sylvester; University of Michigan, Ann Arbor, USA (Invited Speaker)
- 13.2 An 8-T ULV SRAM Macro in 28nm FDSOI with 7.4 pW/bit Retention Power and Back-Biased-Scalable Speed/Energy Trade-Off** 84
T. Haine, D. Flandre, D. Bol; *ICTEAM Institute, Electronic Circuits and Systems (ECS) Université catholique de Louvain, Louvain-la-Neuve, Belgium*
- 13.3 An Image Sensor SOC with Energy Harvesting Mixed-Vth Pixel Generating 5.8 μ W/mm² Power Density and 0.77 Frames/second Self-Powered Frame Rate** 87
M.F. Amir¹, J.H. Ko¹, and S. Mukhopadhyay¹; ¹*School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA*
- 13.4 FDSOI Circuit Design for High Energy Efficiency: Wide Operating Range and ULP Applications – A 7-Year Experience** N/A
Edith Beigne; CEA-Leti, France (Invited Speaker)
- 13.5 Virtually Nonvolatile Retention SRAM cell Using Dual-Mode Inverters** 90
D. Kitagata, H. Yoshida, S. Yamamoto and S. Sugahara; *Laboratory for Future Interdisciplinary Research of Science and Technology, Tokyo Inst. of Tech., Yokohama, Japan*
-

SESSION 14: NOVEL DEVICES

Session Chairs : *João Antonio Martino; University of São Paulo / Jing Wan; Fudan University*

- 14.1 A 0.0487mm² 4Kx8 Metal-Gate Innovative Fuse Memory at 22nm FD-SOI with 1.2V+/-16% Program Voltage, 0.42V Vddmin, and Full Testability** 93
S. Chung¹, J. Lin¹, W-K. Fang¹, W-H. Yu¹, M. Wendt², H. Prengel², A. Xu³, and H.K. Lee³; ¹*Attopsemi Technology, Hsinchu, Taiwan*, ²*GlobalFoundries, Dresden, Germany*, ³*GlobalFoundries, Singapore*

Technical Program

- 14.2 1T DRAM with Vertically Stacked *n*-Oxide-*p* Architecture 95**
Md. H.R. Ansari¹, N. Navlakha¹, J-T. Lin², and A. Kranti¹; ¹Low Power Nanoelectronics Research Group, Discipline of Electrical Engineering, Indian Institute of Technology Indore, Simrol, Indore, India, ²Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan R.O.C.
- 14.3 Characterization of P-Channel FOI-MAHAS Charge Trapping Memory with Improved Operation Characteristics 98**
Z. Hou, H. Yin, Z. Wu; Key Laboratory of Microelectronic Devices and Integrated Technologies, Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China, and also with the University of Chinese Academy of Sciences, Beijing, China
- 14.4 Scattering Mechanisms in Inversion Layers of Ge MOSFETs: Impact of Surface States and Carrier Effective Masses 101**
Rui Zhang Zhejiang University, Hangzhou, China (Invited Speaker)
R. Zhang, X. Yu, and Y. Zhao; College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou, China
-

SESSION 15: POSTER SESSION

Session Chairs : *Michelly de Souza; Centro Universitário FEI / Gary Bronner; Rambus*

- 15.1 Performance & Stability Analysis of SRAM Cells Based on Different FinFET Devices in 7nm Technology 103**
M.U. Mohammed, A. Nizam and M.H Chowdhury; Computer Science Electrical Engineering, University of Missouri - Kansas City, Kansas City, Missouri, USA
- 15.2 Performance Assessment of TFET Architectures as 1T-DRAM 106**
N. Navlakha¹, Md. H. Raza Ansari¹, J-T. Lin², and A. Kranti¹; ¹Low Power Nanoelectronics Research Group, Discipline of Electrical Engineering, Indian Institute of Technology Indore, Simrol, Indore, India, ²Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan R.O.C.
- 15.3 Impact of Process and Device Dimensions on Bio-TFET Sensitivity 109**
C. N. Macambira¹, P. G. D. Agopian^{1,2}, J. A. Martino¹; ¹LSI/PSI/USP, University of São Paulo, Brazil, ²UNESP, São Paulo State University, São João da Boa Vista, Brazil
- 15.4 A Low Leakage Current Tunneling-FET Based on SOI 112**
J. Bu^{1,2}, D. Li^{1,2}, G. Xu¹, X. Cai^{1,2}, Y. Kuang^{1,2}, Z. Han^{1,2,3}, J. Luo^{1,2}; ¹Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China, ²Key Laboratory of Silicon Device Technology, Chinese Academy of Sciences, Beijing, China, ³University of Chinese Academy of Sciences, Beijing, China
- 15.5 A First Principle Study of the Carrier Mobility and Injection Velocity for Strained 2D Materials MOSFETs 115**
K. Luo, Y. Pan, Z. Hou, J. Yao, W. Yang, Z. Wu, H. Yin, and W. Wang; Key Laboratory of Microelectronics Devices and Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China
- 15.6 Mechanism for High Hall-Effect Mobility in Sputtered-MoS₂ Film Controlling Particle Energy 118**
T. Sakamoto¹, T. Ohashi¹, K. Matsuura¹, I. Muneta¹, K. Kakushima¹, K. Tsutsui¹, Y. Suzuki², N. Ikarashi² and H. Wakabayashi¹; ¹Tokyo Institute of Technology, Midori-ku, Yokohama, Kanagawa, Japan, ²Nagoya University, Furo-cho Chikusa-ku, Nagoya, Aichi, Japan

Technical Program

- 15.7 Hall-Effect Mobility Enhancement of Sputtered MoS₂ Film by Vapor Phase Sulfurization through Al₂O₃ Passivation Film 120**
M. Hamada, K. Matsuura, T. Sakamoto, H. Tanigawa, T. Ohashi, I. Muneta, T. Hoshii, K. Kakushima, K. Tsutsui, and H. Wakabayashi; *Tokyo Institute of Technology, Japan*
- 15.8 Modeling the Interface Trap Density Influence on Junctionless Nanowire Transistors Behavior 122**
R. Trevisoli¹, R.T. Doria², M. de Souza², M.A. Pavanello²; ¹*Universidade Federal do ABC, Santo André, Brazil*, ²*Centro Universitário FEI, São Bernardo do Campo, Brazil*
- 15.9 Body Related Parasitic Parameters Extraction for PD-SOI MOSFETs Using Four-Port Network 125**
K. Lu, Y. Chang, W. Yang, and Y. Dong; *State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai, China*
- 15.10 Rapid Fabricating sub-50 nm FD-SOI by Secondary Ion-Cut Processing 127**
B. T. -H. Lee*, Y. -L. Chang, C.-H. Huang, C. -C. Ho, and F.-S. Lo; *Dept. of Mechanical Engineering, National Centration University, Taoyuan City, Taiwan, ROC*
- 15.11 Insights to the Scaling Impact on Back-Gate Biasing for FD SOI MOSFETs 129**
M.-Y. Chang, L.-J. Wang, and M.-H. Chiang; *Department of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan*
- 15.12 Total Dose Effects of 28nm FD-SOI CMOS Transistors 131**
Y. Kuang^{1, 2}, J. Bu^{1, 2}, B. Li^{1, 2}, L. Gao^{1, 2}, C. Liang^{1, 2}, Z. Han^{1, 2, 3}, J. Luo^{1, 2}; ¹*Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China*, ²*Key Laboratory of Silicon Device Technology, Chinese Academy of Sciences, Beijing, China*, ³*University of Chinese Academy of Sciences, Beijing, China*
- 15.13 Channel Length Sizing for Power Minimization in Leakage-Dominated Digital Circuits 134**
D.S. Truesdell and B.H. Calhoun; *Department of Electrical and Computer Engineering, University of Virginia, Charlottesville, Virginia, USA*
- 15.14 Design and Characterization of Bulk Driven MOS Varactor Based VCO at Near Threshold Regime 136**
L.M. Dani¹, N. Mishra¹, S.K. Banchhor¹, S. Miryala², A. Doneria¹, B. Anand¹; ¹*Indian Institute of Technology Roorkee, Roorkee, India*, ²*FERMILAB, Batavia, Illinois, USA*
- 15.15 A Study on Monolithic 3-D RF/AMS ICs: Placing Digital Blocks Under Inductors 138**
P. Chaourani, D. Stathis, S. Rodriguez, P.-E. Hellström, and A. Rusu; *KTH, Royal Institute of Technology, Department of Electronics, Stockholm, Sweden*
- 15.16 TSV Induced Stress Model and Its Application in Delay Estimation 141**
R. Chawla¹, S. Yadav¹, A. Sharma¹, B. Kaur², R. Pratap², and B. Anand²; ¹*Indian Institute of Technology Roorkee, Roorkee, India*, ²*National Institute of Technology Delhi, Delhi, India*

Technical Program

WEDNESDAY OCTOBER 17, 2018

SESSION 16: RFSOI III

Session Chairs : *Jean-Pierre Raskin; Université catholique de Louvain /
Siva Adusumilli; GLOBALFOUNDRIES*

- 16.1 High Performance LNA Devices for Integrated Switch Technology 144**
John Ellis-Monaghan; GLOBALFOUNDRIES, USA (Invited Speaker)
J. Ellis-Monaghan², R. Wolf², A. Stamper², M. Jaffee², M. Abou-Khalil²,
A. Vallett², S. Adusumilli², S. Shank², R. Phelps², A. Joseph², A. Sundaram¹, V.
Vanukuru¹, B. Swaminathan¹; ¹RF Technology Development, RF Model
Development, ²GLOBALFOUNDRIES
- 16.2 A 23 GHz Low-Phase-Noise Transformer-Feedback VCO in 22nm FD-SOI with a
FOM_T of 191 dBc/Hz 146**
Z. Zong^{1,2}, C-H. Tsai^{1,2}, F. Pepe³, G. Mangraviti², Y. Liu², Q. Shi², B. Parvais^{1,2}, P.
Wambacq^{1,2}; ¹Vrije Universiteit Brussel, Dept. of Electronics and Informatics,
Brussels, Belgium, ²imec, Heverlee, Belgium, ³Università di Pavia, Pavia PV, Italy
- 16.3 A 22nm FDSOI Technology with integrated 3.3V/5V/6.5V RFLDMOS Devices for
IOT SOC applications 148**
C. Schippel¹, S. Lehmann¹, S.N. Ong², A. Muehlhoff¹, I. Cortés¹, W.H. Chow², D.
Utess¹, A. Zaka¹, A. Divay⁴, A. Pakfar¹, J. Faul¹, J. Mazurier¹, K.W. Chew², L.H.K. Chan²,
R. Taylor³, B. Rice¹, D. Haramé¹; ¹GLOBALFOUNDRIES, Germany,
²GLOBALFOUNDRIES, Singapore, ³GLOBALFOUNDRIES, USA, ⁴CEA-LETI Minatéc,
France
- 16.4 RF/mmWave Front-End Module Switch in 22nm FDSOI Process 150**
A. Balasubramaniyan¹, A. Bellaouar²; ¹GLOBALFOUNDRIES, Richardson, Texas,
USA, ²GLOBALFOUNDRIES IP Development, Richardson, Texas, USA
- 16.5 A 28-GHz Transceiver Front-End with T/R Switching Achieving 11.2-dBm OP_{1dB},
33.8% PAE_{max} and 4-dB NF in 22-nm FD-SOI for 5G Communication 152**
Y. Liu¹, G. Mangraviti¹, S. Hitomi², K. Khalaf¹, B. Debaillie¹, P. Wambacq^{1,3};
¹imec, Leuven, Belgium, ²Murata Manufacturing Co., Ltd., Kyoto, Japan, ³Dept. of
Electronics and Informatics (ETRO), Vrije Universiteit Brussel (VUB), Brussels,
Belgium

Technical Program

SESSION 17: NOVEL DEVICES AND NEUROMORPHIC COMPUTING

Session Chairs : *Nikhil Shukla; University of Virginia /*
Hitoshi Wakabayashi; Tokyo institute of Technology

17.1 Realizing the Ultra-Low Power Consumption Nanoscale Devices by Controlled and Reversible Crack 155

Long You; *Huazhong University of Science and Technology, China (Invited Speaker)*

L. You^{1,2}, Q. Luo¹, Z. Guo¹, S. Zhang¹, X. Jiang³, N. Xu⁴, HJ. Wang^{3,5}, M. Song⁶, G. Han⁵, J. Hong¹; ¹*School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan, China,* ²*Wuhan National Lab for Optoelectronics, Huazhong University of Science and Technology, Wuhan, China,* ³*State Key Laboratory for Superlattices and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China,* ⁴*Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA USA,* ⁵*School of Microelectronics, Xidian University, Xi'an, China,* ⁶*Hubei Key Laboratory of Ferro & Piezoelectric Materials and Devices, Faculty of Physics and Electronic Science, Hubei University, Wuhan, China*

17.2 MTJ-Based Nonvolatile Ternary Logic Gate for Quantized Convolutional Neural Networks 158

M. Natsui, T. Chiba, and T. Hanyu; *Research Institute of Electrical Communication, Tohoku University, Aoba-ku, Sendai, Japan*

17.3 Resistive Switching Behaviors and Novel Device Applications of Metal-Oxide-Si/Ge Structures 160

Bing Chen; *Zhejiang University, China (Invited Speaker)*

B. Chen¹, Y. Zhang¹, W. Na¹, P. Huang² and Y. Zhao¹; ¹*College of Information Science & Electronic Engineering, Zhejiang University, Hangzhou, China,* ²*Institute of Microelectronics, Peking University, Beijing, China*

17.4 A RRAM-based Coarse Grain Reconfigurable Array for Neural Network Accelerators 162

Z. Chen, H. Zhou and J. Gu; *Department of Electrical Engineering and Computer Science, Northwestern University, Evanston, IL, USA*

17.5 3D Stacked High Throughput Pixel Parallel Image Sensor with Integrated ReRAM Based Neural Accelerator 164

M.F. Amir¹ and S. Mukhopadhyay¹; ¹*School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, Georgia, USA*

SESSION 18: SOI DEVICES I

Session Chairs : *Michelly de Souza; Centro Universitário FEI /*
Mike Alles; Vanderbilt University

18.1 How FDSOI Will Enable VLSI Terahertz Systems N/A

Hani Sherry; *TiHive, France (Invited Speaker)*

18.2 Optimization of the Silicon Thickness on Back Enhanced (BE) SOI_p MOSFET Working as a Visible Spectrum Light Sensor 167

J. A. Padovese¹, L. S. Yojo¹, R. C. Rangel^{1,2}, K. R. A. Sasaki¹, J. A. Martino¹; ¹*LSI/PSI/USP, University of São Paulo, São Paulo, Brazil,* ²*FATEC-SP, Faculdade de Tecnologia de São Paulo, São Paulo, Brazil*

Technical Program

- 18.3 A Highly Sensitive Photodetector Based on Deep Depletion Effects in SOI Transistors 170**
M. Arsalan¹, XY. Cao¹, BR. Lu¹, YF. Chen¹, A. Zaslavsky², S. Cristoloveanu³, M. Bawedin³ and J. Wan¹; ¹State key lab of ASIC and System, School of Information Science and Engineering, Fudan University, Shanghai, China, ²Department of Physics and School of Engineering, Brown University, Providence, Rhode Island, USA, ³IMEP-LAHC, INP-Grenoble/Minatec, Grenoble, France
- 18.4 Optimization of the Permittivity-Based BE SOI Biosensor 173**
L. S. Yojo¹, R. C. Rangel^{1,2}, K. R. A. Sasaki¹, J. A. Martino¹; ¹LSI/PSI/USP, University of São Paulo, São Paulo, Brazil, ²FATEC-SP, Faculdade de Tecnologia de São Paulo, São Paulo, Brazil
- 18.5 A New Photodetector on SOI 176**
J. Liu¹, XY. Cao¹, BR. Lu¹, YF. Chen¹, A. Zaslavsky², S. Cristoloveanu³, M. Bawedin³ and J. Wan¹; ¹State key lab of ASIC and System, School of Information Science and Engineering, Fudan University, Shanghai, China, ²Department of Physics and School of Engineering, Brown University, Providence, Rhode Island, USA, ³IMEP-LAHC, INP-Grenoble/Minatec, Grenoble, France
-

SESSION 19: MONOLITHIC 3D

Session Chairs : *Kai-Shin Li; National Nano Device Laboratories / Anne Vandooren; imec*

- 19.1 Vertically-Stacked Nanowire/FinFETs and Following 2D FETs for Logic Chips 178**
Hitoshi Wakabayashi; Tokyo Institute of Technology, Japan (Invited Speaker)
H. Wakabayashi; Tokyo Institute of Technology, Yokohama, Japan
- 19.2 Monolithic-3D Integration with 2D Materials: Toward Ultimate Vertically-Scaled 3D-ICs 181**
J. Jiang, K. Parto, W. Cao and K. Banerjee; Department of Electrical and Computer Engineering, University of California, Santa Barbara, California, USA
- 19.3 Strategies for 3D Integration of Graphene Devices onto CMOS N/A**
Davood Shahrjerdi; New York University, USA (Invited Speaker)
- 19.4 Beyond Advanced FDSOI: Low Temp SmartCut for Enabling High Density 3D SoC Applications 184**
Walter Schwarzenbach; SOITEC, France (Invited Speaker)
W. Schwarzenbach, B.-Y. Nguyen, L. Ecarnot, S. Loubriat, M. Detard, E. Cela, C. Bertrand-Giuliani, G. Chabanne, C. Maddalon, N. Daval, C. Girard and C. Maleville; Soitec, Parc Technologique des Fontaines, Bernin, France
-

SESSION 20: SOI DEVICES II

Session Chairs : *Paul Grudowski; NXP Semiconductors / Mario Pelella; ON Semiconductor*

- 20.1 Will Self-Heating be Seriously Problematic in Sub-10nm Technology Nodes? 186**
Yi Zhao; College of Information Science & Electronic Engineering, Zhejiang University, Hangzhou, China (Invited Speaker)
Y. Zhao, Y. Qu and B. Chen; College of Information Science & Electronic Engineering, Zhejiang University, Hangzhou, China

Technical Program

- 20.2 Back Bias Influence on Low-Frequency Noise of n-type Nanowires SOI MOSFETs 188**
A.R. Molto, B.C. Paz, R.T. Doria, M. de Souza and M.A. Pavanello; *Centro Universitário FEI, São Bernardo do Campo, Brazil*
- 20.3 A Self-Contained Defect-Aware Module for Realistic Simulations of LFN, RTN and Time-Dependent Variability in FD-SOI Devices and Circuits 191**
C.G. Theodorou, G. Ghibaudo; *IMEP-LAHC, Grenoble INP, MINATEC, France*
- 20.4 Is FD-SOI Immune to Floating Body Effects? 194**
H. Park¹, K. Lee¹, J.-P. Colinge², S. Cristoloveanu¹; ¹IMEP-LaHC, Minatec, Grenoble INP, University Grenoble Alpes, CNRS, Grenoble, France, ²University Grenoble Alpes, CEA-LETI, Grenoble, France
- 20.5 New Approach for Removing the Self-Heating from MOSFET Current Using Only DC Characteristics 197**
C. A. B. Mori¹, P. G. D. Agopian^{1,2}, J. A. Martino¹; ¹LSI/PSI/USP, University of São Paulo, São Paulo, Brazil, ²São Paulo State University (UNESP), São João da Boa Vista, Brazil
-

SESSION 21: 3D TECHNOLOGY II

Session Chairs : *Paul Franzone; North Carolina State University / Jean-Eric Michallet; CEA-Leti*

- 21.1 Pixel-Parallel 3D Integrated CMOS Image Sensors Developed by Direct Bonding of SOI Layers for Next-Generation Video Systems 200**
Masahide Goto; *NHK Science and Technology Research Laboratories, Japan (Invited Speaker)*
M. Goto¹, Y. Honda¹, T. Watabe¹, K. Hagiwara¹, M. Nanba¹, Y. Iguchi¹, T. Saraya², M. Kobayashi², E. Higurashi², H. Toshiyoshi² and T. Hiramoto²; ¹NHK Science and Technology Research Laboratories, Japan, ²The University of Tokyo, Japan
- 21.2 Low-Temperature Wafer Bonding for Three-Dimensional Wafer-Scale Integration 203**
Z. Wan¹, K. Winstel², A. Kumar³ and S. S. Iyer¹; ¹Center for Heterogeneous Integration and Performance Scaling (CHIPS), UCLA, Los Angeles, California, USA, ²IBM Research Albany Nanotech, Albany, New York, USA, ³IBM Research, Yorktown Heights, New York, USA
- 21.3 Si/InP Heterogeneous Integration Techniques from the Wafer-Scale (Hybrid Wafer Bonding) to the Discrete Transistor (Micro-Transfer Printing) 205**
Andrew Carter; *Teledyne Scientific and Imaging, USA (Invited Speaker)*
A.D. Carter¹, M.E. Urteaga¹, Z.M. Griffith¹, K.-J. Lee¹, J. Roderick¹, P. Rowell¹, J. Bergman¹, S. Hong², R. Patti², C. Petteway², G. Fountain², K. Ghosel³, C. Bower³; ¹Teledyne Scientific and Imaging, Thousand Oaks, California, USA, ²NHanced Semiconductors Inc. Naperville, Illinois, USA, ³X-Celeprint US, Research Triangle Park, North Carolina, USA

Technical Program

SESSION 22: NCFETS

Session Chairs : *Nuo Xu; Samsung / Adrian Ionescu; École Polytechnique Fédérale Lausanne*

- 22.1 Device Structural Effects on Negative-Capacitance FETs 209**
Pin Su; National Chiao Tung University, Taiwan (Invited Speaker)
P. Su and W-X. You; *Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Taiwan*
- 22.2 Investigation of Ferroelectric HfZrO FET for Steep Slope Applications 211**
Md N.K. Alam^{1,3}, B. Kaczer¹, L-Å. Ragnarsson¹, M.I. Popovici¹, N. Horiguchi¹, M. Heyns^{1,3}, and J. Van Houdt^{1,2}; ¹IMEC, Leuven, Belgium; ²ESAT, K. U. Leuven; ³Department of Materials Engineering, K. U. Leuven
- 22.3 Evaluation of NC-FinFET Based Subsystem-Level Logic Circuits Using SPICE Simulation 214**
W-X. You¹, P. Su¹ and C. Hu^{2,3}; ¹Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Taiwan, ²International College of Semiconductor Technology, National Chiao Tung University, ³Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, USA
- 22.4 Scaling NC-FinFET to Sub-3 nm Nodes 216**
Ashish Pal, Sushant Mittal, Bahniman Ghosh, Chieh Yu Lin, Blessy Alexander, Buvna Ayyagari, Angada B. Sachid; *Design Technology, Applied Materials, Santa Clara, CA, USA*
- 22.5 Analog/RF Performance of Thin (~10 nm) HfO₂ Ferroelectric FDSOI NCFET at 20 nm Gate Length 218**
S. Mehrotra and S. Qureshi; *Department of Electrical Engineering, Indian Institute of Technology Kanpur, India*
-

SESSION 23: 3D TECHNOLOGY III

Session Chairs : *Davood Shahrjerdi; New York University / Jin-Woo Han; NASA*

- 23.1 FinFET-based Monolithic 3D+ with RRAM Array and Computing in Memory SRAM for Intelligent IoT Chip Application 221**
Kai-Shin Li; National Chiao Tung University, Taiwan (Invited Speaker)
K-S. Li¹, F-K. Hsueh¹, C-H. Shen¹, J-M. Shieh¹, H-C. Chen¹, W-H. Huang¹, H-Y. Chiu², C-C. Yang¹, T-Y. Hsieh¹, B-Y. Chen¹, W-H. Chen², K-H. Hsu², M-F. Chang², and W-K. Yeh¹; ¹National Nano Device Laboratories, Hsinchu, Taiwan; ²Department of Electrical Engineering, National Tsing Hua University, Taiwan
- 23.2 3DVLSI, Technology and Application 224**
Séverine Chéramy; CEA-Leti, France (Invited Speaker)
S. Chéramy, A. Jouve, C. Fenouillet-Beranger, P. Batude, M. Vinet; *Univ. Grenoble Alpes, CEA, LETI*
- 23.3 On the Design of Energy-Efficient I/O Circuits for Interposer-based 2.5D System-in-Package 229**
M. Lee, J. Kim, A. Singh, H.M. Torun, M. Swaminathan, S. Lim, and S. Mukhopadhyay; *School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, CA, USA*