

2018 31st IEEE International System-on-Chip Conference (SOCC 2018)

**Arlington, Virginia, USA
4 – 7 September 2018**



**IEEE Catalog Number: CFP18ASI-POD
ISBN: 978-1-5386-1492-1**

**Copyright © 2018 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP18ASI-POD
ISBN (Print-On-Demand):	978-1-5386-1492-1
ISBN (Online):	978-1-5386-1491-4
ISSN:	2164-1676

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

Abugharbieh, Khaldoon	W1A.4	19	A Discontinuous Charging Technique with Programmable Duty-Cycle for Switched-Capacitor Based Energy Harvesting Circuits in IoT Applications
Adnan, Md Musabbir	W2A.1	37	A Twin Memristor Synapse for Spike Timing Dependent Learning in Neuromorphic Systems
Ahmed, Meraj	F2A.1	284	A One-to-many Traffic Aware Wireless Network-in-Package for Multi-Chip Computing Platforms
Ahn, Byungmin	T1A.2	221	Memory Access Driven Memory Layout and Block Replacement Techniques for Compressed Deep Neural Networks
Ahosan Ul Karim, Muhammed Alkabani, Yousra	T2B.3		10T Differential-Signal SRAM Design in a 14-Nm FinFET Technology for High-Speed Application
Alnaggar, Omar	WP.8	169	PCNNA: A Photonic Convolutional Neural Network Accelerator
Amiri, Parviz	T2B.4		Smart Silicon Substrate for Quick Time to Market Chip-Stacks and Systems-in-Package
Ampadu, Paul	W2B.2	67	An Ultra-Low-Voltage Sub-threshold Pseudo-Differential CMOS Schmitt Trigger
Arunachalam, Meena	W2B.3	72	Reconfigurable Clock Generator with Wide Frequency Range and Single-Cycle Phase and Frequency Switching
Ataei, Samira	T1A.3	227	A Learning-guided Hierarchical Approach for Biomedical Image Segmentation
Baehr, Steffen	F1B.1	266	A Methodology for Low-Power Approximate Embedded SRAM Within Multimedia Applications
Balzer, Matthias	WP.9	174	Data Readout Triggering for Phase 2 of the Belle II Particle Detector Experiment Based on Neural Networks
Bao, Dongxuan	W3B.3	118	A Content-Adapted FPGA Memory Architecture with Pattern Recognition Capability and Interval Compressing Technique
Bastan, Yasin	W3B.4	124	An ASIC Design of Multi-Electrode Digital Basket Catheter Systems with Reconfigurable Compressed Sampling
Bayoumi, Magdy	W2B.2	67	An Ultra-Low-Voltage Sub-threshold Pseudo-Differential CMOS Schmitt Trigger
Becker, Juergen	F1A.3	260	Power-Thermal Aware Balanced Task-Resource Co-Allocation in Heterogeneous Many CPU-GPU Cores NoC in Dark Silicon Era
Beitollahi, Hakem	WP.5	152	Flexible Self-Healing Router for Reliable and High-Performance Network-on-Chips Architecture
Binek, Christian	WP.9	174	Data Readout Triggering for Phase 2 of the Belle II Particle Detector Experiment Based on Neural Networks
Bird, Jonathan	W3B.3	118	A Content-Adapted FPGA Memory Architecture with Pattern Recognition Capability and Interval Compressing Technique
	WP.7	163	PAT-NOXIM: A Precise Power & Thermal Cycle-Accurate NoC Simulator
	WP.4	146	Compact Modeling and Design of Magneto-electric Transistor Devices and Circuits
	WP.4	146	Compact Modeling and Design of Magneto-electric Transistor Devices and Circuits

Burnett, David	T2B.3		10T Differential-Signal SRAM Design in a 14-Nm FinFET Technology for High-Speed Application
Cacciotti, Mattia	WP.6	158	Hardware Acceleration of HDR-Image Tone Mapping on an FPGA-CPU Platform Through High-Level Synthesis
Cadore Cataldo, Rodrigo	F2A.3	296	Broadcast- And Power-aware Wireless NoC for Barrier Synchronization in Parallel Computing
Camus, Vincent	WP.6	158	Hardware Acceleration of HDR-Image Tone Mapping on an FPGA-CPU Platform Through High-Level Synthesis
Chan, Yun-Sheng	F1B.2	272	0.4V Reconfigurable Near-Threshold TCAM in 28Nm High-k Metal-Gate CMOS Process
Chang, Zhe-Wei	F2B.1	302	A Low-Area, Low-Power, and Low-Leakage Error-Detecting Latch for Timing-Error Resilient System Designs
Chen, Alan	WP.2	136	Building an Acceleration Overlay for Novice Students
Chen, Bo-Hao	F1A.1	250	Near-Threshold CORDIC Design with Dynamic Circuitry for Long-Standby IoT Applications
Chen, Chi-Shi	T1B.2	238	Universal CMOS Diamond-graph Circuit for Embedded Computing
	W2B.4	78	A New Circuit Topology for High-Performance Pulsed Time-of-Flight Laser Radar Receivers
Chen, DiHu			An Output-Capacitorless Adaptively Biased Low-Dropout Regulator with Maximum 132-MHz UGF and Without Minimum Loading Requirement
	W2B.1	61	
Chen, He	WP.12	192	An Automated Fault Injection Platform for Fault Tolerant FFT Implemented in SRAM-Based FPGA
Chen, Zhe	F1B.3	278	Energy-Efficient SRAM Design with Data-Aware Dual-Modes 10T Storage Cell for CNN Processors
Cheng, Shun-Wen	T1B.2	238	Universal CMOS Diamond-graph Circuit for Embedded Computing
Chitnis, Kedar	T2B.2		Integrated Surround & CMS Automotive SoC
Choi, Kyusun	T1B.1	233	Designing Algorithm for the High Speed TIQ ADC, with Improved Accuracy
Chonnad, Shivakumar	WP.13	197	A Quantitative Approach to SoC Functional Safety Analysis
Chou, Pei-Yuan	F1A.1	250	Near-Threshold CORDIC Design with Dynamic Circuitry for Long-Standby IoT Applications
Chu, Haoming	W3B.4	124	An ASIC Design of Multi-Electrode Digital Basket Catheter Systems with Reconfigurable Compressed Sampling
Chuang, Ching-Te	F1B.2	272	0.4V Reconfigurable Near-Threshold TCAM in 28Nm High-k Metal-Gate CMOS Process
Coustans, Mathieu	F2B.2	308	A 32kHz Crystal Oscillator Leveraging Voltage Scaling in an Ultra-Low Power 40nA Real-Time Clock
Dabral, Shashank	T2B.2		Integrated Surround & CMS Automotive SoC
DallaPiazza, Silvio	F2B.2	308	A 32kHz Crystal Oscillator Leveraging Voltage Scaling in an Ultra-Low Power 40nA Real-Time Clock
Das, Chita	T1A.3	227	A Learning-guided Hierarchical Approach for Biomedical Image Segmentation
Deb, Sujay	F2A.3	296	Broadcast- And Power-aware Wireless NoC for Barrier Synchronization in Parallel Computing

Dellea, Mario	F2B.2	308	A 32kHz Crystal Oscillator Leveraging Voltage Scaling in an Ultra-Low Power 40nA Real-Time Clock
	T2B.5		Low Power 20 Gbps Type-C USB3.2/DP1.4/Thunderbolt3 Combo Linear Redriver in 0.25 Mm BiCMOS Technology
Delshadpour, Siamak	W1B.2	29	A 64 dB Dynamic Range Programmable Gain Amplifier for Dual Band WLAN 802.11Abg IF Receiver in 0.18 Um CMOS Technology
	W1B.1	23	An FSK Transceiver for USB Power Delivery in 0.14-Um CMOS Technology
Derafshi, Danesh	WP.7	163	PAT-NOXIM: A Precise Power & Thermal Cycle-Accurate NoC Simulator
Diguet, Jean-Philippe	F2A.3	296	Broadcast- And Power-aware Wireless NoC for Barrier Synchronization in Parallel Computing
Dowben, Peter	WP.4	146	Compact Modeling and Design of Magneto-electric Transistor Devices and Circuits
Dutt, Yashwant	T2B.2		Integrated Surround & CMS Automotive SoC
El-Araby, Esam	W2A.3	49	A Scalable High-Precision and High-Throughput Architecture for Emulation of Quantum Algorithms
El-Ghazawi, Tarek	WP.8	169	PCNNA: A Photonic Convolutional Neural Network Accelerator
Eldash, Omar	WP.5	152	Flexible Self-Healing Router for Reliable and High-Performance Network-on-Chips Architecture
Enz, Christian	WP.6	158	Hardware Acceleration of HDR-Image Tone Mapping on an FPGA-CPU Platform Through High-Level Synthesis
Fang, Ya-Bei	F1A.1	250	Near-Threshold CORDIC Design with Dynamic Circuitry for Long-Standby IoT Applications
Gacusan, Michael	W1A.3	13	Cloud Motion Vector Estimation Using Scalable Wireless Sensor Networks
Ganguly, Amlan	F2A.1	284	A One-to-many Traffic Aware Wireless Network-in-Package for Multi-Chip Computing Platforms
Gloster, Clay	WP.2	136	Building an Acceleration Overlay for Novice Students
Godat, Yves	F2B.2	308	A 32kHz Crystal Oscillator Leveraging Voltage Scaling in an Ultra-Low Power 40nA Real-Time Clock
Goel, Tarun	W3A.3	96	A High-performance VLSI Architecture of the PRESENT Cipher and Its Implementations for SoCs
Goswami, Piyali	T2B.2		Integrated Surround & CMS Automotive SoC
Grover, Anuj	WP.14	203	A 81nW Error Amplifier Design for Ultra Low Leakage Retention Mode Operation of 4Mb SRAM Array in 40Nm LSTP Technology
Gu, Jie	W1A.2	7	Holistic Energy Management with μ Processor Co-Optimization in Fully Integrated Battery-less IoTs
	W2B.4	78	A New Circuit Topology for High-Performance Pulsed Time-of-Flight Laser Radar Receivers
Guo, Jianping			An Output-Capacitorless Adaptively Biased Low-Dropout Regulator with Maximum 132-MHz UGF and Without Minimum Loading Requirement
	W2B.1	61	
Hagan, Matthew	WP.3	140	Pro-Active Policing and Policy Enforcement Architecture for Securing MPSoCs

	W3A.1	84	Policy-Based Security Modelling and Enforcement Approach for Emerging Embedded Architectures
Ham, Daesik	T1A.1	215	Reducing Memory Interference Latency of Safety-Critical Applications via Memory Request Throttling and Linux Cgroup
Hamedi-Hagh, Sotoudeh	W2B.2	67	An Ultra-Low-Voltage Sub-threshold Pseudo-Differential CMOS Schmitt Trigger
	W1B.3	33	Design and Analysis of 66GHz Voltage Controlled Oscillators for FMCW Radar Applications with Phase Noise Impact Consideration
Harbaum, Tanja	W3B.3	118	A Content-Adapted FPGA Memory Architecture with Pattern Recognition Capability and Interval Compressing Technique
Hernandez, Hugo	F2B.3	314	0.5V 10MS/s 9-Bits Asynchronous SAR ADC for BLE Receivers in 180Nm CMOS Technology
Hester, Josiah	W1A.2	7	Holistic Energy Management with μ Processor Co-Optimization in Fully Integrated Battery-less IoTs
Higuchi, Tatsuhiko	W3B.2	112	Performance Modeling of VIA-switch FPGA for Device-Circuit-Architecture Co-Optimization
Hong, Seongsoo	T1A.1	215	Reducing Memory Interference Latency of Safety-Critical Applications via Memory Request Throttling and Linux Cgroup
Hosseini, Morteza	T1B.3	244	MPT: Multiple Parallel Tempering for High-Throughput MCMC Samplers
	W2A.2	43	A Low-Power Arithmetic Element for Multi-Base Logarithmic Computation on Deep Neural Networks
Huan, Yuxiang	W3B.4	124	An ASIC Design of Multi-Electrode Digital Basket Catheter Systems with Reconfigurable Compressed Sampling
Huang, Po-Tsang	F1B.2	272	0.4V Reconfigurable Near-Threshold TCAM in 28Nm High-k Metal-Gate CMOS Process
			An Output-Capacitorless Adaptively Biased Low-Dropout Regulator with Maximum 132-MHz UGF and Without Minimum Loading Requirement
Huang, Siji	W2B.1	61	
			0.4V Reconfigurable Near-Threshold TCAM in 28Nm High-k Metal-Gate CMOS Process
Hwang, Wei	F1B.2	272	
Iacob, Radu	WP.13	197	A Quantitative Approach to SoC Functional Safety Analysis
Ichihashi, Motoi	T2B.3		10T Differential-Signal SRAM Design in a 14-Nm FinFET Technology for High-Speed Application
Ishihara, Tohru	W3B.2	112	Performance Modeling of VIA-switch FPGA for Device-Circuit-Architecture Co-Optimization
Islam, Rashidul	T1B.3	244	MPT: Multiple Parallel Tempering for High-Throughput MCMC Samplers
Jadav, Brijesh	T2B.2		Integrated Surround & CMS Automotive SoC
Jadhav, Shrikant	WP.2	136	Building an Acceleration Overlay for Novice Students
Jamal, Lafifa	WP.10	180	Towards Designing Optimized Low Power Reversible Demultiplexer for Emerging Nanocircuits
Jia, Tianyu	W1A.2	7	Holistic Energy Management with μ Processor Co-Optimization in Fully Integrated Battery-less IoTs
Jiang, Huaipan	T1A.3	227	A Learning-guided Hierarchical Approach for Biomedical Image Segmentation
Jiang, Yingtao	W1A.1	1	On a New Hardware Trojan Attack on Power Budgeting of Many Core Systems

Jondhale, Prasad	T2B.2		Integrated Surround & CMS Automotive SoC
Jones, Jason	T2B.2		Integrated Surround & CMS Automotive SoC
Joshi, Vivek	T2B.3		10T Differential-Signal SRAM Design in a 14-Nm FinFET Technology for High-Speed Application
Kallback, Bengt	W3B.4	124	An ASIC Design of Multi-Electrode Digital Basket Catheter Systems with Reconfigurable Compressed Sampling
Kandemir, Mahmut	T1A.3	227	A Learning-guided Hierarchical Approach for Biomedical Image Segmentation
Karmakar, Abhijit	W3A.3	96	A High-performance VLSI Architecture of the PRESENT Cipher and Its Implementations for SoCs
Kawar, Sanad	W1A.4	19	A Discontinuous Charging Technique with Programmable Duty-Cycle for Switched-Capacitor Based Energy Harvesting Circuits in IoT Applications
Kayal, Maher	F2B.2	308	A 32kHz Crystal Oscillator Leveraging Voltage Scaling in an Ultra-Low Power 40nA Real-Time Clock
Kempf, Fabian	WP.9	174	Data Readout Triggering for Phase 2 of the Belle II Particle Detector Experiment Based on Neural Networks
Khalil, Kasem	WP.5	152	Flexible Self-Healing Router for Reliable and High-Performance Network-on-Chips Architecture
Kim, Jungho	T1A.1	215	Reducing Memory Interference Latency of Safety-Critical Applications via Memory Request Throttling and Linux Cgroup
Kim, Taewhan	T1A.2	221	Memory Access Driven Memory Layout and Block Replacement Techniques for Compressed Deep Neural Networks
Kim, Youngsoo	WP.2	136	Building an Acceleration Overlay for Novice Students
Kotra, Jagadish	T1A.3	227	A Learning-guided Hierarchical Approach for Biomedical Image Segmentation
Krishnan, Shoba	W1A.4	19	A Discontinuous Charging Technique with Programmable Duty-Cycle for Switched-Capacitor Based Energy Harvesting Circuits in IoT Applications
Krummenacher, François	F2B.2	308	A 32kHz Crystal Oscillator Leveraging Voltage Scaling in an Ultra-Low Power 40nA Real-Time Clock
Ku, Bon Woong	W2A.1	37	A Twin Memristor Synapse for Spike Timing Dependent Learning in Neuromorphic Systems
Kumar, Ashok	WP.5	152	Flexible Self-Healing Router for Reliable and High-Performance Network-on-Chips Architecture
Kumar, Rakesh	T2B.4		Smart Silicon Substrate for Quick Time to Market Chip-Stacks and Systems-in-Package
Kwon, Soobum	T1B.1	233	Designing Algorithm for the High Speed TIQ ADC, with Improved Accuracy
LaMoyne, Noah	WP.2	136	Building an Acceleration Overlay for Novice Students
Li, Kaiyou	W2B.4	78	A New Circuit Topology for High-Performance Pulsed Time-of-Flight Laser Radar Receivers
Li, Yicheng	W2B.1	61	An Output-Capacitorless Adaptively Biased Low-Dropout Regulator with Maximum 132-MHz UGF and Without Minimum Loading Requirement

Lim, Sung Kyu	W2A.1	37	A Twin Memristor Synapse for Spike Timing Dependent Learning in Neuromorphic Systems
Lin, Chun-Pin	T1B.2	238	Universal CMOS Diamond-graph Circuit for Embedded Computing
	F2B.1	302	A Low-Area, Low-Power, and Low-Leakage Error-Detecting Latch for Timing-Error Resilient System Designs
Lin, Tay-Jyi	F1A.1	250	Near-Threshold CORDIC Design with Dynamic Circuitry for Long-Standby IoT Applications
Litovtchenko, Vladimir	WP.13	197	A Quantitative Approach to SoC Functional Safety Analysis
	F2B.1	302	A Low-Area, Low-Power, and Low-Leakage Error-Detecting Latch for Timing-Error Resilient System Designs
Liu, Chien-Tung	F1A.1	250	Near-Threshold CORDIC Design with Dynamic Circuitry for Long-Standby IoT Applications
Liu, Xinjun	F1B.3	278	Energy-Efficient SRAM Design with Data-Aware Dual-Modes 10T Storage Cell for CNN Processors
Liu, Yi	WP.1	130	A Multi-Objective Architecture Optimization Method for Application-Specific NoC Design
Lu, Zhaojun	W3A.2	90	An Entropy Analysis Based Intrusion Detection System for Controller Area Network in Vehicles
Lung, Sheng-Chi	F1B.2	272	0.4V Reconfigurable Near-Threshold TCAM in 28Nm High-k Metal-Gate CMOS Process
Luo, Li	F1B.3	278	Energy-Efficient SRAM Design with Data-Aware Dual-Modes 10T Storage Cell for CNN Processors
Mahdavi, Amir	W1B.3	33	Design and Analysis of 66GHz Voltage Controlled Oscillators for FMCW Radar Applications with Phase Noise Impact Consideration
Mahmud, Naveed	W2A.3	49	A Scalable High-Precision and High-Throughput Architecture for Emulation of Quantum Algorithms
Mak, Terrence	W1A.1	1	On a New Hardware Trojan Attack on Power Budgeting of Many Core Systems
Mamgain, Ankush	WP.14	203	A 81nW Error Amplifier Design for Ultra Low Leakage Retention Mode Operation of 4Mb SRAM Array in 40Nm LSTP Technology
Mansoor, Naseef	F2A.1	284	A One-to-many Traffic Aware Wireless Network-in-Package for Multi-Chip Computing Platforms
Mao, ChuangAn	WP.12	192	An Automated Fault Injection Platform for Fault Tolerant FFT Implemented in SRAM-Based FPGA
Marcon, César	F2A.3	296	Broadcast- And Power-aware Wireless NoC for Barrier Synchronization in Parallel Computing
Marni, Lahir	T1B.3	244	MPT: Multiple Parallel Tempering for High-Throughput MCMC Samplers
Marshall, Andrew	WP.4	146	Compact Modeling and Design of Magneto-electric Transistor Devices and Circuits
Martin, Kevin	F2A.3	296	Broadcast- And Power-aware Wireless NoC for Barrier Synchronization in Parallel Computing
Mehrabian, Armin	WP.8	169	PCNNA: A Photonic Convolutional Neural Network Accelerator
Mitharwal, Chhavi	W3A.3	96	A High-performance VLSI Architecture of the PRESENT Cipher and Its Implementations for SoCs
Mo, Bing	W2B.4	78	A New Circuit Topology for High-Performance Pulsed Time-of-Flight Laser Radar Receivers

	W2B.1	61	An Output-Capacitorless Adaptively Biased Low-Dropout Regulator with Maximum 132-MHz UGF and Without Minimum Loading Requirement
Mody, Mihir	T2B.2		Integrated Surround & CMS Automotive SoC
Mohsenin, Tinoosh	T1B.3	244	MPT: Multiple Parallel Tempering for High-Throughput MCMC Samplers
Mondal, Hemanta	F2A.3	296	Broadcast- And Power-aware Wireless NoC for Barrier Synchronization in Parallel Computing
Muthukumar, Venkatesan	W1A.3	13	Cloud Motion Vector Estimation Using Scalable Wireless Sensor Networks
Narayanan, Vijaykrishnan	WP.11	186	Noise Aware Power Adaptive Partitioned Deep Networks for Mobile Visual Assist Platforms
Nasrollahpour, Mehdi	W2B.2	67	An Ultra-Low-Voltage Sub-threshold Pseudo-Differential CMOS Schmitt Trigger
	W1B.3	33	Design and Analysis of 66GHz Voltage Controlled Oscillators for FMCW Radar Applications with Phase Noise Impact Consideration
Nasrullah, Jawad	T2B.4		Smart Silicon Substrate for Quick Time to Market Chip-Stacks and Systems-in-Package
Nayak, Mausam	W3A.3	96	A High-performance VLSI Architecture of the PRESENT Cipher and Its Implementations for SoCs
Nejati, Ali	W2B.2	67	An Ultra-Low-Voltage Sub-threshold Pseudo-Differential CMOS Schmitt Trigger
Nikonov, Dmitri	WP.4	146	Compact Modeling and Design of Magneto-electric Transistor Devices and Circuits
Noh, Soonhyun	T1A.1	215	Reducing Memory Interference Latency of Safety-Critical Applications via Memory Request Throttling and Linux Cgroup
Norollah, Amin	WP.7	163	PAT-NOXIM: A Precise Power & Thermal Cycle-Accurate NoC Simulator
Onodera, Hidetoshi	W3B.2	112	Performance Modeling of VIA-switch FPGA for Device-Circuit-Architecture Co-Optimization
Pandey, Jai	W3A.3	96	A High-performance VLSI Architecture of the PRESENT Cipher and Its Implementations for SoCs
Park, Jun Hyuk	T1B.1	233	Designing Algorithm for the High Speed TIQ ADC, with Improved Accuracy
Patooghy, Ahmad	WP.7	163	PAT-NOXIM: A Precise Power & Thermal Cycle-Accurate NoC Simulator
Perera, Darshika	W3B.1	106	Optimized Counter-Based Multi-Ported Memory Architectures for Next-Generation FPGAs
Pezzotta, Alessandro	WP.6	158	Hardware Acceleration of HDR-Image Tone Mapping on an FPGA-CPU Platform Through High-Level Synthesis
Purkayastha, Arnab	W2A.4	55	Taxonomy of Spatial Parallelism on FPGAs for Massively Parallel Applications
Ardhendu			
Purswani, Hardeep	F2A.1	284	A One-to-many Traffic Aware Wireless Network-in-Package for Multi-Chip Computing Platforms
Qiao, Fei	F1B.3	278	Energy-Efficient SRAM Design with Data-Aware Dual-Modes 10T Storage Cell for CNN Processors
Qin, Yajie	W3B.4	124	An ASIC Design of Multi-Electrode Digital Basket Catheter Systems with Reconfigurable Compressed Sampling

Qu, Gang	W3A.2	90	An Entropy Analysis Based Intrusion Detection System for Controller Area Network in Vehicles
Quraini, Abood	T2B.1		<i>DFT, PD & PO Aspects of Xavier - Flagship SOC for Autonomous Driving and Deep Learning</i>
Radfar, Sara	W2B.2	67	An Ultra-Low-Voltage Sub-threshold Pseudo-Differential CMOS Schmitt Trigger
Ramezanpour, Keyvan	W2B.3	72	Reconfigurable Clock Generator with Wide Frequency Range and Single-Cycle Phase and Frequency Switching
Reza, Md Farhadur	F1A.3	260	Power-Thermal Aware Balanced Task-Resource Co-Allocation in Heterogeneous Many CPU-GPU Cores NoC in Dark Silicon Era
Roelke, Alec	F1A.2	254	Co-optimizing CPUs and Accelerators in Constrained Systems
Rose, Garrett	W2A.1	37	A Twin Memristor Synapse for Spike Timing Dependent Learning in Neuromorphic Systems
	WP.15	209	A Practical Sense Amplifier Design for Memristive Crossbar Circuits (PUF)
Rossi, Luca	F2B.2	308	A 32kHz Crystal Oscillator Leveraging Voltage Scaling in an Ultra-Low Power 40nA Real-Time Clock
Ryoo, Jihyun	T1A.3	227	A Learning-guided Hierarchical Approach for Biomedical Image Segmentation
Sagar, Rajat	T2B.2		Integrated Surround & CMS Automotive SoC
Sampson, Jack	WP.11	186	Noise Aware Power Adaptive Partitioned Deep Networks for Mobile Visual Assist Platforms
Sarma, Anup	T1A.3	227	A Learning-guided Hierarchical Approach for Biomedical Image Segmentation
Sayyaparaju, Sagarvarma	W2A.1	37	A Twin Memristor Synapse for Spike Timing Dependent Learning in Neuromorphic Systems
Schlachter, Jeremy	WP.6	158	Hardware Acceleration of HDR-Image Tone Mapping on an FPGA-CPU Platform Through High-Level Synthesis
Schuman, Catherine	W2A.1	37	A Twin Memristor Synapse for Spike Timing Dependent Learning in Neuromorphic Systems
Severo, Lucas	F2B.3	314	0.5V 10MS/s 9-Bits Asynchronous SAR ADC for BLE Receivers in 180Nm CMOS Technology
Sezer, Sakir	WP.3	140	Pro-Active Policing and Policy Enforcement Architecture for Securing MPSoCs
	W3A.1	84	Policy-Based Security Modelling and Enforcement Approach for Emerging Embedded Architectures
Shahriat, Sajeed	F2A.1	284	A One-to-many Traffic Aware Wireless Network-in-Package for Multi-Chip Computing Platforms
Shahrrouzi, S. Navid	W3B.1	106	Optimized Counter-Based Multi-Ported Memory Architectures for Next-Generation FPGAs
Sharma, Nishtha	WP.4	146	Compact Modeling and Design of Magneto-electric Transistor Devices and Circuits
Shi, Hao	WP.12	192	An Automated Fault Injection Platform for Fault Tolerant FFT Implemented in SRAM-Based FPGA
Shiddibhavi, Suhas Ashok	W2A.4	55	Taxonomy of Spatial Parallelism on FPGAs for Massively Parallel Applications
Shin, Philkyue	T1A.1	215	Reducing Memory Interference Latency of Safety-Critical Applications via Memory Request Throttling and Linux Cgroup

Shurtz, Gregory	T2B.2		Integrated Surround & CMS Automotive SoC
Siddiqui, Fahad	WP.3	140	Pro-Active Policing and Policy Enforcement Architecture for Securing MPSoCs
Manzoor	W3A.1	84	Policy-Based Security Modelling and Enforcement Approach for Emerging Embedded Architectures
Sierro, Yves	F2B.2	308	A 32kHz Crystal Oscillator Leveraging Voltage Scaling in an Ultra-Low Power 40nA Real-Time Clock
Singh, Amit	W1A.1	1	On a New Hardware Trojan Attack on Power Budgeting of Many Core Systems
Singh, Raj	W3A.3	96	A High-performance VLSI Architecture of the PRESENT Cipher and Its Implementations for SoCs
Sivasankaran, Shiju	T2B.2		Integrated Surround & CMS Automotive SoC
Sorger, Volker	WP.8	169	PCNNA: A Photonic Convolutional Neural Network Accelerator
Sridhar, Ramalingam	F2A.2	290	Centralized Priority Management Allocation for Network-on-Chip Router
Srinivasan, Rajagopalan	T2B.1		<i>DFT, PD & PO Aspects of Xavier - Flagship SOC for Autonomous Driving and Deep Learning</i>
Stan, Mircea	F1A.2	254	Co-optimizing CPUs and Accelerators in Constrained Systems
Stine, James	F1B.1	266	A Methodology for Low-Power Approximate Embedded SRAM Within Multimedia Applications
Tabkhi, Hamed	W2A.4	55	Taxonomy of Spatial Parallelism on FPGAs for Massively Parallel Applications
Taylor, Greg	T2B.4		Smart Silicon Substrate for Quick Time to Market Chip-Stacks and Systems-in-Package
Tsai, Wei-Chang	T1B.2	238	Universal CMOS Diamond-graph Circuit for Embedded Computing
Uddin, Mesbah	WP.15	209	A Practical Sense Amplifier Design for Memristive Crossbar Circuits (PUF)
Uddin, Riaz	WP.10	180	Towards Designing Optimized Low Power Reversible Demultiplexer for Emerging Nanocircuits
Van Noije, Wilhelmus	F2B.3	314	0.5V 10MS/s 9-Bits Asynchronous SAR ADC for BLE Receivers in 180Nm CMOS Technology
Wang, Jinn-Shyan	F2B.1	302	A Low-Area, Low-Power, and Low-Leakage Error-Detecting Latch for Timing-Error Resilient System Designs
	F1A.1	250	Near-Threshold CORDIC Design with Dynamic Circuitry for Long-Standby IoT Applications
Wang, Qian	W3A.2	90	An Entropy Analysis Based Intrusion Detection System for Controller Area Network in Vehicles
Wang, Wei-Chang	F1B.2	272	0.4V Reconfigurable Near-Threshold TCAM in 28Nm High-k Metal-Gate CMOS Process
Wang, Xiaohang	W1A.1	1	On a New Hardware Trojan Attack on Power Budgeting of Many Core Systems
Weber, Marc	W3B.3	118	A Content-Adapted FPGA Memory Architecture with Pattern Recognition Capability and Interval Compressing Technique
Wei, Qi	F1B.3	278	Energy-Efficient SRAM Design with Data-Aware Dual-Modes 10T Storage Cell for CNN Processors

Wei, Shih-Nung	F2B.1	302	A Low-Area, Low-Power, and Low-Leakage Error-Detecting Latch for Timing-Error Resilient System Designs
Wen, Yiming	W3A.4	102	Leakage Power Analysis (LPA) Attack in Breakdown Mode and Countermeasure
Woo, Youngtag	T2B.3		10T Differential-Signal SRAM Design in a 14-Nm FinFET Technology for High-Speed Application
Wu, Shang-Lin	F1B.2	272	0.4V Reconfigurable Near-Threshold TCAM in 28Nm High-k Metal-Gate CMOS Process
Xie, Yizhuang	WP.12	192	An Automated Fault Injection Platform for Fault Tolerant FFT Implemented in SRAM-Based FPGA
Xie, Yu	WP.12	192	An Automated Fault Injection Platform for Fault Tolerant FFT Implemented in SRAM-Based FPGA
Xu, Changqing	WP.1	130	A Multi-Objective Architecture Optimization Method for Application-Specific NoC Design
Xu, Han	F1B.3	278	Energy-Efficient SRAM Design with Data-Aware Dual-Modes 10T Storage Cell for CNN Processors
Xu, Jiawei	W2A.2	43	A Low-Power Arithmetic Element for Multi-Base Logarithmic Computation on Deep Neural Networks
Yan, Pengzhan	F2A.2	290	Centralized Priority Management Allocation for Network-on-Chip Router
Yang, Dylan	WP.2	136	Building an Acceleration Overlay for Novice Students
Yang, Huazhong	F1B.3	278	Energy-Efficient SRAM Design with Data-Aware Dual-Modes 10T Storage Cell for CNN Processors
Yang, Mei	W1A.1	1	On a New Hardware Trojan Attack on Power Budgeting of Many Core Systems
Yang, Yintang	WP.1	130	A Multi-Objective Architecture Optimization Method for Application-Specific NoC Design
Yogi, Nitin	T2B.1		<i>DFT, PD & PO Aspects of Xavier - Flagship SOC for Autonomous Driving and Deep Learning</i>
Yu, Weize	W3A.4	102	Leakage Power Analysis (LPA) Attack in Breakdown Mode and Countermeasure
Yun, Sunmin	WP.2	136	Building an Acceleration Overlay for Novice Students
Zhao, Danella	F1A.3	260	Power-Thermal Aware Balanced Task-Resource Co-Allocation in Heterogeneous Many CPU-GPU Cores NoC in Dark Silicon Era
Zhao, Yiming	W1A.1	1	On a New Hardware Trojan Attack on Power Budgeting of Many Core Systems
Zheng, Haoxin	W2B.4	78	A New Circuit Topology for High-Performance Pulsed Time-of-Flight Laser Radar Receivers
Zheng, Lirong	W2A.2	43	A Low-Power Arithmetic Element for Multi-Base Logarithmic Computation on Deep Neural Networks
	W3B.4	124	An ASIC Design of Multi-Electrode Digital Basket Catheter Systems with Reconfigurable Compressed Sampling
	WP.11	186	Noise Aware Power Adaptive Partitioned Deep Networks for Mobile Visual Assist Platforms
Zientara, Peter	W2A.2	43	A Low-Power Arithmetic Element for Multi-Base Logarithmic Computation on Deep Neural Networks
Zou, Zhuo	W3B.4	124	An ASIC Design of Multi-Electrode Digital Basket Catheter Systems with Reconfigurable Compressed Sampling