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2018 International Conference on ReConFigurable Computing and FPGAs (ReConFig18)

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General Sessions

Rafael Zamacola, Alberto García Martínez, Javier Mora, Andrés Otero and Eduardo de la Torre. IMPRESS: Automated Tool for the Implementation of Higly Flexible Partial Reconfigurable Systems with Xilinx Vivado

Tiziana Fanni, Alfonso Rodriguez, Carlo Sau, Leonardo Suriano, Francesca Palumbo, Luigi Raffo and Eduardo de la Torre. Multi-Grain Reconfiguration for Advanced Adaptivity in Cyber-Physical Systems

Gökhan Akgün, Habib ul Hasan Khan, Mahmoud Ahmed Elshimy and Diana Göhringer. Dynamic tunable and reconfigurable hardware controller with EKF-based state reconstruction through FPGA-in the loop

Dillon Huff and Pat Hanrahan. Using Runtime Circuit Specialization to Accelerate Simulations of Reconfigurable Architectures

Arpit Soni, Yoon Kah Leow and Ali Akoglu. Post-Routing Analytical Wirelength Model for Homogeneous FPGA Architectures

John McGlone, Paolo Palazzari and Jean-Babtiste Leclere. Accelerating Key In-memory Database Functionality with FPGA Technology

Alan Ehret, Mihailo Isakov and Michel A. Kinsy. Towards a Generalized Reconfigurable Agent Based Architecture: Stock Market Simulation Acceleration

Paulina M. Fusiara, Gijs Schoonderbeek, Johan Pragt, Leon Hiemstra, Menno Schuil, Sjouke Kuindersma and Grant A. Hampson. Design and Fabrication of Full Board Direct LiquidCooling Heat Sink for Densely Packed FPGA Processing Boards

Kalindu Herath, Alok Prakash, Jiang Guiyuan and Thambipillai Srikanthan. Ant Colony Optimization based Module Footprint Selection and Placement for Lowering Power in Large FPGA Designs

Takeharu Ikezoe, Hideharu Amano, Junya Akaike, Kudo Masaru, Kimiyoshi Usami, Keizo Hiraga, Yusuke Shuto and Kojiro Yagami. A Coarse Grained-Reconfigurable Accelerator with energy efficient MTJ-based Non-volatile Flip-flops

Hsin-Yu Ting, Ardalan Amiri Sani and Eli Bozorgzadeh. System Services for Reconfigurable Hardware Acceleration in Mobile Devices

Safdar Mahmood, Pavel Shydlouski and Michael Huebner. An Application Specific Framework for HLS-based FPGA Design of Articulated Robot Inverse Kinematics

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Gustavo Sutter, Mario Ruiz, Sergio López-Buedo and Gustavo Alonso. FPGA-based TCP/IP Checksum Offloading Engine for 100 Gbps Networks

Matthew Cauwels, Joseph Zambreno and Phillip H. Jones. HW/SW Configurable LQG Controller using a Sequential Discrete Kalman Filter

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Norbert Abel, William Kamp and Gianni Comoretto. Complex Multiply Accumulate Cells for the Square Kilometre Array Correlators

Ryo Kamasaka, Yuichiro Shibata and Kiyoshi Oguri. An FPGA-oriented Graph Cut Algorithm for Accelerating Stereo Vision

Joe Avey, Phillip H. Jones and Joseph Zambreno. An FPGA-based Hardware Accelerator for Iris Segmentation

Lester Kalms, Hassan Ibrahim and Diana Goehringer. Full-HD Accelerated and Embedded Feature Detection Video System with 63fps using ORB for FREAK

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Shuai Xie, Zhongyuan Zhao, Weiguang Sheng, Qin Wang and Zhigang Mao. MBSS:A General Paradigm for Static Schedule for Nested Loops with Dynamic Loop Boundary on CGRAs

Kris Heid and Christian Hochberger. AutoStreams: Fully Automatic parallelization of Legacy Embedded Applications with Soft-Core MPSoCs

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Ahmed Ferozpuri and Kris Gaj. High-speed FPGA Implementation of the NIST Round 1 Rainbow Signature Scheme

Michael Tempelmeier, Jens-Peter Kaps and Georg Sigl. Experimental Power and Performance Evaluation of CAESAR Hardware Finalists

Muhammad Abdul Wahab, Pascal Cotret, Mounir Nasr Allah, Guillaume Hiet, Vianney Lapotre, Guy Gogniat and Arnab Kumar Biswas. A small and adaptive coprocessor for information flow tracking in ARM SoCs

Daniel Ziener and Jutta Pirkl. Configuration Tampering of BRAM-based AES Implementations on FPGAs

William Harrison and Gerard Allwein. Language Abstractions for Hardware-based Control-Flow Integrity Monitoring

Zoya Dyka, Dan Kreiser, Ievgen Kabin and Peter Langendoerfer. Flexible FPGA ECDSA Design with a Field Multiplier Inherently Resistant against HCCA

Ievgen Kabin, Dan Kreiser, Zoya Dyka and Peter Langendoerfer. FPGA Implementation of ECC: Low-Cost Countermeasure against Horizontal Bus and Address-Bit SCA

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Franz-Josef Streit, Martin Letras, Stefan Wildermann, Benjamin Hackenberg, Joachim Falk, Andreas Becher and Jürgen Teich. Model-Based Design Automation of Hardware/Software Co-Designs for Xilinx Zynq PSoCs

Paul Sathre, Ahmed Helal and Wu-Chun Feng. A Composable Workflow for Productive Heterogeneous Computing on FPGAs via Whole-Program Analysis and Transformation

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Weiyi Sun, Hanqing Zeng, Yi-Hua Edward Yang and Viktor Prasanna. Throughput-Optimized Frequency Domain CNN with Fixed-Point Quantization on FPGA

Ahmed Abdelsalam, Felix Boulet, Gabriel Demers, J. M. Pierre Langlois and Farida Cheriet. An Efficient FPGA-based Overlay Inference Architecture for Fully Connected DNNs

Takashi Takemoto, Mertig Normann, Masato Hayashi, Saki Susa-Tanaka, Hiroshi Teramoto, Atsuyoshi Nakamura, Ichigaku Takigawa, Shin-Ichi Minato, Tamiki Komatsuzaki and Masanao Yamaoka. FPGA-Based QBoost with Large-Scale Annealing Processor and Accelerated Hyperparameter Search

PhD Forum

Philipp Käsgen, Markus Weinhardt and Christian Hochberger. A Coarse-Grained Reconfigurable Array for High-Performance Computing Applications

Sourya Dey, Diandian Chen, Zongyang Li, Souvik Kundu, Kuan-Wen Huang, Keith Chugg and Peter Beerel. A Highly Parallel FPGA Implementation of Sparse Neural Network Training