

2018 Conference on Design of Circuits and Integrated Systems (DCIS 2018)

**Lyon, France
14-16 November 2018**



**IEEE Catalog Number: CFP18DCI-POD
ISBN: 978-1-7281-0172-9**

**Copyright © 2018 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP18DCI-POD
ISBN (Print-On-Demand):	978-1-7281-0172-9
ISBN (Online):	978-1-7281-0171-2
ISSN:	2471-6170

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

TABLE OF CONTENTS

RUN-TIME MANAGEMENT OF ENERGY-PERFORMANCE TRADE-OFF IN OPTICAL NETWORK-ON-CHIP	1
<i>Jiating Luo ; Van-Dung Pham ; Cédric Killian ; Daniel Chillet ; Ian O’connor ; Olivier Sentieys ; Sébastien Le Beux</i>	
TIME-TO-DIGITAL CONVERTER WITH ADJUSTABLE RESOLUTION USING A DIGITAL VERNIER RING OSCILLATOR	7
<i>A. Annagrebah ; E. Bechetoille ; H. Chanal ; H. Mathez ; I. Laktineh</i>	
LOW PHASE-NOISE CMOS QUADRATURE OSCILLATOR BASED ON (N × 4)-STAGE SELF-TIMED RING	11
<i>Oussama Elissati ; Assia El-Hadbi ; Abdelkarim Cherkaoui ; Sébastien Rieubon ; Laurent Fesquet</i>	
ENERGY-AWARE ADAPTATIVE SUPERCAPACITOR STORAGE SYSTEM FOR MULTI-HARVESTING SOLUTIONS	16
<i>Albert Álvarez-Carulla ; Yaiza Montes-Cebrián ; Manel Puig-Vidal ; Jaime López-Sánchez ; Jordi Colomer-Farrarons ; Pere Miribel-Català</i>	
RELIABILITY ANALYSIS OF ON-CHIP WIRELESS LINKS FOR MANY CORE WNOCS	22
<i>Sri Harsha Gade ; Sidhartha Sankar Rout ; Ravi Kashyap ; Sujay Deb</i>	
DATA CONVERSION IN AREA-CONSTRAINED APPLICATIONS: THE WIRELESS NETWORK-ON-CHIP CASE	28
<i>Sergi Abadal ; Eduard Alarcón</i>	
EXPLORING THE PERFORMANCE-ENERGY OPTIMIZATION SPACE OF A BRIDGE BETWEEN 3D-STACKED ELECTRONIC AND OPTICAL NETWORKS-ON-CHIP	34
<i>Mahdi Tala ; Oliver Schrape ; Milos Krstic ; Davide Bertozzi</i>	
FROM RTL LIVENESS ASSERTIONS TO COST-EFFECTIVE HARDWARE CHECKERS	40
<i>Ranganathan Hariharan ; Tara Ghasempouri ; Behrad Niazmand ; Jaan Raik</i>	
DESIGN OF A FULLY INTEGRATED CMOS-PMUT SYSTEM	46
<i>I. Zamora ; E. Ledesma ; A. Uranga ; N. Barniol</i>	
RELIABILITY EMPHASIZED MTJ/CMOS HYBRID CIRCUIT TOWARDS ULTRA-LOW POWER	51
<i>Hao Cai ; Menglin Han ; You Wang ; Lirida Naviner ; Xinning Liu ; Jun Yang ; Weisheng Zhao</i>	
OPTIMAL ACCELERATED TEST REGIONS FOR TIME- DEPENDENT DIELECTRIC BREAKDOWN LIFETIME PARAMETERS ESTIMATION IN FINFET TECHNOLOGY	56
<i>Xexin Yang ; Rui Zhang ; Taizhi Liu ; Dae-Hyun Kim ; Linda Milor</i>	
INVESTIGATION OF CONDUCTIVITY CHANGES IN MEMRISTORS UNDER MASSIVE PULSED CHARACTERIZATION	62
<i>M. Pedro ; J. Martin-Martinez ; R. Rodriguez ; M. Nafria ; X. Aymerich</i>	
LOW-POWER FREQUENCY MONITORING CIRCUIT FOR CLOCK FAILURE DETECTION	66
<i>Rodrigo Capeleiro ; José M. Leitão ; Ricardo Chaves ; Marcelino B. Santos</i>	
RRAM CROSSBAR ARRAYS FOR STORAGE CLASS MEMORY APPLICATIONS: THROUGHPUT AND DENSITY CONSIDERATIONS	72
<i>A. Levisse ; B. Giraud ; J.-P. Noel ; M. Moreau ; J.-M. Portal</i>	
MULTIOCTAVE DISTRIBUTED MMIC POWER AMPLIFIER IN GALLIUM NITRIDE TECHNOLOGY WITH P_{1dB} > 31DBM	78
<i>Iban Barrutia ; Amparo Herrera ; Benoit Haentjens ; Laura Diego ; Charles A. Mjema</i>	
A FUEL CELL-BASED ADAPTABLE SELF-POWERED EVENT DETECTION PLATFORM ENHANCED FOR BIOSAMPLING APPLICATIONS	84
<i>Y. Montes-Cebrián ; A. Álvarez-Carulla ; J. Colomer-Farrarons ; M. Puig-Vidal ; J. López-Sánchez ; P. Miribel-Català</i>	
APPROXIMATE WIRELESS NETWORKS-ON-CHIP	90
<i>Giuseppe Ascia ; Vincenzo Catania ; Salvatore Monteleone ; Maurizio Palesi ; Davide Patti ; John Jose</i>	
VECTOR-BASED MISMATCH SHAPING CIRCUIT FOR A LOW IF MULTIBIT ΣΔ ADC	96
<i>M. Portela-Garcia ; V. M. Medina ; S. Paton</i>	
DESIGN FOR CALIBRATABILITY OF A N-INTEGGER LOW-FREQUENCY PHASE-LOCKED LOOP	102
<i>Rui Moutinho Teixeira ; José Machado Da Silva</i>	
ARFT: AN APPROXIMATIVE REDUNDANT TECHNIQUE FOR FAULT TOLERANCE	108
<i>Gennaro Severino Rodrigues ; Adria Barros De Oliveira ; Alberto Bosio ; Fernanda Lima Kastensmidt ; Edison Pignaton De Freitas</i>	

BREAKDOWN VOLTAGE SHIFT OF CMOS BURIED QUAD JUNCTION (BQJ) DETECTOR	114
<i>Thais Luana Vidal De Negreiros Da Silva ; Guo-Neng Lu ; Patrick Pittet</i>	
CMOS VCSEL DRIVER DEDICATED FOR SUB-NANOSECOND LASER PULSES GENERATION IN SPAD-BASED TIME-OF-FLIGHT RANGEFINDER	120
<i>S. Rigault ; N. Moeneclaey ; L. Labrak ; I. O'connor</i>	
A CMOS LOW FREQUENCY ANALOG RFID FRONT-END FOR THE IOT	126
<i>X. Zuriarrain ; A. Beriain ; G. Bistué ; D. Del Río ; R. Berenguer ; H. Solar ; J. Sosa ; J.A. Montiel-Nelson</i>	
SYSTEM-ON-PROGRAMMABLE-CHIP AES-GCM IMPLEMENTATION FOR WIRE-SPEED CRYPTOGRAPHY FOR SAS.....	132
<i>Mikel Rodríguez ; Armando Astarloa ; Jesús Lázaro ; Unai Bidarte ; Jaime Jiménez</i>	
EMBEDDED EMOTION RECOGNITION WITHIN CYBER-PHYSICAL SYSTEMS USING PHYSIOLOGICAL SIGNALS.....	138
<i>Jose Angel Miranda Calero ; Rodrigo Marino ; Jose M. Lanza-Gutierrez ; Teresa Riesgo ; Mario Garcia-Valderas ; Celia Lopez-Ongil</i>	
FINITE PRECISION ANALYSIS OF FPGA-BASED ARCHITECTURE FOR FBMC TRANSMULTIPLEXERS IN BROADBAND PLC	144
<i>Rubén Nieto ; Raúl Mateos ; Álvaro Hernández</i>	
EMBEDDED SYSTEM FOR DISTANCE MEASUREMENT AND SURFACE DISCRIMINATION APPLICATIONS	150
<i>Hélène Tap ; Laurent Gatet ; Emmanuel Moutaye ; Blaise Mulliez</i>	
PERFORMANCE-ORIENTED IMPLEMENTATION OF HILBERT FILTERS ON FPGAS	156
<i>Daniel Fortún ; Carlos García De La Cueva ; Jesús Grajal ; Marisa López-Vallejo ; Carlos López Barrio</i>	
SYSTEMATIC DESIGN METHOD OF PASSIVE LADDER FILTERS USING A GENERALISED VARIABLE.....	162
<i>Arthur Perodou ; Anton Komiiienko ; Gérard Scorletti ; Ian O'connor</i>	
SECURITY-ORIENTED CODE-BASED ARCHITECTURES FOR MITIGATING FAULT ATTACKS.....	168
<i>Batya Karp ; Mael Gay ; Osnat Keren ; Ilia Polian</i>	
LOW NOISE, HIGH EFFICIENCY, SEGMENTED LCD DRIVERS FOR ULTRA-LOW POWER APPLICATIONS IN 22 NM FD-SOI.....	174
<i>Rodrigo B. Capeleiro ; Marcelino B. Santos</i>	
AN INTEGRATED 10MHZ 3 STATES BUCK CONVERTER FOR FAST TRANSIENT RESPONSE IN 180NM CMOS	180
<i>Arnaud Toni ; Hassan Ihs ; Taner Dosluoglu ; Remy Cellier ; Nacer Abouchi</i>	
EFFICIENT SIMULATION OF FAULTS IN NETWORKED CYBER-PHYSICAL SYSTEMS.....	184
<i>Enrico Fraccaroli ; Davide Quaglia ; Franco Fummi</i>	
BENCHMARKING OF NANOMETER TECHNOLOGIES FOR DPA-RESILIENT DPL-BASED CRYPTOCIRCUITS	190
<i>E. Tena-Sánchez ; I. M. Delgado-Lozano ; J. Núñez ; A. J. Acosta</i>	
SINGLE EVENT TRANSIENT INJECTION IN LARGE MIXED-SIGNAL CIRCUITS.....	196
<i>Valentin Gutierrez ; Gildas Leger</i>	
EVENT STORMS IN IEC 61499 APPLICATIONS.....	202
<i>David Pescha ; Martin Horauer</i>	
MRAM: FROM STT TO SOT, FOR SECURITY AND MEMORY	207
<i>M. Kharbouche-Harrari ; R. Alhalabi ; J. Postel-Pellerin ; R. Wacquez ; D. Aboukassimi ; E. Nowak ; I.L. Prejbeanu ; G. Prenat ; G. Di Pendina</i>	
ESTIMATION OF THE OPTIMAL ACCELERATED TEST REGION FOR FINFET SRAMS DEGRADED BY FRONT-END AND BACK-END WEAROUT MECHANISMS	213
<i>Rui Zhang ; Kexin Yang ; Taizhi Liu ; Linda Milor</i>	
ASSESSING TEST PROCEDURE EFFECTIVENESS FOR POWER DEVICES	219
<i>D. Piumatti ; M. Sonza Reorda</i>	
FLOORPLANNING AS A PRACTICAL COUNTERMEASURE AGAINST CLOCK FAULT ATTACK IN TRIVIUM STREAM CIPHER	225
<i>F. E. Potestad-Ordóñez ; C. J. Jiménez-Fernández ; C. Baena-Oliva ; P. Parra-Fernández ; M. Valencia-Barrero</i>	
SOC ARCHITECTURE FOR AN ULTRASONIC RECEIVER APPLIED TO LOCAL POSITIONING SYSTEMS.....	231
<i>Álvaro Hernández ; Jesús Ureña ; José M. Villadangos ; Khaoula Mannay</i>	
IMPROVEMENT OF ACTIVE-INPUT CURRENT MIRRORS USING ADAPTIVE BIASING TECHNIQUE.....	236
<i>Mohan Julien ; Serge Bernard ; Fabien Soulier ; Vincent Kerzérho ; Guy Cathébras</i>	

QUANTUM DOT LOCATION RELEVANCE INTO SET-FET CIRCUITS BASED ON FINFET DEVICES 240
E. Amat ; A. Del Moral ; J. Bausells ; F. Perez-Murano ; F. Klüpfel
Author Index