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M. Kobayashi, The Univ. of Tokyo
K. Okada, Tokyo Institute of Technology
E. Naviasky, Cadence
G. Yeric, ARM Ltd.

Moderator: K. Makinwa, Delft Univ. of Technology

Panelists: B. Nauta, Univ. of Twente
Z. Wang, Tsinghua Univ.
F. Yinug, SIA
A. Piovaccari, Silicon Labs
S. Sumida, Woodside Capital Partners
J. Chang, TSMC

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K. Chang, Xilinx Inc

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T. Palacios, MIT

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N/A

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Moderator: A. DeVilliers, TEL

Panelists: K. Mistry, Intel Corp.
A. Yu, GLOBALFOUNDRIES Inc.
C. Chidambaram, Qualcomm Technologies, Inc.
P. Jung, Samsung
T. Ohba, Tokyo Tech. Univ.
K. Zhang, TSMC

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M. Ikeda, The Univ. of Tokyo
C.-P. Chang, Applied Materials, Inc.
K. Chang, Xilinx Inc

8:40-

Plenary

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B. Ginsburg, Texas Instruments

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Low-Power and ppm-Level Detection of Gas Molecules by Integrated Metal Nanosheets, T. Tanaka*, K. Tabuchi*, K. Tatehara*, Y. Shiiki*, S. Nakagawa*, T. Takahashi**, R. Shimizu*, H. Ishikuro*, T. Kuroda*, T. Yanagida** and K. Uchida****, *Keio Univ., **Kyushu Univ. and ***The Univ. of Tokyo, Japan

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JFS2-4 - 17:15

Record-High Performance Trantenna Based on Asymmetric Nano-Ring FET for Polarization-Independent Large-Scale/Real-Time THz Imaging, E.-S. Jang*, M. W. Ryu*, R. Patel*, S. H. Ahn*, H. J. Jeon*, K. Han** and K. R. Kim*, *Ulsan National Institute of Science and Technology and **Dongguk Univ., Korea

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JFS2-5 - 17:40

(Invited)

Custom Silicon and Sensors Developed for a 2nd Generation Augmented Reality User Interface, P. O'Connor, C. Meekhof, C. McBride, C. Mei, C. Bamji, D. Rohn, H. Strande, J. Forrester, M. Fenton, R. Haraden, T. Ozguner and T. Perry, Microsoft, USA.

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Technology / Circuits Joint Focus Session 3**Technology and System for AI [Shunju II, III]**

Thursday, June 13, 8:30-10:10

Chairpersons: H. Wu, Tsinghua Univ.

G. Yeric, ARM Ltd.

JFS3-1 - 8:30

(Invited)

Considerations of Integrating Computing-In-Memory and Processing-In-Sensorinto Convolutional Neural Network Accelerators for Low-Power Edge Devices, K.-T. Tang*, W.-C. Wei*, Z.-W. Yeh*, T.-H. Hsu*, Y.-C. Chiu*, C.-X. Xue*, Y.-C. Kuo*, T.-H. Wen*, M.-S. Ho**, C.-C. Lo*, R.-S. Liu*, C.-C. Hsieh* and M.-F. Chang*, *National Tsing Hua Univ. and **National Chung Hsin Univ., Taiwan

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JFS3-2 - 8:55 Computational Memory-Based Inference and Training of Deep Neural Networks , A. Sebastian*, I. Boybat***, M. Dazzi****, I. Giannopoulos****, V. Jonnalagadda*, V. Joshi****, G. Karunaratne****, B. Kersting****, R. Khaddam-Aljameh****, S. R. Nandakumar****, A. Petropoulos****, C. Piveteau****, T. Antonakopoulos****, B. Rajendran****, M. Le Gallo* and E. Eleftheriou*, *IBM Research, **EPFL, ***ETH Zürich, Switzerland, ****New Jersey Institute of Technology, USA, *****RWTH, Germany and *****Univ. of Patras, Greece	117
JFS3-3 - 9:20 A Ternary Based Bit Scalable, 8.80 TOPS/W CNN Accelerator with Many-Core Processing-in-Memory Architecture with 896K Synapses/mm² , S. Okumura, M. Yabuuchi, K. Hijioka and K. Nose, Renesas Electronics Corp., Japan	119
JFS3-4 - 9:45 Energy-Efficient Continual Learning in Hybrid Supervised-Unsupervised Neural Networks with PCM Synapses , S. Bianchi*, I. Muñoz-Martin*, G. Pedretti*, O. Melnic*, S. Ambrogio** and D. Ielmini*, *Politecnico di Milano, Italy and **IBM Research, USA	121
SESSION 14 - GeSn Device [Shunju I] Thursday, June 13, 8:30-10:10 Chairpersons: N. Sugii, Hitachi, Ltd. N. Collaert, imec	
T14-1 - 8:30 High Performance GeSn Photodiode on a 200 mm Ge-On-Insulator Photonics Platform for Advanced Optoelectronic Integration with Ge CMOS Operating at 2 μm Band , S. Xu*, K. Han*, Y.-C. Huang**, Y. Kang*, S. Masudy-Panah*, Y. Wu*, D. Lei*, Y. Zhao*, X. Gong* and Y.-C. Yeo*, *National Univ. of Singapore, Singapore and **Applied Materials, Inc., USA	123
T14-2 - 8:55 Record Low Contact Resistivity ($4.4 \times 10^{-10} \Omega\text{-cm}^2$) to Ge Using <i>In-Situ</i> B and Sn Incorporation by CVD with Low Thermal Budget ($\leq 400^\circ\text{C}$) and without Ga , F.-L. Lu*, C.-E. Tsai*, C.-H. Huang*, H.-Y. Ye*, S.-Y. Lin* and C. W. Liu***, *National Taiwan Univ. and **Taiwan Semiconductor Research Institute, Taiwan	125
T14-3 - 9:20 First Vertically Stacked, Compressively Strained, and Triangular Ge_{0.91}Sn_{0.09} pGAAFETs with High I_{ON} of 19.3 μA at V_{OV}=V_{DS}=-0.5V, G_m of 50.2 μS at V_{DS}=-0.5V and Low SS_{lin} of 84mV/Dec by CVD Epitaxy and Orientation Dependent Etching , Y.-S. Huang*, H.-Y. Ye*, F.-L. Lu*, Y.-C. Liu*, C.-T. Tu*, C.-Y. Lin*, S.-Y. Lin*, S.-R. Jan* and C. W. Liu***, *National Taiwan Univ. and **Taiwan Semiconductor Research Institute, Taiwan	127
T14-4 - 9:45 First Demonstration of Complementary FinFETs and Tunneling FinFETs Co-Integrated on a 200 mm GeSnOI Substrate: A Pathway Towards Future Hybrid Nano-Electronics Systems , K. Han*, Y. Wu*, Y. Huang**, S. Xu*, E. Kong*, A. Kumar*, Y. Kang*, J. Zhang*, C. Wang*, H. Xu*, C. Sun* and X. Gong*, *National Univ. of Singapore, Singapore and **Applied Materials, Inc., USA	129
Technology / Circuits Joint Focus Session 4 The Future of Memory [Shunju II, III] Thursday, June 13, 10:30-12:35 Chairpersons: H.-T. Lue, Macronix International Co., Ltd. G. Hemink, Western Digital Corp.	
JFS4-1 - 10:30 Circuit and Systems Based on Advanced MRAM for Near Future Computing Applications , S. Fujita, S. Takaya, S. Takeda and K. Ikegami, Toshiba, Japan	131
JFS4-2 - 10:55 Ag Ionic Memory Cell Technology for Terabit-Scale High-Density Application , S. Fujii*, R. Ichihara*, T. Konno*, M. Yamaguchi*, H. Seki*, H. Tanaka*, D. Zhao*, Y. Yoshimura*, M. Saitoh* and M. Koyama*, Toshiba Memory Corp., Japan	133
JFS4-3 - 11:20 Recent Progress and Next Directions for Embedded MRAM Technology , W. J. Gallagher, E. Chien, T.-W. Chiang, J.-C. Huang, M.-C. Shih, C. Y. Wang, C. Bair, G. Lee, Y.-C. Shih, C.-F. Lee, R. Wang, K.-H. Shen, J. J. Wu, W. Wang and H. Chuang, TSMC, Taiwan	135
JFS4-4 - 11:45 The PCM Way for Embedded Non Volatile Memories Applications , P. Zuliani, A. Conte and P. Cappelletti, STMicroelectronics, Italy	137
JFS4-5- 12:10 Manufacturable 300mm Platform Solution for Field-Free Switching SOT-MRAM , K. Garello, F. Yasin, H. Hody, S. Couet, L. Souriau, S. H. Sharifi, J. Swerts, R. Carpenter, S. Rao, K. Sethu, J. Wu, D. Crotti, A. Furnémont, G. S. Kar, W. Kim, M. Pak and N. Jossart, imec, Belgium	139
SESSION 15 - Advanced FinFET & GAA II [Shunju II] Thursday, June 13, 10:30-12:35 Chairpersons: H. Morioka, Socionext Inc. W. Rachmady, Intel Corp.	
T15-1 - 10:30 12-EUV Layer Surrounding Gate Transistor (SGT) for Vertical 6-T SRAM: 5-nm-Class Technology for Ultra-Density Logic Devices , M. S. Kim*, N. Harada**, Y. Kikuchi*, J. Boemmels*, J. Mitard*, T. Huynh-Bao*, P. Matagne*, Z. Tao*, W. Li*, K. Devriendt*, L.-A. Ragnarsson*, C. Lorant*, D. Mocuta*, F. Masuoka**, F. Sebaai*, C. Porret*, E. Rosseel*, A. Dangol*, D. Batuk*, G. Martinez-Alanis*, J. Geypen*, N. Jourdan*, A. Sepulveda*, H. Puliyalil*, G. Jamieson*, M. van der Veen*, L. Teugels*, Z. El-Mekki*, E. Altamirano-Sanchez*, Y. Li** and H. Nakamura**, *imec, Belgium and **Unisantis, Singapore	141
T15-2 - 10:55 Self-Heating Temperature Behavior Analysis for DC - GHz Design Optimization in Advanced FinFETs , S.-L. Liu, J. J. Horng, A. Akundu, Y. C. Hsu, B. S. Lien, S. F. Liu, C. W. Chang, H. D. Hsieh, D. S. Huang, Y. C. Peng, S. Liu and M. Chen, TSMC, Taiwan	143
T15-3 - 11:20 Economics of Semiconductor Scaling, A Cost Analysis for Advanced Technology Node , A. Mallik, J. Ryckaert, R.-H. Kim, P. Debacker, S. Decoster, F. Lazzarino, R. Ritzenthaler, N. Horiguchi, D. Verkest and A. Mocuta, imec, Belgium	145
T15-4 - 11:45 Device-, Circuit- & Block-Level Evaluation of CFET in a 4 Track Library , P. Schuddinck*, O. Zografos*, P. Weckx*, P. Matagne*, S. Sarkar*, Y. Sherazi*, R. Baert*, D. Jang*, D. Yakimets*, A. Gupta*, B. Parvais***, J. Ryckaert*, D. Verkest* and A. Mocuta*, *imec and **Vrije Universiteit Brussel, Belgium	147
T15-5 - 12:10 2nm Node: Benchmarking FinFET Vs Nano-Slab Transistor Architectures for Artificial Intelligence and Next Gen Smart Mobile Devices , S. C. Song*, C. Chidambaram*, B. Colombeau**, M. Bauer**, S. Natarajan**, V. Moroz***, X.-W. Lin***, D. Sherlekar***, M. Choi***, J. Huang***, P. Asenov**** and B. Cheng****, *Qualcomm Technologies, Inc., **Applied Materials, Inc., ***Synopsys, Inc., USA and ****Synopsys, Inc., UK	149
Luncheon Talk [Suzaku I] Thursday, June 13, 12:35-14:00	
Developing Visual Systems for Entertainment and Art , Y. Hanai, Rhizomatiks, Japan	

SESSION 16 - 3D NAND [Shnju II, III]

Thursday, June 13, 14:00-15:40

Chairpersons: K. Hamada, Micron Memory Japan, Inc.
G. Hemink, Western Digital Corp.

T16-1 - 14:00

Advantage of Extremely-Thin Body (Tsi~3nm) Device to Boost The Memory Window for 3D NAND Flash, H.-T. Lue, C. C. Hsieh, T. H. Hsu, W. C. Chen, C. P. Chen, C. Chiu, K.-C. Wang and C.-Y. Lu, Macronix International Co., Ltd., Taiwan

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T16-2 - 14:25

A Novel Confined Nitride-Trapping Layer Device for 3D NAND Flash with Robust Retention Performances, C.-H. Fu, H.-T. Lue, T.-H. Hsu, W.-C. Chen, G.-R. Lee, C.-J. Chiu, K.-C. Wang and C.-Y. Lu, Macronix International Co., Ltd., Taiwan

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T16-3 - 14:50

Modeling of Charge Loss Mechanisms During The Short Term Retention Operation in 3-D NAND Flash Memories, C. Woo*, M. Lee**, S. Kim*, J. Park*, G.-B. Choi**, M.-S. Seo**, K. H. Noh**, M. Kang*** and H. Shin*, *Seoul National Univ., **SK hynix Inc. and ***Korea National Univ. of Transportation, Korea

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T16-4 - 15:15

Pre-Shipment Data-Retention/Read-Disturb Lifetime Prediction & Aftermarket Cell Error Detection & Correction by Neural Network for 3D-TLC NAND Flash Memory, M. Abe, T. Nakamura and K. Takeuchi, Chuo Univ., Japan

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SESSION 17 - Ferroelectric II [Shunju I]

Thursday, June 13, 14:00-15:40

Chairpersons: S. Takagi, The Univ. of Tokyo
K. Benaissa, Texas Instruments

T17-1 - 14:00

Transient Negative Capacitance as Cause of Reverse Drain-Induced Barrier Lowering and Negative Differential Resistance in Ferroelectric FETs, C. Jin, T. Saraya, T. Hiramoto and M. Kobayashi, The Univ. of Tokyo, Japan

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T17-2 - 14:25

A Comprehensive Kinetic Modeling of Polymorphic Phase Distribution of Ferroelectric-Dielectrics and Interfacial Energy Effects on Negative Capacitance FETs, Y.-T. E. Tang*, C.-L. Fan**, Y.-C. Kao**, N. Modolo**, C.-J. Su*, T.-L. Wu**, K.-H. Kao***, P.-J. Wu****, S.-W. Hsiao****, A. Useinov**, P. Su**, W.-F. Wu*, G.-W. Huang*, J.-M. Shieh*, W.-K. Yeh* and Y.-H. Wang***, *Taiwan Semiconductor Research Institute, **National Chiao Tung Univ., ***National Cheng Kung Univ. and ****National Synchrotron Radiation Research Center, Taiwan

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T17-3 - 14:50

Negative Capacitance CMOS Field-Effect Transistors with Non-Hysteretic Steep Sub-60mV/Dec Swing and Defect-Passivated Multidomain Switching, C. Liu*, H.-H. Chen*, C.-C. Hsu*, C. C. Fan*, H.-H. Hsu** and C.-H. Cheng***, *National Chiao Tung Univ., **National Taipei Univ. of Technology and ***National Taiwan Normal Univ., Taiwan

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T17-4 - 15:15

Microscopic Crystal Phase Inspired Modeling of Zr Concentration Effects in Hf_{1-x}Zr_xO₂ Thin Films, A. K. Saha*, B. Grisafe**, S. Datta** and S. Gupta*, *Purdue Univ. and **Univ. of Notre Dame, USA

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SESSION 18 - ReRAM & Selector [Shunju II, III]

Thursday, June 13, 16:00-18:05

Chairpersons: S.-W. Chung, SK Hynix Semiconductor Ltd.
F. Arnaud, ST Microelectronics

T18-1 - 16:00

Non-Volatile RRAM Embedded into 22FFL FinFET Technology, O. Golonzka, U. Arslan, P. Bai, M. Bohr, O. Baykan, Y. Chang, A. Chaudhari, A. Chen, J. Clarke, C. Connor, N. Das, C. English, T. Ghani, F. Hamzaoglu, P. Hentges, P. Jain, C. Jezewski, I. Karpov, H. Kothari, R. Kotlyar, B. Lin, M. Metz, J. O'Donnell, D. Ouellette, J. Park, A. Pirkle, P. Quintero, D. Seghete, M. Sekhar, A. Sen Gupta, M. Seth, N. Strutt, C. Wiegand, H. J. Yoo and K. Fischer, Intel Corp., USA

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T18-2 - 16:25

A 40nm 2Mb ReRAM Macro with 85% Reduction in FORMING Time and 99% Reduction in Page-Write Time Using Auto-FORMING and Auto-Write Schemes, Y.-C. Chiu*, H.-W. Hu*, L.-Y. Lai*, T.-Y. Huang*, H.-Y. Kao*, K.-T. Chang*, M.-S. Ho**, C.-C. Chou***, Y.-D. Chih***, T.-Y. Chang*** and M.-F. Chang*, *National Tsing Hua Univ., **National Chung Hsing Univ. and ***TSMC, Taiwan

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T18-3 - 16:50

Application-Induced Cell Reliability Variability-Aware Approximate Computing in TaO_x-Based ReRAM Data Center Storage for Machine Learning, C. Matsui, S. Fukuyama, A. Hayakawa and K. Takeuchi, Chuo Univ., Japan

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T18-4 - 17:15

Nb_{1-x}O₂ Based Universal Selector with Ultra-High Endurance (>10¹²), High Speed (10ns) and Excellent V_{th} Stability, Q. Luo*, J. Yu*, X. Zhang*, K.-H. Xue**, J.-H. Yuan**, Y. Cheng***, T. Gong*, H. Lv*, X. Xu*, P. Yuan*, J. Yin*, J. Li****, S. Long*, X. Miao**, L. Tai*, Q. Liu* and M. Liu*, *Institute of Microelectronics of the Chinese Academy of Sciences, **Huazhong Univ. of Science and Technology, ***East China Normal Univ., China and ****Univ. of Wisconsin-Madison, USA

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T18-5 - 17:40

Evidence of Filamentary Switching and Relaxation Mechanisms in Ge_xSe_{1-x} OTS Selectors, Z. Chai*, W. Zhang*, R. Degraeve**, S. Clima**, F. Hatem*, J. F. Zhang*, P. Freitas*, J. Marsland*, A. Fantini**, D. Garbin**, L. Goux** and G. Kar**, *Liverpool John Moores Univ., UK and **imec, Belgium

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SESSION 19 - III-V & 2D [Shunju I]

Thursday, June 13, 16:00-17:40

Chairpersons: Y. Shiratori, NTT Corp.
P. Grudowski, NXP

T19-1 - 16:00

GaN HEMTs with Breakdown Voltage of 2200 V Realized on a 200 mm GaN-on-Insulator(GNOI)-on-Si Wafer, Z. LIU*, H. Xie*, K. H. Lee*, C. S. Tan**, G. I. Ng** and E. A. Fitzgerald***, *Singapore-MIT Alliance for Research and Technology (SMART), **Nanyang Technological Univ., Singapore and ***Massachusetts Institute of Technology, USA

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T19-2 - 16:25

First Demonstration of 40-nm Channel Length Top-Gate WS₂ pFET Using Channel Area-Selective CVD Growth Directly on SiO₂/Si Substrate, C. C. Cheng*, Y.-Y. Chung***, M.-Y. Li*, C.-T. Lin***, C.-F. Li***, J.-H. Chen**, T.-Y. Lai**, K.-S. Li**, J.-M. Shieh**, S.-K. Su*, H.-L. Chiang*, T.-C. Chen*, L.-J. Li*, H.-S. Wong* and C.-H. Chien***, *Taiwan Semiconductor Manufacturing Company, Corporation Research, **Taiwan Semiconductor Research Institute, National Applied Research Laboratories and ***Institute of Electronics, National Chiao Tung Univ., Taiwan

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T19-3 - 16:50

Reassessing Ingaas for Logic: Mobility Extraction in Sub-10nm Fin-Width FinFETs, X. Cai*, A. Vardi*, J. Grajal** and J. del Alamo*, *Massachusetts Institute of Technology, USA and **Universidad Politecnica de Madrid, Spain

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T19-4 - 17:15

Monolithic Integration of GaAs/InGaAs Photodetectors for Multicolor Detection, D.-M. Geum*, S. H. Kim***, S. K. Kim**, S. S. Kang****, J. H. Kyhm****, J. D. Song**, W. J. Choi** and E. Yoon*, *Seoul National Univ., **Korea Institute of Science and Technology (KIST), ***KAIST and ****Dongguk Univ., Korea

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