# 2019 IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2019)

Miami, Florida, USA 15 – 17 July 2019



IEEE Catalog Number: ISBN:

CFP19179-POD 978-1-7281-3392-8

## Copyright © 2019 by the Institute of Electrical and Electronics Engineers, Inc. All Rights Reserved

*Copyright and Reprint Permissions*: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

#### \*\*\* This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.

IEEE Catalog Number:	CFP19179-POD
ISBN (Print-On-Demand):	978-1-7281-3392-8
ISBN (Online):	978-1-7281-3391-1
ISSN:	2159-3469

#### Additional Copies of This Publication Are Available From:

Curran Associates, Inc 57 Morehouse Lane Red Hook, NY 12571 USA Phone: (845) 758-0400 Fax: (845) 758-2633 E-mail: curran@proceedings.com Web: www.proceedings.com



### 2019 IEEE Computer Society Annual Symposium on VLSI (ISVLSI) ISVLSI 2019

#### **Table of Contents**

Message from the General Chairs .xx
Message from the Technical Program Chairs .xxi
ISVLSI 2019 Organizing Committee .xxiii
ISVLSI Steering Committee xxv.
Technical Program Committee xxvi

#### Session 01: Digital Circuits and FPGA Based Designs I

#### Session 02: Special Session: FPGA Accelerator Design and Optimization I

Optimization of Convolutional Neural Networks on Resource Constrained Devices .19...... Arish S (Nanyang Technological University), Sharad Sinha (Indian Institute of Technology (IIT) Goa), and Smitha K G (Nanyang Technological University)

When Neural Architecture Search Meets Hardware Implementation: from Hardware Awareness to Co-Design .25 Xinyi Zhang (University of Pittsburgh), Weiwen Jiang (University of Notre Dame), Yiyu Shi (University of Notre Dame), and Jingtong Hu (University of Pittsburgh)

A (	Cost-Effective CNN Accelerator Design with Configurable PU on FPGA .31
	Chi Fung Brian Fong (Hong Kong University of Science and Technology),
	Jiandong Mu (Hong Kong University of Science and Technology), and Wei
	Zhang (Hong Kong University of Science and Technology)

#### Session 03: System Design and Security I

Transient Effect Ring Oscillators Leak Too 37
Ugo Mureddu (Ūniv Lyon, UJM-Saint-Etienne, CNRS, Laboratoire Hubert
Curien UMR 5516), Brice Colombier (Univ Lyon, UJM-Saint-Etienne, CNRS,
Laboratoire Hubert Curien UMR 5516), Nathalie Bochard (Univ Lyon,
UJM-Saint-Etienne, CNRS, Laboratoire Hubert Curien UMR 5516), Lilian
Bossuet (Univ Lyon, UJM-Saint-Etienne, CNRS, Laboratoire Hubert Curien
UMR 5516), and Viktor Fischer (Univ Lyon, UJM-Saint-Etienne, CNRS,
Laboratoire Hubert Curien UMR 5516)
Not All Feed-Forward MUX PUFs Generate Unique Signatures 43
Alex Ayling (University of Illinois), Satya Venkata Sandeep Avvaru
(University of Minnesota), and Keshab Parhi (University of Minnesota)
SPN-DPLIE: Substitution-Permutation Network Based Secure Circuit for Digital PLIE 49

SPN-DPUF: Substitution-Permutation Network Based Secure Circuit for Digital PUF .49...... Johan Marconot (Univ, Grenoble Alpes, CEA, LETI, DSYS,; Univ. Grenoble Alpes, Grenoble INP), David Hely (Univ. Grenoble Alpes, Grenoble INP), and Florian Pebay-Peyroula (Univ, Grenoble Alpes, CEA, LETI)

#### Session 04: Special Session: FPGA Accelerator Design and Optimization II

Area Efficient Box Filter Acceleration by Parallelizing with Optimized Adder Tree .55 Xinzhe Liu (ShanghaiTech University), Fupeng Chen (ShanghaiTech University), and Yajun Ha (ShanghaiTech University)	
Towards Efficient Compact Network Training on Edge-Devices .6.1 Feng Xiong (Tsinghua University), Fengbin Tu (Tsinghua University), Shouyi Yin (Tsinghua University), and Shaojun Wei (Tsinghua University)	
Near-Memory and In-Storage FPGA Acceleration for Emerging Cognitive Computing Workloads Ashutosh Dhar (University of Illinois), Sitao Huang (University of Illinois), Jinjun Xiong (University of Illinois; BM Research), Damir Jamsek (IBM Systems), Bruno Mesnet (IBM Systems), Jian Huang (University of Illinois), Nam Sung Kim (University of Illinois; Samsung), Wen-mei Hwu (University of Illinois), and Deming Chen (University of Illinois)	3 .68

#### Session 05: Computer-Aided Design and Verification I

Formal Verification of Integer Dividers:Division by a Constant .76..... Atif Yasin (University of Massachusetts Amherst), Tiankai Su (University of Massachusetts Amherst), Sébastien Pillement (University of Nantes, France), and Maciej Ciesielski (University of Massachusetts Amherst)

#### Session 06: Special Session: NVM Based Architecture and System I

University)

The Power of Orthogonality .100 Sébastien Ollivier (University of Pittsburgh), Donald Kline Jr. (University of Pittsburgh), Roxy Kawsher (University of South Florida), Rami Melhem (University of Pittsburgh), Sanjukta Banja (University of South Florida), and Alex K. Jones (University of Pittsburgh)	
In-memory AES Implementation for Emerging Non-Volatile Main Memory .103 Mimi Xie (University of Pittsburgh), Yawen Wu (University of Pittsburgh), Zhenge Jia (University of Pittsburgh), and Jingtong Hu (University of Pittsburgh)	
Investigating Fairness in Disaggregated Non-Volatile Memories .104 Vamsee Reddy Kommareddy (University of Central Florida), Clayton Hughes (Sandia National Laboratories), Simon Hammond (Sandia National Laboratories), and Amro Awad (University of Central Florida)	
Pj-AxMTJ: Process-in-memory with Joint Magnetization Switching for Approximate Computing Tunnel Junction .1.11.	in Magnetic
Hao Cai (Southeast University), Honglan Jiang (Institute of Microelectronics, Tsinghua University), Menglin Han (Southeast University), Zhaohao Wang (Beihang University), You Wang (Beihang University), Jun Yang (Southeast University), Jie Han (University of Alberta), Leibo Liu (Institute of Microelectronics, Tsinghua University), and Weisheng Zhao (Beihang University)	

#### Session 07: Computer-Aided Design and Verification II

Dark-Silicon Inspired Energy Efficient Hierarchical TDM NoC .1.16..... Salma Hesham (Ruhr University Bochum, Germany, German University in Cairo, Egypt), Diana Goehringer (Technische Universitaet Dresden, Germany), and Mohamed A. Abd El Ghany (German University in Cairo, Egypt)

Traffic Driven Automated Synthesis of Network-on-Chip from Physically Aware Behavioral Specification.122 Anup Gangwar (Arm, Inc.), Zheng Xu (Arm, Inc.), Nitin Kumar Agarwal (Arm, Inc.), Ravishankar Sreedharan (Arm, Inc.), and Ambica Prasad (Arm, Inc.) Automated Communication and Floorplan-Aware Hardware/Software Co-Design for SoC .128..... Jong Bin Lim (University of Illinois at Urbana-Champaign) and Deming Chen (University of Illinois at Urbana-Champaign)

Computationally Efficient Learning of Quality Controlled Word Embeddings for Natural Language

Processing 134

Mohammed Alawad (Oak Ridge National Laboratory) and Georgia Tourassi (Oak Ridge National Laboratory)

#### Session 08: Circuit, Reliability and Fault Tolerance I

- Formal Hardware Verification of InfoSec Primitives .140. Mohamed Asan Basiri M (IIT KANPUR) and Sandeep K Shukla (IIT Kanpur)
- SRAM On-Chip Monitoring Methodology for Energy Efficient Memory Operation at Near Threshold Voltage 146 Taehwan Kim (Seoul National University, Korea), Kwangok Jeong (Samsung Electronics Co., Ltd.), Taewhan Kim (Seoul National University, Korea), and Kyumyung Choi (Seoul National University, Korea)

Energy and Error Reduction using Variable Bit-width Optimization on Dynamic Fixed Point Format .152...... Mingze Gao (University of Maryland, College Park), Qian Wang (University of Maryland, College Park), and Gang Qu (University of Maryland, College Park)

Machine Learning-Based Processor Adaptability Targeting Energy, Performance, and Reliability .158...... Anderson Luiz Sartor (Carnegie Mellon University (CMU)), Pedro Henrique Exenberger Becker (Universidade Federal do Rio Grande do Sul (UFRGS)), Stephan Wong (Delft University of Technology (TU Delft)), Radu Marculescu (Carnegie Mellon University (CMU)), and Antonio Carlos Schneider Beck (Universidade Federal do Rio Grande do Sul)

#### Session 09: VLSI for Applied and Future Computing Technology I

Energy-Efficient Embedded Inference of SVMs on FPGA .164 Osman Elgawi (Sultan Qaboos University), A. M. Mutawa (Kuwait University), and Afaq Ahmad (Sultan Qaboos University)
A Reconfigurable Layered-Based Bio-Inspired Smart Image Sensor .169 Pankaj Bhowmik (University of Florida), Md Jubaer Hossain Pantho (University of Florida), Sujan Saha (University of Florida), and Christophe Bobda (University of Florida)
An Asynchronous Analog to Digital Converter for Video Camera Applications .1.75 Sunil R. (Vignan's Foundation for Science, Technology & Research, Guntur, A.P., India), Siddharth R.K. (National Institute of Technology Goa, India), Nithin Kumar Y.B. (National Institute of Technology Goa, India), and Vasantha M.H. (National Institute of Technology Goa, India)

Design of Switched-Current Based Low-Power PIM Vision System for IoT Applications .181......
Zheyu Liu (Tsinghua University), Zichen Fan (Tsinghua University), Qi
Wei (Tsinghua University), Xing Wu (East China Normal University), Fei
Qiao (Tsinghua University), Ping Jin (Tsinghua University), Xin-jun
Liu (Tsinghua University), Chengliang Liu (Shanghai Jiao Tong
University), and Huazhong Yang (Tsinghua University)

### Session 10: Special Session: Neuromorphic Computing and Emerging Technologies

IDE Development, Logic Synthesis and Buffer/Splitter Insertion Framework for Adiabatic Ouantum-Flux-Parametron Superconducting Circuits .187..... Ruizhe Cai (Northeastern University), Xiaolong Ma (Northeastern University), Olivia Chen (Yokohama National University), Ao Ren (Northeastern University), Ning Liu (Northeastern University), Nobuyuki Yoshikawa (Yokohama National University), and Yanzhi Wang (Northeastern University) A Framework for the Analysis of Throughput-Constraints of SNNs on Neuromorphic Hardware 193,.... Adarsha Balaji (Drexel University) and Anup Das (Drexel University) Accelerating Deep Neural Networks in Processing-in-Memory Platforms: Analog or Digital Approach? .197.... Shaahin Angizi (University of Central Florida), Zhezhi He (University of Central Florida), Davane Reis (University of Notre Dame), Xiaobo Sharon Hu (University of Notre Dame), Wilman Tsai (TSMC), Shy Jay Lin (TSMC), and Deliang Fan (University of Central Florida) Exploiting Near-Memory Processing Architectures for Bayesian Neural Networks Acceleration .203..... Yinglin Zhao (Beihang University), Jianlei Yang (Beihang University),

Yinglin Zhao (Beihang University), Jianlei Yang (Beihang University),
 Xiaotao Jia (Beihang University), Xueyan Wang (Beihang University),
 Zhaohao Wang (Beihang University), Wang Kang (Beihang University),
 Youguang Zhang (Beihang University), and Weisheng Zhao (Beihang University)

#### **Poster Session**

Variable-Latency Designs .2.18. Ning-Chi Huang (National Chiao Tung University), Yu-Guang Chen (Yuan

Ze University), and Kai-Chiang Wu (National Chiao Tung University)

Improving Logic Optimization in Sequential Circuits using Majority-inverter Graphs .224 Walter Lau Neto (University of Utah), Xifan Tang (University of Utah), Max Austin (University of Utah), Luca Amaru (Synopsys Inc.), and Pierre-Emmanuel Gaillardon (University of Utah)
Design of a CMOS Broadband Transimpedance Amplifier With Floating Active Inductor .230 Xiangyu Chen (Gifu University) and Yasuhiro Takahashi (Gifu University)
Distributed Pulse Rotary Traveling Wave VCO: Architecture and Design .235 Prashansa Mukim (University of California Santa Barbara), Aditya Dalakoti (University of California Santa Barbara), David McCarthy (University of California Santa Barbara), Brandon Pon (University of California Santa Barbara), Carrie Segal (University of California Santa Barbara), Merritt Miller (University of California Santa Barbara), James F. Buckwalter (University of California Santa Barbara), and Forrest Brewer (University of California Santa Barbara)
Test Your Test Programs Pre-Silicon: A Virtual Test Methodology for Industrial Design Flows .241 Sebastian Pointner (Johannes Kepler University), Oliver Frank (Infineon Technologies Austria), Christoph Hazott (Infineon Technologies Austria), and Robert Wille (Johannes Kepler University)
Design of a Safe Convolutional Neural Network Accelerator .2.47. Zheng Xu (University of Texas at Austin) and Jacob Abraham (University of Texas at Austin)
Test Point Insertion Using Artificial Neural Networks .253. Yang Sun (Auburn University) and Spencer Millican (Auburn University)
Evaluation of Compilers Effects on OpenMP Soft Error Resiliency .259 Jonas Gava (UFRGS), Vitor Bandiera (UFRGS), Ricardo Reis (UFRGS), and Luciano Ost (Loughborough University)
A One-Cycle FIFO Buffer for Memory Management Units in Manycore Systems .265 Ann Gordon-Ross (University of Florida), Saleh Abdel-Hafeez (Jordan University of Science and Technology), and Mohamad Hammam Alsafrjalni (University of Miami)
Impact of Autocorrelation on Stochastic Circuit Accuracy .271 <i>Timothy Baker (University of Michigan) and John Hayes (University of Michigan)</i>
A Novel Single/Double Precision Normalized IEEE 754 Floating-Point Adder/Subtracter .278 Brett Mathis (Oklahoma State University) and James Stine (Oklahoma State University)
Tackling the Drawbacks of a Lagrangian Relaxation Based Discrete Gate Sizing Algorithm .284 Henrique Placido (Universidade Federal do Rio Grande do Sul) and Ricardo Reis (Universidade Federal do Rio Grande do Sul)
A Dual-Band CMOS Low-Noise Amplifier using Memristor-Based Tunable Inductors .290 Nicolas Wainstein (Technion - Israel Institute of Technology), Tamir Tsabari (Technion - Israel Institute of Technology), Yarden Goldin (Technion - Israel Institute of Technology), Eilam Yalon (Technion - Israel Institute of Technology), and Shahar Kvatinsky (Technion - Israel Institute of Technology)

Micro-electrode-dot Array Based Biochips : Advantages of Using Different Shaped CMAs .296 Pampa Howladar (Indian Institute of Engineering Science andTechnology,Shibpur), Pranab Roy (Indian Institute of engineering Science and Technology,Shibpur), and Hafizur Rahaman (Indian Institute of Engineering Science and Technology,Shibpur)
An Improved Automatic Hardware Trojan Generation Platform .302 Shichao Yu (Queen's University Belfast), Weiqiang Liu (Nanjing University of Aeronautics and Astronautics), and Maire O'Neill (Queen's University Belfast)
TrustFlow: A Trusted Memory Support for Data Flow Integrity .308 Cyril Bresch (Univ. Grenoble Alpes, Grenoble INP, LCIS), David Hély (Univ. Grenoble Alpes, Grenoble INP, LCIS), Stéphanie Chollet (Univ. Grenoble Alpes, Grenoble INP, LCIS), and Ioannis Parissis (Univ. Grenoble Alpes, Grenoble INP, LCIS)
Enabling Microarchitectural Randomization in Serialized AES Implementations to Mitigate Side Channel Susceptibility .3.14
Securing a Wireless Network-on-Chip Against Jamming Based Denial-of-Service Attacks .320 Abhishek Vashist (Rochester Institute of Technology), Andrew Keats (Rochester Institute of Technology), Sai Manoj Pudukotai Dinakarrao (George Mason University), and Amlan Ganguly (Rochester Institute of Technology)
FAST: A Frequency-Aware Skewed Merkle Tree for FPGA-Secured Embedded Systems .326 Yu Zou (University of Central Florida) and Mingjie Lin (University of Central Florida)
Defense-Net: Defend Against a Wide Range of Adversarial Attacks through Adversarial Detector .332 Adnan Siraj Rakin (University of Central Florida) and Deliang Fan (University of Central Florida)
Deep State Encryption for Sequential Logic Circuits .338 Yasaswy Kasarabada (University of Cincinnati), Sudheer Ram Thulasi Raman (University of Cincinnati), and Ranga Vemuri (University of Cincinnati)

### **Student Research Forum**

A Multi-Phase Time-to-Digital Converter Differential Vernier Ring Oscillato <u>344</u> annagrebah amina (Lyon Institute of Nuclear Physics), E. Bechetoille
(Lyon Institute of Nuclear Physics), I.B. Laktineh (Lyon Institute of
Nuclear Physics), H. Chanal (Lyon Institute of Nuclear Physics), P.
Russo (Lyon Institute of Nuclear Physics), and H. Mathez (Lyon
Institute of Nuclear Physics)
ASSET: Architectures for Smart Security of Non-Volatile Memories .348 Shivam Swami (University of Pittsburgh) and Kartik Mohanram (University of Pittsburgh)
IRC Cross-Layer Design Exploration of Intermittent Robust Computation Units for IoTs .354 Arman Roohi (University of Central Florida) and Ronald F. DeMara
(University of Central Florida)

Design of Quantum Circuits for Cryptanalysis and Image Processing Applications .360 Edgard Muñoz-Coreas (University of Kentucky) and Himanshu Thapliyal (University of Kentucky)
Effect of Loop Positions on Reliability and Attack Resistance of Feed-Forward PUFs .366 Satya Venkata Sandeep Avvaru (University of Minnesota) and Keshab Parhi (University of Minnesota)
A Case Study On Approximate FPGA Design With an Open-Source Image Processing Platform .3.72 Yunxiang Zhang (University of Houston Clear Lake), Xiaokun Yang (University of Houston Clear Lake), Lei Wu (Auburn University at Montgomery), and Jean Andrian (Florida International University)
Real-Time Automatic Music Transcription (AMT) with Zync FPGA .3.78 Kevin Vaca (University of Houston Clear Lake), Archit Gajjar (University of Houston Clear Lake), and Xiaokun Yang (University of Houston Clear Lake)

#### Session 11: Digital Circuit and FPGA Based Designs II

An Approximate Multiply-Accumulate Unit with Low Power and Reduced Are	a .385
Tongxin Yang (Logic Research Co., Ltd.), Toshinori Sato (Fukuoka	
University), and Tomoaki Ukezono (Tomoaki Ukezono)	

A Low-Power Recurrence-Based Radix 4 Divider Using Signed-Digit Addition .391..... Matthew Gaalswyk (Oklahoma State University) and James Stine (Oklahoma State University)

Towards Data-Driven Approximate Circuit Design .397. Ling Qiu (Clemson University), Ziji Zhang (University of Electronic Science and Technology of China), Jon Calhoun (Clemson University), and Yingjie Lao (Clemson University)

### Session 12: Special Session: Explorations in Energy-Efficient Computing for IoT Applications I

University)

Approximate Energy Recovery 4-2 Compressor for Low-Power Sub-GHz IoT Applications .4.14...... Himanshu Thapliyal (University of Kentucky) and Zachary Kahleifeh (University of Kentucky)

#### Session 13: Emerging and Post-CMOS Technologies I

Routing Performance Optimization for Homogeneous Droplets on MEDA-based Digital Microfluidic Biochips .419. Sarit Chakraborty (Government College of Engineering and Leather Technology, Kolkata, India) and Susanta Chakraborty (IIEST, Shibpur)
Time-Constrained Sample Preparation Algorithm for Reactant Minimization on Digital Microfluidic
Biochips .425.
Ling-Yen Song (National Chiao Tung University, Taiwan), Yu-Ying Li
(National Chiao Tung University, Taiwan), Yung-Chun Lei (National
Chiao Tung University, Taiwan), and Juinn-Dar Huang (National Chiao
Tung University, Taiwan)
Logic Synthesis for Hybrid CMOS-ReRAM Sequential Circuits .431.
Saman Fröhlich (University of Bremen, Germany), Saeideh Shirinzadeh
(University of Bremen, Germany), and Rolf Drechsler (University of
Bremen, Germany)

## Session 14: Special Session: Explorations in Energy-Efficient Computing for IoT Applications II

Ferroelectric FET Based TCAM Designs for Energy Efficient Computing .437
Xunzhao Yin (University of Notre Dame), Dayane Reis (University of
Notre Dame), Michael Niemier (University of Notre Dame), and Xiaobo
Sharon Hu (University of Notre Dame)
Post-Layout Simulation of Quasi-Adiabatic Logic Based Physical Unclonable Function .443
Yasuhiro Takahashi (Gifu University), Hiroki Koyasu (Gifu University),

S. Dinesh Kumar (University of Kentucky), and Himanshu Thapliyal (University of Kentucky)

A 1.8mW Perception Chip with Near-Sensor Processing Scheme for Low-Power AIoT Applications .447...... Zheyu Liu (Tsinghua University), Erxiang Ren (Beijing Jiaotong University), Li Luo (Beijing Jiaotong University), Qi Wei (Tsinghua University), Xing Wu (East China Normal University), Xueqing Li (Tsinghua University), Fei Qiao (Tsinghua University), Xin-Jun Liu (Tsinghua University), and Huazhong Yang (Tsinghua University)

#### Session 15: VLSI for Applied and Future Computing Technology II

Linear Optimization for Memristive Device in Neuromorphic Hardware 453
Jingyan Fu (North Dakota State University), Zhiheng Liao (North Dakota
State University), Na Gong (University of South Alabama), and Jinhui
Wang (University of South Alabama)
Neuromorphic Image Sensor Design with Region-Aware Processing .459.
Md Jubaer Hossain Pantho (University of Florida), Pankaj Bhowmik
(University of Florida), and Christophe Bobda (University of Florida)

CSrram: Area-Efficient Low-Power Ex-Situ Training Framework for Memristive Neuromorphic Circuits Based on Clustered Sparsity .465...... Arash Fayyazi (University of Southern California), Souvik Kundu (University of Southern California), Shahin Nazarian (University of

Southern California), Peter A. Beerel (University of Southern

California), and Massoud Pedram (University of Southern California)

#### Session 16: System Design and Security II

Security in Many-Core SoCs Leveraged by Opaque Secure Zones .471 Luciano Caimi (UFFS) and Fernando Gehm Moraes (PUCRS)
CAESAR-MPSoC: Dynamic and Efficient MPSoC Security Zones .4.77 Siavoosh Payandeh Azad (Tallinn University of Technology), Gert Jervan (Tallinn University of Technology), Michael Tempelmeier (Technical University of Munich), and Johanna Sepúlveda (Technical University of Munich)
Modeling Hardware Trojans in 3D ICs .483. Zhiming Zhang (University of New Hampshire) and Qiaoyan Yu (University of New Hampshire)

#### Session 17: Circuit, Reliability and Fault Tolerance II

A Low-Complexity RS Decoder for Triple-Error-Correcting RS Codes .489..... Zengchao Yan (Nanjing University), Jun Lin (Nanjing University), and Zhongfeng Wang (Nanjing University)

Optimization of Comparator Selection Algorithm for TIQ Flash ADC Using Dynamic Programming Approach ..... 495

Ali Ozdemir (Pennsylvania State University), Mshabab Alrizah (Pennsylvania State University), and Kyusun Choi (Pennsylvania State University)

TSV-IaS: Analytic Analysis and Low-Cost Non-Preemptive on-Line Detection and Correction Method for

TSV Defects .501..... Khanh Dang (Vietnam National University Hanoi), Akram Ben Ahmed (Keio University, Japan), Abderazek Ben Abdallah (The University of Aizu, Japan), and Xuan-Tu Tran (Vietnam National University Hanoi)

Energy-efficient Analog Processing Architecture for Direction of Arrival with Microphone Array .507..... *Changlu Liu (Tsinghua University), Tianxiang Lan (Beijing Institute of Technology), Qin Li (Tsinghua University), Kaige Jia (Tsinghua University), Yidian Fan (Beihang University), Xing Wu (East China Normal University), Fei Qiao (Tsinghua University), Wei Qi (Tsinghua University), Xin-Jun Liu (Tsinghua University), and Huazhong Yang (Tsinghua University)* 

#### Session 18: Special Session: Emerging Technologies and Architectures

Ensan (Pennsylvania State University), Swagata Mandal (Jalpaiguri Government Engineering College), Swaroop Ghosh (Pennsylvania State University), and Anupam Chattopadhyay (Nanyang Technological University)
Accelerating Compact Convolutional Neural Networks with Multi-threaded Data Streaming .5.19 Weiguang Chen (Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, Shenzhen, China, University of Chinese Academy of Sciences, China), Zheng Wang (Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, Shenzhen, China), Shanliao Li (Guilin University of Electronic Technology, Guilin, China), Zhibin Yu (Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, Shenzhen, China), and Huijuan Li (Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, Shenzhen, China)
Design of a Hierarchical Clos-Benes Optical Network-on-Chip Architecture .523 Renjie Yao (Shanghai Jiao Tong University), Yaoyao Ye (Shanghai Jiao Tong University), and Weichen Liu (Nanyang Technological University, Singapore)
Machine Learning-based Prediction for Phase-Based Dynamic Architectural Specialization .529 Ruben Vazquez (University of Florida), Islam Badreldin (University of Florida), Mohamad Hammam Alsafrjalani (University of Miami), and Ann Gordon-Ross (University of Florida)

#### Session 19: System Design and Security III

Hybrid Memristor-CMOS Obfuscation Against Untrusted Foundries 535 Amin Rezaei (Northwestern University), Jie Gu (Northwestern University), and Hi Zhou (Northwestern University)
Memory Locking: An Automated Approach to Processor Design Obfuscation .541 Michael Zuzak (University of Maryland, College Park) and Ankur Srivastava (University of Maryland, College Park)
Hardware-Software Co-Design Based Obfuscation of Hardware Accelerators .547 Abhishek Chakraborty (University of Maryland College Park) and Ankur Srivastava (University of Maryland College Park)

#### Session 20: Special Session: Energy-Efficient Machine Learning

Deep Learning for Edge Computing: Current Trends, Cross-Layer Optimizations, and Open Research Challenges .553..... Alberto Marchisio (Technische Universität Wien (TU Wien)), Muhammad Abdullah Hanif (Technische Universität Wien (TU Wien)), Faiq Khalid (Technische Universität Wien (TU Wien)), George Plastiras (University of Cyprus (UCY)), Christos Kyrkou (University of Cyprus (UCY)), Theocharis Theocharides (University of Cyprus (UCY)), and Muhammad Shafique (Technische Universität Wien (TU Wien)) Approximate Computing Applied to Bacterial Genome Identification using Self-Organizing Maps .560......
Dimitrios Stathis (KTH Royal Institute of Technology, Sweden), Yu Yang
(KTH Royal Institute of Technology, Sweden), Saurabh Tewari (IIT
Delhi, India), Ahmed Hemani (KTH Royal Institute of Technology,
Sweden), Kolin Paul (IIT Delhi, India and TalTech Tallinn University
of Technology, Estonia), Manfred Grabherr (Uppsala University,
Sweden), and Rafi Ahmad (Inland University of Norway)

Towards Efficient On-Board Deployment of DNNs on Intelligent Autonomous Systems .568..... Alexandros Kouris (Imperial College London, UK), Stylianos I. Venieris (Samsung AI Center, Cambridge, UK), and Christos-Savvas Bouganis (Imperial College London, UK)

#### Session 21: Digital Circuits and FPGA Based Designs III

PVTMC: An All-Digital Sub-Picosec	ond Timing Measurement Circuit Based on Process Variations .574
Shuo Li (UMass Amherst), Xiaoli	n Xu (University of Illinois at
Chicago), and Wayne Burleson (U	Umass Amherst)

Hardware Implementation of Improved Fast-SSC-Flip Decoder for Polar Codes .580..... Jing Zeng (Nanjing University), Yangcan Zhou (Nanjing University), Jun Lin (Nanjing University), and Zhongfeng Wang (Nanjing University)

A Comparison-free Hardware Sorting Engine .586..... Surajeet Ghosh (Indian Institute of Engineering Science & Technology, India), Shaon Dasgupta (Bentley Systems India Private Limited, Kolkata), and Sanchita Saha Ray (St. Thomas' College of Engineering & Technology, India)

### Session 22: Special Session: Botnet of Things: Hardware Insecurity in the IoT Era

Persistently-Secure Processors: Challenges and Opportunities for Securing Non-Volatile Memories .6.10...... Amro Awad (University of Central Florida), Suboh Suboh (University of Central Florida), Mao Ye (University of Central Florida), Kazi Abu Zubair (University of Central Florida), and Mazen Al-Wadi (University of Central Florida)

Adaptive Transceiver for Wireless NoC to Enhance Multicast/Unicast Communication Scenarios .592...... Joel Ortiz Sosa (University of Rennes 1, Inria), Olivier Sentieys (University of Rennes 1, Inria), and Christian Roland (University of Southern Brittany, Lab-STICC)

#### Session 23: Digital Circuits and FPGA Based Designs IV

Focus on What is Needed: Area and Power Efficient FPGAs Using Turn-Restricted Switch Boxes .6.15...... Fatemeh Serajeh-hassani (Sharif University of Technology), Mohammad Sadrosadati (Sharif University of Technology), Sebastian Pointner (Johannes Kepler University), Robert Wille (Johannes Kepler University), and Hamid Sarbazi-azad (Sharif University of Technology)

Using Harmonized Parabolic Synthesis to Implement a Single-Precision Floating-Point Square Root Unit.621.. Süleyman Savas (Halmstad University, Sweden), Yassin Atwa (Halmstad University, Sweden), Tomas Nordström (Halmstad University, Sweden), and Zain Ul-Abdin (Halmstad University, Sweden)

Self Timed SRAM Array with Enhanced low Voltage Read and Write Capability .627..... Prasad Vernekar (National Institute of Technology Goa, India), Nithin Kumar Y.B (National Institute of Technology Goa, India), and Vasantha M.H (National Institute of Technology Goa, India)

#### Session 24: Special Session: Secure, Smart, Connected Devices for Emergent Applications

Session 25: Emerging and Post-CMOS Technologies II

A Hyper-Parameter Based Margin Calculation Algorithm for Single Flux Quantum Logic Cells .645..... Soheil Nazar Shahsavani (University of Southern California) and Massoud Pedram (University of Southern California)

Ignore Clocking Constraints: An Alternative Physical Design Methodology for Field-Coupled

Nanotechnologies .651.....

Robert Wille (Johannes Kepler University Linz), Marcel Walter (University of Bremen), Frank Sill Torres (DFKI), Daniel Große

(University of Bremen), and Rolf Drechsler (DFKI GmbH Bremen)

#### Session 26: System Design and Security IV

Mitigating Reverse Engineering Attacks on Deep Neural Networks .657..... Yuntao Liu (University of Maryland, College Park), Dana Dachman-Soled (University of Maryland, College Park), and Ankur Srivastava (University of Maryland, College Park)

Hardware Watermarking Using Polymorphic Inverter Designs Based On Reconfigurable Nanotechnologies .663
Shubham Rai (Technische Universitaet Dresden), Ansh Rupani (Technische
Universitaet Dresden), Pallab Nath (Indian Institute of Technology
Indore), and Akash Kumar (Technische Universitaet Dresden)
Machine Learning Based IoT Edge Node Security Attack and Countermeasures .670
Vishalini Laguduva (University of South Florida), Sheikh Ariful Islam
(University of South Florida), Sathyanarayanan Aakur (University of
South Florida), Srinivas Katkoori (University of South Florida), and
Robert Karam (University of South Florida)

Author Index 67.7.