

# **5th Annual World Conference of the Society for Industrial and Systems Engineering (SISE 2016)**

San Francisco, California, USA  
13 - 14 October 2016

## **Editors:**

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## SISE 2016 BREAKOUT SESSIONS – Thursday October 13, 2016

<b>1.</b>	<b>Session: Manufacturing &amp; Production Planning - I</b> <b>Room: Ballroom I</b>	<b>Time: 2:45 pm - 4:00 pm</b> <b>Chair: TK Baradhan</b>
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SISE 2016 Dinner Banquet and Speech	
Time:	6:30 pm – 8:30 pm
Venue:	Ballroom III
Speech Title:	<b>"Industrial &amp; Systems Engineering Tools Utilized to Address Challenges in High Density Memory Module Process Development"</b>
Speaker:	<b>Satya Iyer, PhD</b> Sr. Director, SMART Modular Technologies, USA
<p>Satya Iyer is a Sr. Director of New Product Introduction, Test &amp; Engineering Design Services at SMART Modular Technologies. Satya has over 15 years of engineering and management experience and leads a cross-functional engineering team of over 25 engineers, including engineering managers &amp; individual contributors focusing in the areas of NPI, process engineering, PCB design, mechanical engineering, component engineering, test engineering, design verification testing &amp; engineering services, located across different geographical locations worldwide. Satya holds a PhD in Systems Science with a specialization in Manufacturing Systems from the State University of New York at Binghamton. He also holds a master's degree in Industrial Engineering from the State University of New York at Binghamton, with a specialization in electronics manufacturing and packaging and a bachelor's degree in Mechanical Engineering from Mumbai University.</p>	
<p><b>Abstract:</b> The trend in the electronics industry is toward producing smaller, lighter products that are friendlier, more functional, reliable, and cost effective. The memory module industry is continuously striving for more functionality and superior performance with each new generation of product offering. The growth in demand for memory capacity is surpassing the pace at which memory component manufacturers are able to cost-effectively produce the next generation of monolithic memory devices. This drives the need for utilizing stacked components for memory module assemblies. The introduction of stacked BGA components, which consist of multiple layers of solder balls and is heavier than regular BGA components, requires that the processes used for assembling monolithic components be reviewed and "optimized" to suit its manufacturability and reliability. The key note focuses on some of the challenges associated with development of a stacked BGA component and provides real life examples of Industrial and Systems Engineering tools utilized to address the same.</p>	

## SISE 2016 BREAKOUT SESSIONS – Friday October 14, 2016

<b>5.</b>	<b>Session: Systems Engineering</b> <b>Room: Ballroom I</b>	<b>Time: 9:00am – 10:15am</b> <b>Chair: DL Santos</b>
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8.	<b>Session: Manufacturing and Production Planning - II</b> <b>Room: Ballroom I</b>	<b>Time: 1:00 pm - 2:15 pm</b> <b>Chair: N Schmeidler</b>
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-O. Mannuss