2021 China Semiconductor Technology International Conference (CSTIC 2021)

Shanghai, China 14 – 15 March 2021



IEEE Catalog Number: CFP2160Y-POD ISBN: 978-1-6654-4946-5

Copyright © 2021 by the Institute of Electrical and Electronics Engineers, Inc. All Rights Reserved

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

*** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.

 IEEE Catalog Number:
 CFP2160Y-POD

 ISBN (Print-On-Demand):
 978-1-6654-4946-5

 ISBN (Online):
 978-1-6654-4945-8

Additional Copies of This Publication Are Available From:

Curran Associates, Inc 57 Morehouse Lane Red Hook, NY 12571 USA Phone: (845) 758-0400

Fax: (845) 758-2633

E-mail: curran@proceedings.com Web: www.proceedings.com



Table of Contents

Preface

Chapter I - Device Engineering and Memory Technology

CMOS Device Design with Ferroelectric Materials1 Changhwan Shin Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon, Korea	1-56
Si/Sn ₂ Vertical Heterojunction Tunneling Transistor with Ionic-Liquid Gate for Ultra-Low Power Applications3 Liang Chen, Rundong Jia, Qianqian Huang and Ru Huang Key Laboratory of Microelectronic Devices and Circuits (MOE), Institute of Microelectronics, Peking University, Beijing, China	1-43
Light-Modulated Subthreshold Swing Effect in a MoS ₂ -Si Hetero MOSFET6 Yingxin Chen ¹ , Jianan Deng ¹ , Qianqian Huang ² , Wenzhong Bao ¹ and Jing Wan ¹ ¹ State key laboratory of ASIC and System, Fudan University, Shanghai, China ² Key Laboratory of Microelectronic Devices and Circuits (MOE), Institute of Microelectronics, Peking University, Beijing, China	1-45
Smart Manufacturing for Si, SiC, and GaN Power Devices in AI Era9 Min-hwa Chi ^{1,2} ¹ SiEn (Qindao) Integrated Circuits Cor., Shandong, China ² Micro-Nano Technology College, Qindao University, Qindao, Shandong, China	1-5
Interconnect-Centric Benchmarking of In-Memory Acceleration for DNNS14 Gokul Krishnan ¹ , Sumit K. Mandal ² , Chaitali Chakrabarti ¹ , Jae-sun Seo ¹ , Umit Y. Ogras ² and Yu Cao ¹ ¹ School of Electrical, Computer, and Energy Engineering, Arizona State University, Tempe, USA ² Department of Electrical and Computer Engineering, University of Wisconsin, Madison, USA	1-54
A Novel Lightweight PUFs Using Interconnect Line Mismatch for Hardware Security18 Ye Lin ¹ , Yuejun Zhang ^{1,2} , Jia Chen ¹ and Jinliang Han ¹ ¹ Faculty of Electronic Engineering and Computer Science, Ningbo University, Ningbo, China ² State Key Laboratory of ASIC and System Fudan University, Shanghai, China	1-41
Frontiers in Low-Frequency Noise Research in Advanced Semiconductor Devices20 Eddy Simoen ^{1,2} , Anabela Veloso ¹ , Barry O'Sullivan ¹ , Kenichiro Takakura ³ and Cor Claeys ⁴ Ilmec, Leuven, Belgium also at Solid-State Sciences Depart., Ghent University, Gent, Belgium National Institute of Technology (KOSEN) Kumamoto-College, Suya, Koshi-City, Japan ESAT-INSYS Depart., KU Leuven, Leuven, Belgium	1-28

Low Frequency Noise Characteristics in 16 nm FinFET Technology24 Gang Wang Rockchip, Shanghai, China	1-3
A Mechanism Study of High-k Dielectric Quality and Metal Gate Al Diffusion Affecting PPU Transistor Threshold Voltage27 Weiwei Ma, Ran Huang, Yamin Cao and Wei Zhou Shanghai Huali Integrated Circuit Corporation, Shanghai, China	1-32
The Systematic Investigation About Al Diffusion and Efficient Improvement on Device Variation and Uniformity Under 28nm HKMG Process30 Zhejun Liu, Liangkai Liu, Yonghua Cui, Ran Huang, Ying Xu and Wei Zhou Shanghai Huali Integrated Circuit Corporation, Shanghai, China	1-39
The Effect of Poly Corner Etch Residue on Advanced FinFET Device Performance33 Qingpeng Wang, Yu De Chen, Cheng Li, Rui Bao, Jacky Huang and Joseph Ervin Coventor Inc., A Lam Research Company, Shanghai, China	1-4
High-k Bubble Defect Researches in Stack-BSI Process Product36 Zhuo Yin ^{1,2} , Jianjun Li ² , Xiaoping Li ² , Na Zhu ² , Lifeng Liu ¹ , Hanming Wu ³ , Dejing Ma ² and Xing Zhang ² ¹ School of Software and Microelectronic, Peking University, Beijing, China ² Semiconductor Manufacturing International Corporation (SMIC), Beijing, China	1-1
Super Junction by Implant Through Trench Contact for Low-Voltage Power MOSFET and IGBT39 Janifer Liu ¹ , P. Li ¹ , R. Qiu ¹ , H. Zhou ¹ , K. Yang ¹ , C. Xu ¹ , E. Wu ¹ , L. Du ¹ , K. Lin ¹ J. Feng ¹ and M. Chi ² ¹ SiEn (Qingdao) Integrated Circuits Cor., Shandong, China ² Micro-Nano Technology College, Qindao University, Qindao, Shandong, China	1-6
Impact of Contact Misalignment on V _T for Trench Power MOSFET42 Perry. Li ¹ , R. Qiu ¹ , H. Zhou ¹ , J. Liu ¹ , K. Yang ¹ , C. Xu ¹ , E. Wu ¹ , L. Du ¹ , K. Lin ¹ , J. Feng ¹ and M. Chi ² ¹ SiEn (Qingdao) Integrated Circuits Cor., Shandong, China ² Micro-Nano Technology College, Qindao University, Qindao, Shandong, China	1-7
Numerical Study of the VDMOS with an Integrated High-k Gate Dielectric and High-k Trench46 Zhenyu Zhang ^{1,2} , Jiafei Yao ^{1,2} , Yufeng Guo ^{1,2} , YongChen He ¹ , JinCheng Liu ¹ , Mingyuan Gu ^{1,2} and Qicong Liang ^{1,2} ¹ The College of Electronic and Optical Engineering & College of Microelectronics, Nanjing University of Posts and Telecommunications, Nanjing, China ² National and Local Joint Engineering Laboratory of RF Integration and Micro-assembly technology, Nanjing, China	1-9
Wafer Edge Crack Defect Investigation and Improvement in 19nm PSZ DEP Process49 Junwei Han, Qiliang Ni, Xiaofang Gu, Jiaya Bo, Jian Li and Pengkai Xu Shanghai Huali Microelectronics Corporation, Shanghai, China	1-10

FinFET GGNMOS DC Parameter Variation Understanding and ESD Performance Improvement Solution by TCAD Simulation52 Hui Shen, YangKui Li and XueJie Shi Semiconductor Manufacturing International (Shanghai) Corporation	1-11
Semiconaucior Managaciaring International (Snanghai) Corporation	
Optimize the Cleaning Process of Tungsten Contact CMP to Avoid Copper Wire Bridges and Improve Product Yield56 Jinfeng Wang, Qiliang Ni , Xiaofang Gu, Guangzhi He, Zhe Wang and Mengyun Cao Shanghai Huali Microelectronics Corporation, Shanghai, China	1-13
FDSOI SIP Epitaxy Optimization for Leakage Reducing60 Jiaqi Hong, Qiang Yan and Jun Tan Shanghai Huali Integrated Circuit Corporation, Shanghai, China	1-14
Etch Back Before ILD-CMP for Improving the Loading Issue After ILD CMP62 Yangyang Dong, Junjie Zhang, Kai Guo, Wei Zhang, Haifeng Zhou, Jingxun Fang and Yu Zhang	1-15
Shanghai Huali Integrated Circuit Corporation, Shanghai, China	
Research and Improvement of Metal Residues in High-k Metal Gate Process Based on CMP Process64	1-16
Qingqing Duan, Junjie Zhang, Qingxuan Hong, Wei Zhang, Haifeng Zhou, Jingxun Fang and Yu Zhang	
Shanghai Huali Microelectronics Corporation, Shanghai, China	
The Effect of Different Well Implant Element on Different Pitch Size CMOS Image Sensor68	1-18
Xiaoyu Li, Qian Wang and Chenchen Qiu Shanghai Huali Microelectronics Corporation, Shanghai, China	
Advanced Manufacturing Process of LCOS Based on Copper Reflector70 Zhao Guo Shanghai Huali Microelectronics Corporation, Shanghai, China	1-19
Single Patterning ILT for Advanced Memory Challenging Design73 Camille Xu, Jingjing Liu, Zhen Shi and Xudong Zhu ChangXin Memory Technologies Inc., Hefei, Anhui, China	1-20
The Comprehensive Solution of Ultra Top Metal Stress Impact on Seal Ring77 Qiang Liu	1-21
Shanghai Huali Microelectronics Corporation, Shanghai, China	
Improved Method to Analysis Doping Profile for Ion Implants in Silicon80 Hui Chen, Xiaoyu Li, Zhengying Wei, Chang Sun, Jiong Xu and Ming Wang Shanghai Huali Microelectronics Corporation, Shanghai, China	1-24
Methods of Reducing Metal Damager Defect in Back End of Line for Semiconductor in 28nm Technology83 Shanshan Chen, Hunglin Chen, Yin Long, Hao Guo and Kai Wang Shanghai Huali Microelectronics Corporation, Shanghai, China	1-25

Influence of Negative DIBL Effect on MOSFET Effective Drive Current and CMOS Circuit86 Weixing Huang ^{1,2} , Huilong Zhu ¹ , Yongkui Zhang ¹ , Zhenhua Wu ¹ , Kunpeng Jia ¹ , Xiaogen Yin ¹ , Yangyang Li, Xuezheng Ai and Qiang Huo ¹ Key Laboratory of Microelectronics Devices and Integrated Technology, Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China ² University of Chinese Academy of Sciences, Beijing, China	1-38
Non-Linear Resistive Switching Characteristics in HfO ₂ -Based RRAM with Low-Dimensional Material Engineered Interface89 Linbo Shan, Zongwei Wang, Lindong Wu, Shengyu Bao, Yi-shao Chen, Kechao Tang, Yimao Cai and Ru Huang Institute of Microelectronics, Peking University, Beijing, China	1-42
A Configurable Computing-in-Memory Structure Based on Convolutional Neural Network92 Jiancheng Yang ^{1,2} , Xiaoxin Cui ^{1,2} , Song Jia ^{1,2} and Yuan Wang ^{1,2} ¹ Key Laboratory of Microelectronic Devices and Circuits (MOE), Institute of Microelectronics Peking University, Beijing, China ² Beijing Laboratory of future IC technology and science, Peking University, Beijing, China	1-44
Engineering of Substrate Oxidation in Deposited SiC Gate Stacks for Improving Interface Performance95 Shuo Liu, Jingquan Liu and Xiuyan Li Department of Micro/Nano Electronics, Shanghai Jiao Tong University, Shanghai, China	1-46
Improvement of RRAM Uniformity and Analog Characteristics Through Localized Metal Doping99 Yabo Qin ¹ , Zongwei Wang ^{1,2} , Qingyu Chen ¹ , Yaotian Ling ¹ , Lindong Wu ¹ , Yimao Cai ^{1,2} and Ru Huang ^{1,2} ¹ Institute of Microelectronics, Peking University, Beijing, China ² Key Laboratory of Microelectronic Devices and Circuits, Peking University, Beijing, China	1-47
Impacts of Ferroelectric Parameters on the Electrical Characteristics of FEFET for Low-Power Logic and Memory Applications102 Kaifeng Wang, Qianqian Huang, Chang Su, Liang Chen, Mengxuan Yang and Ru Huang Key Laboratory of Microelectronic Devices and Circuits (MOE), Institute of Microelectronics, Peking University, Beijing, China	1-49

Chapter II – Lithography and Patterning

Negative-Tone Imaging (NTI) for Advanced Lithography with EUV Exposure to Improve 'Chemical Stochastic'105	2-8
Toru Fujimori	
Electronic Materials Research Laboratories FUJIFILM Corporation Kawashiri,	
Yoshida-cho, Haibara-Gun, Shizuoka, Japan	
High Performance Bulk and POU Filtration of EUV Lithography Materials108 Lucia D'Urzo ¹ , Toru Umeda ² , Takehito Mizuno ² , Atsushi Hattori ³ , Amarnauth Singh ⁴ , Rajan Beera ⁵ , Philippe Foubert ⁶ and Waut Drent ⁶ ¹ Pall Corp., Hoegaarden, Belgium	2-40
² Nihon Pall Ltd, Kasuminosato, Ami-machi, Inashiki-gun, Ibaraki, Japan ³ Nihon Pall Manufacturing Ltd., Kasuminosato, Ami-machi, Inashiki-gun, Ibaraki, Japan ⁴ Pall Corp., Port Washington, NY, USA ⁵ Pall Corp, 1 USA ⁶ imec, Leuven, Belgium	
Development of Planarizing Spin-on Carbon Material for High-Temperature Processes112 Runhui Huang, Xing-Fu Zhong, Jakub Koza, Gu Xu, Boyu Zhang and Sean Simmons <i>Brewer Science, Inc., Rolla, Missouri, USA</i>	2-43
Lithographic Simulator Based on Deep Learning with Graph Input118 Peng Xu, Pengpeng Yuan and Yayi Wei Institute of Microelectronics, Chinese Academy of Science, Beijing, China	2-3
The Setting of Linewidth Reference on Photomasks Through Physical Process Modeling122 Rui Hu and Qiang Wu Shanghai IC R&D Center, Zhangjiang Hi-Tech Park, Shanghai, China	2-28
SEM Image Transformation Between Litho Domain and Etch Domain125 Yan Yan ¹ , Xuelong Shi ¹ , Chen Li ¹ , Bowen Xu ¹ , Yifei Lu ¹ , Ying Gao ¹ , Wenzhan Zhou ² and Kan Zhanghai IC R&D Center, Shanghai, China ² Shanghai Huali Microelectronics Corporation, Shanghai, China	2-31 hou ²
Optical Proximity Correction, Methodology and Limitations127 Yongqiang Hou and Qiang Wu Shanghai IC R&D Center, Zhangjiang Hi-Tech Park, Shanghai, China	2-12
Source and Mask Optimization with Narrow-Band Semi-Implicit Scheme132 Yijiang Shen School of Automation, Guangdong University of Technology, Guangzhou 510006, China	2-2

An Innovative Graphical Platform for Real Time Accurate AEI Overlay Prediction and Rework Control136 Yaobin Feng¹, JianFeng Li¹, Alex Wang¹, Xue Huang¹, Senmao Zeng¹, Nick Lu¹, Dean Wu¹, Pandeng Xuan¹, Yang Kuang³, Ningqi Zhu², Erik Xiao², Mi Zhang², Jin Zhu³, Jason Pei² and Kevin Huang⁴ ¹Yangtze Memory Technologies Co., Ltd. (YMTC), Wuhan, China ²KLA, Zhangjiang High-Tech Park, Shanghai, China ³KLA, Future Technology City, Jiangxia district, Wuhan, China ⁴KLA, Milpitas, California, United States	2-45
The Photoresist Developing Ability Study at Different Contact Angle and Mask Transmission Rate140 Chen Lijun, Zheng Haichang, Wang Xiaolong, Qin Lipeng, Chen Jiawen and Yin Pengteng Shanghai Huali Microelectronics Corporation, Shanghai, China	2-4
The Mechanism Study of Rounded AA Damage Defect After POLY Loop143 Zheng Haichang, Chen Lijun, Wang Xiaolong, Zhang Yu, Zhu Xiaobin and Zhang Chi Shanghai Huali Microelectronics Corporation	2-5
Aberration Analysis and Control Based on Fully Connected Neural Network146 Shuang Zhang ^{1,2} , Tianyang Gai ^{1,2} , Libin Zhang ² , Pengzheng Gao ^{1,2} , Jianfang He ² And Yayi Wei ^{1,2} ¹ University Of Chinese Academy Of Sciences (UCAS), Beijing, China ² Institute Of Microelectronics, Chinese Academy Of Sciences, Beijing, China	2-33
Mining Lithography Hotspots from Massive SEM Images Using Machine Learning Model149 Tao Zhou ¹ , Bowen Xu ¹ , Chen Li ¹ , Xuling Diao ¹ , Yan Yan ¹ , Shoumian Chen ¹ , Yuhan Zhao ¹ , Kan Zhou ² , Wenzhan Zhou ² , Xuan Zeng ³ and Xuelong Shi ¹ Ishanghai Integrated Circuits R&D Center Co., Ltd., Shanghai, China Shanghai Huali Microelectronics Corporation, Shanghai, China state Key Lab Of Asic & System, School Of Microelectronics, Fudan University, Shanghai, China	2-34
Chapter III – Dry & Wet Etch and Cleaning	
Deep and Vertical Polyimide Etching152 Yuwei Kong, Yuanwei Lin and Zihan Dong Depart. Semiconductor Etching, NAURA Technology Group Co., Ltd., Beijing, China	3-12
Tunable Step Coverage of In-Situ PE-ALD in Etch Chamber for Sidewall Protection During 3D NAND High Aspect-Ratio Etch155 Jingdong Yan, Bosen Ma, Stephen Liou, Ce Qin and Amit Jain Lam Research Service Co., Ltd. F11, Future Technology Building, Wuhan, China	3-2
Release Process Development for MEMS Micro-Bridge Structure158 Bo Zhang ¹ , Xiaoxu Kang ² and Xiaolan Zhong ²	3-15
Shanghai Huahong Grace Semiconductor Manufacturing Corporation, Shanghai, China	
Process Technology Department, Shanghai IC R&D Center, Shanghai, China	

Simulation-Assisted Ion Angle Tuning in High Aspect-Ratio (HAR) Etch for Wafer Edge Bottom Etch Enhancement161 Jingdong Yan, Run Zhang and Zhijie Hao Lam Research Service Co, Wuhan, China	3-3
A Study of Inter-Via CD and PEB Amount Correlation in Dual Damascene Process164 Xinruo Su, XueBing Zhao, Yuan Li and Jun Wang Semiconductor Manufacturing North China Corporation, Beijing, China	3-18
Manufacturing Process Optimization of Polycrystalline Aluminum and Aluminum Alloy on SiO ₂ /Si167 Ping Linda Zhang ¹ , Ping Huang ² , Zhongyuan Jin ² and C.C. Han ³ ¹ Richmond Star High-Tech Consulting, Richmond, BC, Canada ² Shanghai SIM-BCD semiconductor Co. Ltd., Shanghai, China ³ TDK Headway Technologies Inc., Milpitas, California, USA	3-34
The Etching Morphology of Silver Study by Inductively Coupled Ar-Based Plasmas170 Qingqing Lian, Ruiping Zhu, Wang Jing, Hailong Liu and Zhongwei Jiang NAURA Microelectronics Equipment CO., Ltd, Beijing, China	3-43
The Improvement of Resistance Al-Cu Alloy Cl-Corrosion Resistance173 Shifeng Zou, Chengjie Wang, Jun Liu and Yun Xu Shanghai Huahong Grace Semiconductor Manufacturing Corporation, China	3-1
Study on Low Power Back-Side Deep Trench Isolation Etching on Stack-BSI CMOS Image Sensor176 Zhuo Yin ¹² , Jianjun Li ² , Xinruo Su ² , Dejing Ma ² , Hanming Wu ³ and Xing Zhang ² ¹ School of Software and Microelectronic, Peking University, Beijing, China ² Semiconductor Manufacturing International Corporation (SMIC), Beijing, China ³ School of Microelectronics, Zhejiang University, Hangzhou, China	3-13
Exploring Gate-Cut Patterning Approaches Using Simulation and Defect Modelling179 Sun Li Fei, Wang Qing Peng, Zhang Ji Hong and Chi Yu Shan Lam Research Service Co., Ltd., Shanghai, China	3-24
HNA Wet Etching Optimization in Wafer Thinning of BSI Process183 Pengfei Lyu ¹ , Mingyuan Xiang ¹ , Jia Xu ¹ , Tianhao Zhang ¹ , Quan Zhang ² and Qingpeng Zhao ² 'Lam Research Service Co., Ltd, Shanghai, China 'Shanghai Huali Microelectronics Corporation, Shanghai, China	3-25
Si ₃ N ₄ Plasma Etch Study for Optimized Morphology Performance187 Quanbao Li, Xiaohui Ren, Jihong Zhang and Yushan Chi Lam Research Service Co., Ltd, Shanghai, China	3-29

Silicon Wafer Uniformity and Roughness Control by Spin Etch D and Spin Etch E on Wafer Thinning191 PinChang Li ¹ , GuoMing Lin ¹ and SiYang Long ² 'Lam Research Service Co., Ltd, Shanghai, China ² CanSemi, Guangdong, China	3-32
Peeling Defect Studying with N ₂ /H ₂ Plasma during Carbon-based Recess Etch194 Jinrong Wu ¹ , Junwen Huang ¹ , Taojun Zhuang ¹ , Weijun Luo ¹ , Victor Fang ¹ , Chris Lansford ¹ , Yun Chen ² , Martin Liu ² and Scott Shao ² 'Lam Research Corporation, Wuhan, Hubei Province, China 'Yangtze Memory Technologies Co., Ltd, Wuhan, Hubei Province, China	3-40
Chapter IV – Thin Film, Plating and Process Integration	
Improvement of Fin Bridge Defect for FinFETs Technology197 Junhong Zhao, Hai Zhao and Jiwei Zhang Semiconductor Manufacturing International Corp., Shanghai, China	4-1
Mechanism of Reverse Leakage Current in Schottky Diodes Involving Velocity Overshoot201 W.S. Lau Nanyang Technological University (Retired), School of EEE, Singapore	4-34
Improvement of Wafer Edge Defect For FinFETs Technology203 Junhong Zhao, Hai Zhao and Jiwei Zhang Semiconductor Manufacturing International Corp., Shanghai, China	4-12
STI Gap-Fill Technology and Flowable CVD Process Application208 Yan.Sun and SiMeng.Wei Beijing NAURA Microelectronics Equipment Co., Beijing, Chin	4-42
Investigation of Physical Properties and Thermal Stability of Ultra- Thin TiN/HfO ₂ Film Stack Prepared By Atomic Layer Deposition210 Yiqun Liu, Qingqing Wu, Xiang Lv, Gang Chen and Jianjun Zhu Shanghai IC R&D Center, Zhangjiang Hi-Tech Park, Shanghai, China	4-4
Mechanism B I-V Symmetry for MIM Capacitors Used in Microelectronics213 W.S. Lau Nanyang Technological University (Retired), School of EEE, Singapore	4-33
Optimization of Selective Inhibition for Void-Suppressed Tungsten Gap-fill215 Xin Gan Lam Research (Shanghai) Co., Ltd. Wuhan Branch, Wuhan, China	4-9
Machine Learning Assisted In-situ Sensing and Detection on System of PECVD Depositing Hydrogenated Silicon Films217 Zong-Wei Shang ¹ , Qian Yu-Pu Yang ¹ , Hsiao-Han Lo ¹ , Wei-Lun Chen ¹ , Song-Ho Wang ¹ , Te-yun Lu ¹ , Hsueh-Er Chang ¹ , Peter J. Wang ² , Walter Lai ² , Yiin-kuen Fuh ¹ and Tomi T. Li ¹	4-13

Department of Mechanical Engineering, National Central University, Taoyuan City, Taiwan, China Delta Electronics, Inc., Taoyuan City, Taiwan, China	
Investigation on Channel Plasma Effect in Doped Tin-Oxide Thin-Film Transistors Using Experiments and Simulation221 Zong-Wei Shang ¹ , Qian Xu ¹ , Guan-You He ¹ , Zhi-Wei Zheng ¹ and Chun-Hu Cheng ² School of Electronic Science and Engineering, Xiamen University, Xiamen, China Dept. of Mechatronic Engineering, National Taiwan Normal University, Taipei, Taiwan, China	4-2
Optimization of SiGe Selective Epitaxial Growth for Advanced FDSOI Technology224 Yongyue Chen, Jun Tan and Haifeng Zhou Research and Development Dept., Shanghai Huali Integrated Circuit Corporation, Shanghai, China	4-11
Influence of Different Pressures on Characteristics of Plasmas in PECVD Chamber226 Xingyu Li ¹ , Yongjie Hu ¹ , Jie Yuan ¹ , Lulu Guan ¹ , Xiaobo Liu ² , Dongdong Hu ² , Lu Chen ² , Kaidong Xu ^{1,2} and Shiwei Zhuang ¹ School of Physics and Electronic Engineering, Jiangsu Normal University, Xuzhou, China Jiangsu Leuven Instruments Co. Ltd, Xuzhou, China	5 4-29
Investigation of the Optical Properties of a-Si:H films Deposited by PECVD Using Various Experimental Techniques228 Yudong Zhang ^{1,2} , Xingyu Li ^{1,2} , Jiale Tang ^{1,2} , Yongjie Hu ^{1,2} , Jie Yuan ^{1,2} , Lulu Guan ^{1,2} , Hushan Cui ² , Guanghui Ding ² , Xinying Shi ¹ , Kaidong Xu ^{1,2} and Shiwei Zhuang ¹ School of Physics and Electronic Engineering, Jiangsu Normal University, Xuzhou, China Jiangsu Leuven Instruments Co. Ltd, Xuzhou, China	4-31
Chapter V – CMP and Post-Polish Cleaning	
Copper Corrosion Issue Analysis and Study on Advanced CMP Process230 Lei Zhang, Yuanyuan Meng, Yi Xian, Wei Zhang, Haifeng Zhou, Jingxun Fang and Yu Zhang Shanghai Huali Integrated Circuit Corporation, Shanghai, China	5-13
Effect of Oxone and Peroxodisulphates on the Chemical Mechanical Polishing Efficiency of C-Plane GaN233 Yebo Zhu ^{1,2} , Xinhuan Niu ^{1,2} , Ziyang Hou ^{1,2} , Yinchan Zhang ^{1,2} and Yanan Lu ^{1,2} 'School of Electronics and Information Engineering, Hebei University of Technology, Tianjin, China 'Tianjin Key Laboratory of Electronic Materials and Devices, Tianjin, China	5-23
Preparation of ZnO Doped SiO ₂ Abrasive and Chemical Mechanical Polishing Performance on C-Plane Sapphire Substrate236	5-24

Ziyang Hou ^{1,2} , Xinhuan Niu ^{1,2} , Yanan Lu ^{1,2} , Yinchan Zhang ^{1,2} , Yebo Zhu ^{1,2} and Yangang He ^{1,2}	
1 School of Electronics and Information Engineering, Hebei University of Technology Tianjin, China	
2 Tianjin Key Laboratory of Electronic Materials and Devices, Tianjin, China	
Analysis of Main Physical Factors of Chemical Mechanical Polishing About Lithium Tantalate239	5-38
Ye Li ^{1,2} , Baoguo Zhang ^{1,2} , Haoran Li ^{1,2} , Xiaofan Yang ^{1,2} , Wei Wei ^{1,2} and Zhaoxia Yang ^{1,2} 1 School of Electronics and Information Engineering, Hebei University of Technology Tianjin, China	
2 Tianjin Key Laboratory of Electronic Materials and Devices, Tianjin, China	
Effect of FA/O II Surfactant as a Complex Non-Ionic Surfactant on Copper CMP242 Yinchan Zhang ^{1,2} , Xinhuan Niu ^{1,2} , Jiakai Zhou ^{1,2} , Chenghui Yang ^{1,2} , Ziyang Hou ^{1,2} and Yebo Zhu ^{1,2}	5-22
School of Electronics and Information Engineering, Hebei University of Technology Tianjin, China	
2 Tianjin, China 2 Tianjin Key Laboratory of Electronic Materials and Devices, Tianjin, China	
Research on Ultra-Precision Polishing Process of Semiconductor Wafer Surface Based on Disc Hydrodynamic Polishing245 Jiang Xiang-min ¹ , Jiang Xiaoxiong ² , Lin Bin ¹ and Cao zhong-chen ¹	5-28
1 Key Laboratory of Advanced Ceramics and Machining Technology, Ministry of Education, Tianjin University, Tianjin, China	
2 Laboraotory of Science and Technology on Marine Navigation and Control, China State Shipbuilding Corporation, Tianjin, China	
Investigation of Factor Inducing Edge Over Erosion During Chemical Mechanical Polishing248	5-4
Lixiao Wu ¹ , Sookap Hahn ² and Changfeng Yan ¹ 1 School of Mechanical & Electronical Engineering, Lanzhou University of Technology,	
Lanzhou, China, 2 SKW Associates, Santa Clara, CA, USA	
Sub-Nano Depth Scratches on Various Crystal Surfaces During Chemical Mechanical Polishing251	5-35
Xiaolong Han, Zhuji Jin and Ping Zhou Key Laboratory for Precision and Non-traditional Machining Technology of Ministry of Education, Dalian University of Technology, Dalian, China	
Effects of Surfactants on Cu-Co Galvanic Corrosion in Post-CMP Cleaning253 Yazhen Wang ^{1,2} , Baimei Tan ^{1,2} , Shihao Zhang ^{1,2} , Mengrui Liu ^{1,2} and Xiaoqin Sun ^{1,2} I School of Electronic Information Engineering, Hebei University of Technology, Tianjin, China	5-32
2 Tianiin Key Laboratory of Electronic Materials and Devices, Tianiin, China	

Research on Improvement of CMP Thickness Uniformity Control on Wafer Edge Defocus Defects257 Zengyi Yuan, Kai Wang, Hunglin Chen and Yin Long Shanghai Huali Microelectronics Corporation, Shanghai, China	5-15
Study on Dispersion of Nano-Diamond During the Heat Treatment Process262 Song Yuan and Xiaoguang Guo Key Laboratory for Precision and Non-Traditional Machining Technology of Ministry of Education, Dalian University of Technology, Dalian, China	5-17
Development of a Standard Evaluation System to Characterize and Quantify Pad Foam Morphology for Chemical Mechanical Polishing (CMP)265 Qi Zhang¹, Zhenyun Chu² and Zhichao Li³ 1 School of Mechanical Engineering, Yangzhou University, Yangzhou, Jiangsu, China 2 College of Mechanical and Electronic Engineering, Shandong University of Science and Technology, Qingdao, Shandong, China 3 Dept. of Industrial & System Engineering, North Carolina Agricultural & Technology State University, Greensboro, North Carolina, USA	5-19
Chemical Mechanical Polishing of Semiconductor Wafers: Surface Element Modeling and Simulation to Predict Wafer Surface Shape268 Qi Zhang ¹ , Zhen Li ² , Houjun Qi ² and Zhichao Li ³ 1 School of Mechanical Engineering, Yangzhou University, Yangzhou, Jiangsu, China 2 Tianjin Key Lab of High Speed & Precision Machining, Tianjin University of Technology and Education, Tianjin, China 3 Dept. of Industrial & System Engineering, North Carolina A&T State University, Greensboro, North Carolina, USA	5-20
Effect of PASP Inhibitor on Cu-Co Galvanic Corrosion270 Haoran Li ^{1,2} , Baoguo Zhang ^{1,2} , Ye Li ^{1,2} , Xiaofan Yang ^{1,2} , Wei Wei ^{1,2} and Zhaoxia Yang ^{1,2} I School of Electronics and Information Engineering, Hebei University of Technology Tianjin, China ² Tianjin Key Laboratory of Electronic Materials and Devices, Tianjin, China	5-29
Role of 1-H Carboxyl Benzotriazole as Corrosion Inhibitor for Cobalt "Bulk Step" CMP in H ₂ O ₂ Based Alkaline Slurry273 Shuangshuang Lei ¹ , Chenwei Wang ¹ and Shengli Wang ² 1 School of Electronic Information Engineering, Hebei University of Technology, Tianjin, China 2 Tianjin Key Laboratory of Electronic Materials and Devices, Tianjin, China	5-31
Effect of TTA-K as Inhibitor on Cu/Ru/Tan Structure Based Patterned Wafer CMP276 Yuan Tian ^{1,2} , Chenwei Wang ^{1,2} , Jianwei Zhou ² , Chen Xu ^{1,2} , Xue Zhang ^{1,2} and Chao Wang ^{1,2} School of Electronic Information Engineering, Hebei University of Technology, Tianjin, China 2 Tianjin Key Laboratory of Electronic Materials and Devices, Tianjin, China	5-33

Role of FA/O II Complexing Agent and Bit on Dishing and Erosion Reduction During Cu Barrier CMP279 Zhihui Cui, Hongdong Zhao, Yuling Liu and Chenwei Wang ¹ School of Electronic Information Engineering, Heibei University of Technology ² Tianjin Key Laboratory of Electronic Materials and Devices, Tianjin, China	5-34
Investigation on the Material Removal Process of Copper by a Single Pad Asperity281 Haipeng Li, Lin Wang, Ying Yan and Ping Zhou Key Laboratory for Precision and Non-traditional Machining Technology of Ministry of Education, Dalian University of Technology, Dalian, China	5-36
Measurement and Characterization of Surface Roughness of Polishing Pad284 Changyu Hou, Lin Wang, Ying Yan and Ping Zhou Key Laboratory for Precision and Non-traditional Machining Technology of Ministry of Education, Dalian University of Technology, Dalian, China	5-37
Chapter VI – Metrology, Reliability and Testing	
Implementation of Spectral Interferometry for Enhanced Critical Dimensions Optical Metrology287 Dror Shafir, Roy Shtainman and Igor Turovets Nova measuring instruments, Rehovot, Israel	6-41
Advantages of Picosecond Ultrasonic Technology for Advanced RF Metrology290 Johnny Dai ¹ , Johnny Mu ² , Cheolkyu Kim ³ and Priya Mukundhan ¹ 1 Onto Innovation, 550 Clark Drive, Budd Lake, NJ, USA 2 Onto Innovation, Shanghai, China 3 Onto Innovation, Sungnam-si, Gyunggi-do, Korea	6-37
Inline Thickness Measurement for Thick Amorphous Silicon Film by Spectroscopic Ellipsometry Method293 Bo Zhang ¹ , Xiaoxu Kang ² and Guangping Hua ¹ 1 Shanghai Huahong Grace Semiconductor Manufacturing Corporation, Shanghai, China 2 Process Technology Department, Shanghai IC R&D Center, Shanghai, China	6-33
Mask Design Method for Un-Patterned Dark Field Defect Inspection System296 Chao Liu ^{1,2} , Shuang Xu ^{1,2} , Cheng Liao ^{1,2} and Yufei Liu ^{1,2} 1 Key Laboratory of Metallurgical Equipment and Control Technology, Wuhan University of Science and Technology, Wuhan, China 2 Hubei Key Laboratory of Mechanical Transmission and Manufacturing Engineering, Wuhan University of Science and Technology, Wuhan, China	6-40
An Efficient Way of Developing 5G MIMO Transceiver Test on ATE299 Hao Chen, Wensen Lin and Xuequan Chen Advantest (China) Co., Ltd., Shanghai, China	6-5

Complex Protocol Construct System on ATE Platform303 Xin Song and Man Cao Advantest (China) Co., Ltd., Shanghai, China	6-8
Universal Semiconductor ATPG Solutions for ATE Platform Under the Trend of AI and ADAS307 Qimeng Wang, Zhonghe Tian, Xi He, Ziteng Xu, Mingjie Tang, Shenqi Cai and Wei Zong Advantest (China) Co., Ltd., Shanghai, China	6-14
Picosecond Imaging Circuit Analysis of CMOS Circuits Using SIL Measurement310 Shang Chih Lin and Frank Yong Gallant Precision Machining Co., Hsinchu, Taiwan, China	6-9
Backside Defect Monitoring Strategy Aand Improvement in the Advanced Semiconductor Manufacturing314 JianGang Zhou, Hungling Chen, Yin Long, Kai Wang, Hao Guo and Feijue Liu Shanghai Huali Integrated Circuit Manufacturing Co., Ltd, Shanghai, China	6-26
Convolutional Neural Network (CNN) Based Automated Defect Classification (ADC) With Imbalanced Data319 Hairong Lei, Cho Teh, Zhe Wang, Gino Fu, Lingling Pu and Wei Fang ASML, San Jose, California, USA	6-28
A Novel Wafer-Map Similarity Search System with High Speed and Accuracy322 Chang Xu, Qi-Shi Shi and Ping-fen Shi Fujian Jinhua Integrated Circuit Co., Ltd., Jinjiang, Quanzhou, China	6-16
Reliability Challenges and In-line Metrology – An Effective Approach to Implementation in Advanced Devices325 Daniel Fishman ¹ and Sang Hyun Han ² 1 Nova Measuring Instruments, LTD, Rehovot, Israel 2 Nova Measuring Instruments, Inc., Fremont CA, USA	6-42
The Gate Length Dependence of Single Event Upset in 14nm Bulk and SOI FinFET SRAM Cells328 Jingyi Liu ¹ , Xia An ¹ , Gensong Li ¹ , Zhexuan Ren ¹ , Kunlei Gu ² and Ru Huang ¹ 1 Institute of Microelectronics, Peking University, Beijing, China 2 Electronic Information Engineering, Anhui University, Anhui, China	6-32
Board-Level Thermal Cycle Simulation and Improvement of 2.5D Large-Size Package331 Shiyu Chen ² , Dan Yang ² , Na Mei ² , Tuobei Sun ² and Keqing Ouyang ¹ 1 State Key Laboratory of Mobile Network and Mobile Multimedia Technology 2 Department of Packaging and Testing ZTE Corporation, Shen Zhen, China	6-7
Throughput Improvements Via Logistics in Current Semiconductor Factories334 George W Horn and William Podgorski Middlesex Industries SA, Switzerland	6-3

R2R Based Alternating Direction Method of Multi-Parameter Control Strategy336 Huating Huang, Jingwen Ma and Chang Xu Fujian Jinhua Integrated Circuit Co., Ltd., Jinjiang, Quanzhou, China	6-17
A Dynamic Sampling Algorithm Based on Cost-Risk Assessment Model in Semiconductor Manufacturing339 Sen Wang, Shijia Yan, Lei Li, Cong Luo, Juan Ai, Qiang Shen, Desheng Wang, Shenglan Ding and Qing Xia Wuhan Xinxin Semiconductor Manufacturing Co., Ltd.(XMC), Wuhan, Hubei, China	6-25
New Register Configuration Solution for High Speed IO Test343 Tianyu Zhang, Yanfen Fang and Jiaying Xiang Advantest, Shanghai, China	6-1
Effects of Different Gate Stress Conditions on Hot Carrier Injection in High Voltage N-Channel CMOS346	6-2
Lei Li, Sarah Zhou and Kelly Yang Semiconductor Manufacturing International (Shanghai) Corp., Shanghai, China A New Solution of Power Management Integrated Circuit One Time Programable Test349 Yong Liang, L.F. Tao and Colin Xing Global NPI Test Center, NXP Semiconductors (China) Ltd., Tianjin, China	6-4
Investigation Between 2-Terminal and 4-Terminal Kelvin Structure in Terms of WLR IsoEM and PLR EM For Metal Interconnection352 Dingrui Zhang, Weihai Fan, Jizhou Li and Kelly Yang Q&R, Semiconductor Manufacturing International Corporation (SMIC), Shanghai, China	6-6
The Failure Mechanism of Drain Bias TDDB and Characterization of Lifetime Model For HV DePMOS355 Xiumei Song, Weihai Fan, Xiaobo Duan and Qingyuan Qin	6-10
Q&R, Semiconductor Manufacturing International Corporation(SMIC), Shanghai, China	
Electro-Migration Behavior Study on Metal Line Width and Length of AlCu Interconnects358 Jizhou Li, Lei Sun and Weihai Fan Semiconductor Manufacturing International (Shanghai) Corp., Shanghai, China	6-11
Experimental Study on Void Growth and EM Performance Under Directional Current Reversal361 Dingrui Zhang, Weihai Fan, Jizhou Li and Kelly Yang Q&R, Semiconductor Manufacturing International Corporation (SMIC), Shanghai, China	6-12
Defect Principle and Improvement of 28nm Germanium Silicon Epitaxial Growth Process364 Qu Yan, Cai Kun, Hunglin Chen, Long Yin and Wang Kai ShangHai Huali Intergrated Circuit Corporation Shanghai, China	6-15

The Strong Effect of Spectral Mode and Directional Electrical Field for Nuisance Filtering in Defect Inspection366 Xingdi Zhang, Hunglin Chen, Yin Long and Kai Wang Shanghai Huali Microelectronics Corporation, Shanghai, China	6-18
Impact of the Stress on Reference Voltage of Power SIP Chip Applied in 5G Based Station369 Qiong Jin², Yang Chen², Na Mei², Xiangming Fang², Tuobei Sun² and Keqing Quyang¹	6-19
State Key Laboratory of Mobile Network and Mobile Multimedia Technology ² Department of Packaging and Testing ZTE Corporation, Shen Zhen, China	
A Method to Enhance the Hot Carrier Injection Effect of IonMOS Device372 Shuang Jiao, Chenchen Qiu, Jun Qian and Chang Sun Shanghai Huali Microelectronics Corporation, Shanghai, China	6-20
ATE Test Solution for High Resolution and High Voltage DAC374 Tianyu Zhang, Jian Wang and Juyang Sun Advantest, Shanghai, China	6-22
Machine Learning Based Prediction of Aging Caused Path-Delay Degradation377 Qi Wei ^{1,2} , Chenfei Wu ^{1,2} , Jiayong Li ^{1,2} and Keqing Ouyang ²	6-23
1 State Key Laboratory of Mobile Network and Mobile Multimedia Technology, China 2 Department of back-end design, Sanechips Technology Co., Ltd, Shenzhen, China	
The Inline Detection of Tiny Bubble Defect and Solution for 14nm Photolithography Process380 Yin Long, Cai Kun, Hunglin Chen and Wang Kai Shanghai Huali Integrated Circuit Corporation, Shanghai, China	6-27
WI-FI 6E TEST CHALLENGES ON ATE383 PING WANG, MASON ZHANG, ZHIQIANG BAI, HAIXIA GUO AND ENG- KEONG TAN Advantest (China) Co., Ltd, Shanghai, China	6-29
Next Generation Test Library for RF SOC on ATE387 Ping Wang, Haocheng Yuan, Vincent Lin, Haixia Guo and Goh Frank Global Application and Development Center of ADVANTEST, Shanghai, China	6-30
Wafer Defect Classification Based on DCNN Model391 Pan Tian ¹ , Chen Li ¹ , Hao Fu ¹ , Xueru Yu ¹ , Zhengying Wei ² , Qiliang Ni ² , Xu Chen ² , Yunwei Ding ² , Ruojia Xu ² and Rui Sun ²	6-31
Shanghai Integrated Circuits R&D Center Co., Ltd., Shanghai, China	
Shanghai HLMC, Shanghai, China	
RESEARCH ON RESTORATION OF COLOR OBJECT IN COMPUTATIONAL HOLOGRAPHY BASED ON GENETIC ALGORITHM394 Yufei Liu ^{1,2} , Shuang Xu ^{1,2} , Cheng Liao ^{1,2} and Chao Liu ^{1,2}	6-34

Key Laboratory of Metallurgical Equipment and Control Technology, Ministry of Education, Wuhan University of Science and Technology, Wuhan, China ² Hubei Key Laboratory of Mechanical Transmission and Manufacturing Engineering, Wuhan University of Science and Technology, Wuhan, China	
Design Optimization of GaAs/AlGaAs Lasers Epitaxially Grown on Si Substrates with Threading Dislocation Density in the Range of ~10 ⁶ cm ⁻² 397 Yugeng Shi, Bing Wang and Siyuan Yu School of Electronics and Information Technology, Sun Yat-sen University, Guangzhou, China	6-35
Fault Detection of Sensor Data in Semiconductor Processing Using Neural Network with Dynamic Time Wrapping Loss400 Wang Yong, Lu Jingjing, Chen Xu and Wei Zhengying Shanghai Huali Microelectronics Corporation, Shanghai, China	6-36
Study on Retest Reduction by Minimizing Probe Card Contact Resistance at Wafer Level403 Hua Li and Deguang Zheng Wafer Test Department, NXP Semiconductor (China) Ltd., Tianjin, China	6-46
Chapter VII – Packaging and Assembly	
Research on the Improvement of Si Performance of High Bandwidth Memory Interface By New 2.5D Silicon Interposer Structure407 Xiaolang Chen, Jian Pang, Jiangtao Zhang and Tuobei Sun Department of Packaging and Testing, ZTE Corporation, Shen Zhen, China	7-6
A high Performance Six-Pack Double Side Cooled IGBT Module for EV/HEV Applications409 Yaqing Ma, Jianfeng Li and Hongyao Long Zhuzhou CRRC Times Electric UK Innovation Center, Solihull, United Kingdom	7-17
Ashing Process on Warpage Wafer With Low Damage412 Zihan Dong, Yuanwei Lin and Yuwei Kong Department of Semiconductor Etching, NAURA Technology Group Co., Ltd., Beijing, China	7-5
Numerical Study on the Effect of Graphene Sheet Alignment on Thermal Conductance of Graphene Form415	7-14

Pei Lu ¹ , Hang Yin ¹ , Huihui Wang ¹ , Yong Zhang ¹ , Yan Zhang ¹ and Johan Liu ^{1,2} 1 School of Mechatronics Engineering and Automation, Shanghai University, Shanghai, China 2 Department of Microtechnology and Nanoscience, Chalmers University of Technology, SE- Gothenburg, Sweden	
First Pass Yield Gain Strategies During Tri-Temperature Automotive Package Test418 Jerry J. Broz and Bret A. Humphrey International Test Solutions, Inc., Reno, Nevada, USA	7-8
Research on the Thermal Reliability of Multi-Unit Power Integrated Module422 Juan Hu ^{1,2} , Jie Bao ² , Li Wang ² and Sha Lu ² 1 College of Mechanical and Electrical Engineering, Huangshan University, Huangshan, China 2 Engineering Technology Research Center of Intelligent Microsystem of Anhui Province, Huangshan, China	7-9
A Study of Thermal Interface Materials with Different Thermal Conductivity for HFCBGA Package426 Feng Wang ¹ , Na Mei ¹ , Yuanting Lai ¹ , Tuobei Sun ¹ and Keqing Ouyang ² 1 Department of Packaging and Testing, ZTE Corporation., Nanhsan District, Shenzen, China 2 State Key Laboratory of Mobile Network and Mobile Multimedia Technology	7-7
A Novel Multifunctional Single-Layer Adhesive Used for both Temporary Bonding and Mechanical Debonding in Wafer-Level Packaging Applications429 Wenkai Cheng, Yubao Wang, Debbie Blumenshine, Xiao Liu, Dongshun Bai and Rama Puligadda Brewer Science, Inc. Rolla, Missouri, USA	7-19
Research on the Design and Fabrication of Aluminum Nitride Microwave Multilayer Ceramic Package433 Lin-jie Liu, Zhen-tao Yang and Zan Ren The 13th Research Institute, CETC, Shijiazhuang, China	7-10
A Micro Soldering Method to Improve Strength Between Bonding Pad and Wire435 Li He ^{1,2} , Zhang Jie ^{1,2} , Yang Kai ^{1,2} and Wang Xi ^{1,2} 1 Microsystem & Terahertz Research Center, China Academy of Engineering Physics (CAEP), Chengdu, China 2 Institute of Electronic Engineering, CAEP, Mianyang, China	7-11
Effect of Bi Content on the Microstructure and Mechanical Properties of Cu/Sn-XBi/Cu Solder Joints after Soldering and Aging438 Mingliang Huang, Renyong Wu and Jing Ren School of Materials Science and Engineering, Dalian University of Technology Dalian, China	7-15

Non-Destructive High-Resolution Tomographic Cross-Sectional Imaging on Suspended Structures Inside a MEMS Package441 Dai Haiwen, Zhao Si Ping, Lim Meng Keong, Jagdish Saraswatula and Michael Rauscher ZEISS Process Control Solutions, Carl Zeiss Pte Ltd, Singapore	8-2
Wafer Defect Map Similarity Search Using Deep Learning in Semiconductor Manufacturing444 Sen Wang, Shijia Yan, Qiang Shen, Cong Luo, Juan Ai, Lei Li, Desheng Wang, Shenglan Ding and Qing Xia Wuhan Xinxin Semiconductor Manufacturing Co., Ltd.(XMC), Wuhan, Hubei, China	8-3
Design of CMOS Terahertz Detector Array Based on Surface Plasmon Resonance Antenna448 Haoyu Zhu ¹ , Ke Wang ¹ , Chang Liu ¹ , Xiaoli Ji ¹ and Yiming Liao ² ¹ Institute of the electronic Science and Engineering, Nanjing University, China ² School of Electronic and Optical Engineering, Nanjing University of Science and Technology, Nanjing, China	8-1
Reduction of Random Telegraph Signal Noise By Optimizing Deep Trench Isolation Process for Backside Illuminated CMOS Image Sensor451 Chunshan Zhao, Bai Kang, Wuzhi Zhang, Yamin Cao and Wei Zhou Shanghai Huali Integrated Circuit Corporation, Shanghai, China	8-4
A MEMS Micro-Tweezers for Precision Micro Fabricating and Assembly454 Zhang Hao ^{1,2} , Dong Chenglong ^{1,2} , Li He ^{1,2} , Zhang Jie ^{1,2} and Wang Xi ^{1,2} ¹ Microsystem & Terahertz Research Center, China Academy of Engineering Physics (CAEP), Chengdu, , China ² Institute of Electronic Engineering, CAEP, Mianyang, China	8-5
Design of Millimeter Wave Transceiver Isolation System Based on Polarization Converter and Grating457 Jiabing Liu ¹ , Ke Wang ¹ , Yaozu Guo ¹ , Xiaoli Ji ¹ , Ping Han ¹ , Feng Yan ¹ and Yiming Liao ² ¹ School of the Electronic Science and Engineering, Nanjing University ² School of Electronic and Optical Engineering, Nanjing University of Science and Technology	8-6
A Combination Design of 3D Depth Imaging and 2D Intensity Imaging SPAD Device Circuit460 Xiangshun Kong, Guisheng Zhao, Xiong Yang, Hao Chen, Feng Yan and Cheng Mao Nanjing University, Nanjing, Jiangsu, China	8-7
A Study on Pixel Performance of DCG CMOS Image Sensor Through Optimizing Implant Condition463 Mao Junxia Shanghai Huali Micro Electronics Co., Ltd	8-8

Chapter IX – Design Automation of Circuit and Systems

Stochastic Circuit Design Based on Exact Synthesis465 Xiang He and Zhufei Chu	9-9
EECS, Ningbo University, Ningbo, China	
Proactive Supply Noise Mitigation and Design Methodology for Robust VLSI Power Distribution468 Masanori Hashimoto and Jun Chen	9-2
Department of Information Systems Engineering, Osaka University, Osaka, Japan	
Impact of Supply Noise on Nano-Meter VLSI Design: Hard or Soft Threshold?472 Chenyi Wen, Yue Cai and Cheng Zhuo College of Information Science & Electronic Eng., Zhejiang University, Hangzhou, China	9-16
Conege of Information Science & Liectronic Eng., Zheftang Oniversity, Hangzhou, China	
Modeling of CMOS Transistors from 0.18μm Process by Artificial Neural Network476 JiaHao Wei ¹ , Tian Zhao ¹ , Zheng Zhang ² and Jing Wan ¹	9-14
¹ State key lab of ASIC and System, School of Information Science and Engineering, Fudan University, Shanghai, China ² Suzhou Foohu Technology Co., Ltd., China	
Valid Test Pattern Identification for VLSI Adaptive Test479 Tianming Ni ¹ and Tai Song ²	9-27
¹ College of Electrical Engineering, Anhui Polytechnic University, Wuhu, China ² School of Microelectronics, Hefei University of Technology, Hefei, , China	
Effective Radiation Damage to Floating Gate of Flash Memory483 CZ. Chen ^{1,3} , David Y. Hu ³ and Hanming Wu ^{2,3} ¹ University of Chinese Academy of Sciences, Huairou, Beijing, China	9-24
² School of Micro-nanoelectronics, Zhejiang University, Hangzhou, China ³ EtownIP Microelectronics, Beijing, China	
A CNN Accelerator With Embedded RISC-V Controllers486 Li Zhang, Xian Zhou and Chuliang Guo	9-23
College of Information Science & Electronic Engineering, Zhejiang University, Hangzhou, China	
A Low-Bit Quantized and HLS-Based Neural Network FPGA Accelerator for Object	9-7
Detection489 Jiaming Huang ¹ , Junyan Yang ² , Saisai Nui ² , Hang Yi ³ , Wei Wang ³ and Hai-Bao Chen ¹ ¹ School of Electronic Information and Electrical Engineering Shanghai Jiaotong University, Shanghai, China	
² Shanghai, China ³ Beijing Institute of Astronautical Systems Engineering, Beijing, China	
Mapping Convolutional Neural Networks Onto Neuromorphic Chip for Spike-Based Computation492	9-8
Chenglong Žou ^{1,2} , Xiaoxin Cui ¹ , Yisong Kuang ¹ and Xinan Wang ²	
¹ Institute of Microelectronics, Peking University, Beijing, China ² School of ECE, Peking University Shenzhen Graduate School, Shenzhen, China	
Nonlinear Quantization for In-SRAM Multi-Bit MAC Design495 Shuo Chen ¹ , Xudong Lu ¹ , Zhanxi Pang ¹ , Shaodi Wang ² , Cheng Zhuo ¹ and Xunzhao Yin ¹	9-22

² WITIN Tech Co. Ltd., Beijing, China	
ApproxDNNFlow: An Evaluation and Exploration Framework for DNNs with Approximate Multipliers499 Jide Zhang, Su Zheng and Lingli Wang School of Microelectronics, Fudan University, Shanghai, China	9-18
A Novel Toffoli Gate Design Using Quantum-dot Cellular Automata502 Huiming Tian and Zhufei Chu EECS, Ningbo University, Ningbo, China	9-10
The Study of TSV-Induced and Strained Silicon-Enhanced Stress in 3D-IC505 Jindong Zhou, Youliang Jing and Pingqiang Zhou School of Information Science and Technology, ShanghaiTech University, Shanghai, China	9-33
Design of Ternary Logic Based on RERAM Crossbars508 Weiyi Liu ¹ , Yanan Sun ¹ , Weifeng He ¹ , Qin Wang ¹ and Weikang Qian ² *Department of Micro-Nano Electronics, *University of Michigan-Shanghai Jiao Tong University Joint Institute, Shanghai Jiao Tong University, Shanghai, China	9-35
An Economic Layout Solution with 20 µm Scribe Line and Integrated Test Pad Based on 55 nm Platform511 Yang Zhao, Chengdong Liang, Luchen, Jianning Deng and Liangliang He Shanghai Huali Microelectronics Corporation (HLMC), Shanghai, China	9-11
A MobileNet Accelerator with High Processing-Element-Efficiency on FPGA514 Jiale Xiao, Yonghao Chen and Tao Su School of Electronics and Information Technology, Sun Yat-sen University, Guangzhou, Guangdong, China	9-13
Isolated Word Speech Recognition Based on BNN and Its Hardware Implementation517 Xin Liu ^{1,2} , Kefei Liu ^{1,2} , Xiaoxin Cui ^{1,2} and Yuan Wang ^{1,2} ¹ Key Laboratory of Microelectronic Devices and Circuits (MOE), Institute of Microelectronics Peking University, Beijing, China ² Beijing Laboratory of Future IC Technology and Science, Peking University, Beijing, China	9-20
Automated Recognition of Wafer Backside Image Based on a Hierarchical Model521 Junjun Zhuang ¹ , Zeyi Wang ² , Ming Guo ² , Guiyun Mao ¹ , Yong Wang ¹ , Xu Chen ¹ , Yansheng Wang ² and Zhengying Wei ^{1,2} ¹ Shanghai Huali Microelectronics Corporation, Shanghai, China ² Shanghai Huali Integrated Circuit Corporation, Shanghai, China	9-26
A Homeostasis Based Enhanced Training Method in Spiking Neural Networks for Pattern Recognition525 Guanbin Yang ^{1,2} , Dunshan Yu ^{1,2} , Song Jia ^{1,2} , Xiaoxin Cui ^{1,2} and Yuan Wang ^{1,2} **IKey Laboratory of Microelectronic Devices and Circuits (MOE), Institute of Microelectronics, Peking University, Beijing, China **Beijing Laboratory of future IC technology and science, Peking University, Beijing, China**	9-32

¹Zhejiang University, Hangzhou, China

Optimizing the Energy Efficiency of Switched-Capacitor Converters in Multiprocessor System-On-Chips with a Preset DVFS Policy528	9-34
Linfeng Zheng ^{1,2,3} and Pingqiang Zhou ShanghaiTech University, Shanghai, China	
² Shanghai Institute of Microsystem and Information Technology, Chinese Academy of	
Sciences, Shanghai, Chi	
³ University of Chinese Academy of Sciences, Beijing, China	
Automatic Digital Modeling for Analog Blocks in Mixed Signal Verification531 Yangyang Leng, Zuochang Ye, Jian Xin, Zhikai Wang and Yan Wang The Institute of Microelectronics, Tsinghua University, Beijing, China	9-36