

# **2022 IEEE International Test Conference (ITC 2022)**

**Anaheim, California, USA**  
**23 – 30 September 2022**



**IEEE Catalog Number:** CFP22ITC-POD  
**ISBN:** 978-1-6654-6271-6

**Copyright © 2022 by the Institute of Electrical and Electronics Engineers, Inc.  
All Rights Reserved**

*Copyright and Reprint Permissions:* Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

***\*\*\* This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP22ITC-POD
ISBN (Print-On-Demand):	978-1-6654-6271-6
ISBN (Online):	978-1-6654-6270-9
ISSN:	1089-3539

**Additional Copies of This Publication Are Available From:**

Curran Associates, Inc  
57 Morehouse Lane  
Red Hook, NY 12571 USA  
Phone: (845) 758-0400  
Fax: (845) 758-2633  
E-mail: [curran@proceedings.com](mailto:curran@proceedings.com)  
Web: [www.proceedings.com](http://www.proceedings.com)

# 2022 IEEE International Test Conference (ITC)

## ITC 2022

### Table of Contents

Paper Selection Process .....	xvi
-------------------------------	-----

#### Regular Paper

Wafer Map Defect Classification Based on the Fusion of Pattern and Pixel Information .....	1
<i>Yiwen Liao (University of Stuttgart, Germany), Raphaël Latty (Advantest Europe GmbH, Germany), Paul R. Gensler (University of Stuttgart, Germany), Hussam Amrouch (University of Stuttgart, Germany), and Bin Yang (University of Stuttgart, Germany)</i>	
Modeling Challenge Covariances and Design Dependency for Efficient Attacks on Strong PUFs ....	10
<i>Hongfei Wang (Hubei Engineering Research Center on Big Data Security; National Engineering Research Center for Big Data Technology and System, Services Computing Technology and System Lab; Huazhong University of Science and Technology, China), Wei Liu (National Engineering Research Center for Big Data Technology and System, Services Computing Technology and System Lab; Cluster and Grid Computing Lab, School of Computer Science and Technology; Huazhong University of Science and Technology, China), Hai Jin (National Engineering Research Center for Big Data Technology and System, Services Computing Technology and System Lab; Cluster and Grid Computing Lab, School of Computer Science and Technology; Huazhong University of Science and Technology, China), Yu Chen (Hubei Engineering Research Center on Big Data Security; National Engineering Research Center for Big Data Technology and System, Services Computing Technology and System Lab; Huazhong University of Science and Technology, China), and Wenjie Cai (College of Public Administration; Huazhong University of Science and Technology, China)</i>	
DIST: Deterministic In-System Test with X-Masking .....	20
<i>Grzegorz Mrugalski (Siemens Digital Industries Software, USA), Janusz Rajska (Siemens Digital Industries Software, USA), Jerzy Tyszer (Poznan University of Technology, Poland), and Bartosz Włodarczak (Poznan University of Technology, Poland)</i>	
Reliability Study of 14 nm Scan Chains and Its Application to Hardware Security .....	28
<i>Franco Stellari (IBM Research, USA) and Peilin Song (IBM Research, USA)</i>	

Neural Fault Analysis for SAT-Based ATPG .....	36
Junhua Huang ( <i>Noah's Ark Lab, Huawei, China</i> ), Hui-Ling Zhen ( <i>Noah's Ark Lab, Huawei, China</i> ), Naixing Wang ( <i>HiSilicon Co., Huawei, China</i> ), Hui Mao ( <i>Noah's Ark Lab, Huawei, China</i> ), Mingxuan Yuan ( <i>Noah's Ark Lab, Huawei, China</i> ), and Yu Huang ( <i>HiSilicon Co., Huawei, China</i> )	
TAMED: Transitional Approaches for LFI Resilient State Machine Encoding .....	46
Muhtadi Choudhury ( <i>University of Florida, USA</i> ), Minyan Gao ( <i>University of Florida, USA</i> ), Shahin Tajik ( <i>Worcester Polytechnic Institute, USA</i> ), and Domenic Forte ( <i>University of Florida, USA</i> )	
Configurable BISR Chain For Fast Repair Data Loading .....	56
Wei Zou ( <i>Siemens Digital Industries Software, USA</i> ) and Benoit Nadeau-Dostie ( <i>Siemens Digital Industries Software, Canada</i> )	
A Practical Online Error Detection Method for Functional Safety using Three-Site Implications .....	63
Kazuya Ioki ( <i>ROHM Co., Ltd., Japan</i> ), Yasuyuki Kai ( <i>Kyushu Institute of Technology, Japan</i> ), Kohei Miyase ( <i>Kyushu Institute of Technology, Japan</i> ), and Seiji Kajihara ( <i>Kyushu Institute of Technology, Japan</i> )	
Transient Fault Pruning for Effective Candidate Reduction in Functional Debugging .....	73
Dun-An Yang ( <i>National Tsing Hua University, Taiwan</i> ), Jing-Jia Liou ( <i>National Tsing Hua University, Taiwan</i> ), and Harry H. Chen ( <i>MediaTek Inc., Computing and AI Technology Group, Taiwan</i> )	
Scan-Based Test Chip Design with XOR-Based C-Testable Functional Blocks .....	82
Yan-Fu Chen ( <i>National Cheng Kung University, Taiwan</i> ), Duo-Yao Kang ( <i>National Cheng Kung University, Taiwan</i> ), and Kuen-Jong Lee ( <i>National Cheng Kung University, Taiwan</i> )	
Fault Modeling and Testing of Memristor-Based Spiking Neural Networks .....	92
Kuan-Wei Hou ( <i>National Tsing Hua University, Taiwan</i> ), Hsueh-Hung Cheng ( <i>National Tsing Hua University, Taiwan</i> ), Chi Tung ( <i>National Tsing Hua University, Taiwan</i> ), Cheng-Wen Wu ( <i>National Tsing Hua University, Taiwan; Industrial Technology Research Institute, Taiwan</i> ), and Juin-Ming Lu ( <i>Industrial Technology Research Institute, Taiwan</i> )	
RCANet: Root Cause Analysis via Latent Variable Interaction Modeling for Yield Improvement....	100
Xiaopeng Zhang ( <i>The Chinese University of Hong Kong</i> ), Shoubo Hu ( <i>Huawei Noah's Ark Lab</i> ), Zhitang Chen ( <i>Huawei Noah's Ark Lab</i> ), Shengyu Zhu ( <i>Huawei Noah's Ark Lab</i> ), Evangeline F.Y. Young ( <i>The Chinese University of Hong Kong</i> ), Pengyun Li ( <i>HiSilicon</i> ), Cheng Chen ( <i>HiSilicon</i> ), Yu Huang ( <i>HiSilicon</i> ), and Jianye Hao ( <i>Huawei Noah's Ark Lab</i> )	
Compression-Aware ATPG .....	108
Xing Wang ( <i>HiSilicon Technologies Co., Ltd., China</i> ), Zezhong Wang ( <i>HiSilicon Technologies Co., Ltd., China</i> ), Naixing Wang ( <i>HiSilicon Technologies Co., Ltd., China</i> ), Weiwei Zhang ( <i>HiSilicon Technologies Co., Ltd., China</i> ), and Yu Huang ( <i>HiSilicon Technologies Co., Ltd., China</i> )	

Fault Diagnosis for Resistive Random-Access Memory and Monolithic Inter-Tier Vias in Monolithic 3D Integration .....	118
Shao-Chun Hung ( <i>Duke University, USA</i> ), Arjun Chaudhuri ( <i>Duke University, USA</i> ), Sanmitra Banerjee ( <i>Duke University, USA</i> ), and Krishnendu Chakrabarty ( <i>Duke University, USA</i> )	
Existence of Single-Event Double-Node Upsets (SEDU) in Radiation-Hardened Latches for Sub-65nm CMOS Technologies .....	128
Sam M.-H. Hsiao ( <i>National Yang Ming Chiao Tung University, Taiwan</i> ), Lowry P.-T. Wang ( <i>National Yang Ming Chiao Tung University, Taiwan</i> ), Aaron C.-W. Liang ( <i>National Yang Ming Chiao Tung University, Taiwan</i> ), and Charles H.-P. Wen ( <i>National Yang Ming Chiao Tung University, Taiwan</i> )	
Just-Enough Stress Test for Infant-Mortality Screening using Speed Binning .....	137
Chen-Lin Tsai ( <i>National Tsing Hua University, Taiwan</i> ) and Shi-Yu Huang ( <i>National Tsing Hua University, Taiwan</i> )	
Automatic Structural Test Generation for Analog Circuits using Neural Twins .....	145
Jonti Talukdar ( <i>Duke University, USA</i> ), Arjun Chaudhuri ( <i>Duke University, USA</i> ), Mayukh Bhattacharya ( <i>Synopsys Inc., USA</i> ), and Krishnendu Chakrabarty ( <i>Duke University, USA</i> )	
ADWIL: A Zero-Overhead Analog Device Watermarking using Inherent IP Features .....	155
Upoma Das ( <i>University of Florida, USA</i> ), Md Rafid Muttaki ( <i>University of Florida, USA</i> ), Mark M. Tehranipoor ( <i>University of Florida, USA</i> ), and Farimah Farahmandi ( <i>University of Florida, USA</i> )	
RTL-FSMx: Fast and Accurate Finite State Machine Extraction at the RTL for Security Applications .....	165
Rasheed Kibria ( <i>University of Florida, Florida</i> ), M. Sazadur Rahman ( <i>University of Florida, Florida</i> ), Farimah Farahmandi ( <i>University of Florida, Florida</i> ), and Mark Tehranipoor ( <i>University of Florida, Florida</i> )	
Diagnosing Double Faulty Chains Through Failing Bit Separation .....	175
Cheng-Sian Kuo ( <i>National Taiwan University, Taiwan</i> ), Bing-Han Hsieh ( <i>National Taiwan University, Taiwan</i> ), James Chien-Mo Li ( <i>National Taiwan University, Taiwan</i> ), Chris Nigh ( <i>Qualcomm Technologies, Inc., USA</i> ), Gaurav Bhargava ( <i>Qualcomm Technologies, Inc., USA</i> ), and Mason Chern ( <i>Qualcomm Semiconductor Corporation, Taiwan</i> )	
Efficient and Robust Resistive Open Defect Detection Based on Unsupervised Deep Learning .....	185
Yiwen Liao ( <i>University of Stuttgart, Germany</i> ), Zahra Paria Najafi-Haghi ( <i>University of Stuttgart, Germany</i> ), Hans-Joachim Wunderlich ( <i>University of Stuttgart, Germany</i> ), and Bin Yang ( <i>University of Stuttgart, Germany</i> )	
DeepTPI: Test Point Insertion with Deep Reinforcement Learning .....	194
Zhengyuan Shi ( <i>The Chinese University of Hong Kong, Hong Kong S.A.R.</i> ), Min Li ( <i>The Chinese University of Hong Kong, Hong Kong S.A.R.</i> ), Sadaf Khan ( <i>The Chinese University of Hong Kong, Hong Kong S.A.R.</i> ), Liuzheng Wang ( <i>HiSilicon Technologies Co., Ltd., China</i> ), Naixing Wang ( <i>HiSilicon Technologies Co., Ltd., China</i> ), Yu Huang ( <i>HiSilicon Technologies Co., Ltd., China</i> ), and Qiang Xu ( <i>The Chinese University of Hong Kong, Hong Kong S.A.R.</i> )	

PPA Optimization of Test Points in Automotive Designs .....	204
<i>Brian Foutz (Cadence Design Systems, USA), Sarthak Singhal (Cadence Design Systems, USA), Prateek Kumar Rai (Cadence Design Systems, USA), Krishna Chakravadhanula (Cadence Design Systems, USA), Vivek Chickermane (Cadence Design Systems, USA), Bharath Nandakumar (Cadence Design Systems, USA), Sameer Chillarige (Cadence Design Systems, USA), Christos Papameletis (Cadence Design Systems, USA), and Satish Ravichandran (Cadence Design Systems, USA)</i>	
ML-Assisted Vmin Binning with Multiple Guard Bands for Low Power Consumption .....	213
<i>Wei-Chen Lin (National Taiwan University, Taiwan), Chun Chen (National Taiwan University, Taiwan), Chao-Ho Hsieh (National Taiwan University, Taiwan), James Chien-Mo Li (National Taiwan University, Taiwan), Eric Jia-Wei Fang (MediaTek Inc., Taiwan), and Sung S.-Y. Hsueh (MediaTek Inc., Taiwan)</i>	
Reusing IEEE 1687-Compatible Instruments and Sub-Networks over a System Bus .....	219
<i>Farrokh Ghani Zadegan (Ericsson, Sweden), Zilin Zhang (Ericsson, Sweden), Kim Petersén (Ericsson, Sweden), and Erik Larsson (Lund University, Sweden)</i>	
Unsupervised Learning-Based Early Anomaly Detection in AMS Circuits of Automotive SoCs .....	229
<i>Ayush Arunachalam (University of Texas at Dallas), Athulya Kizhakkayil (University of Texas at Dallas), Shamik Kundu (University of Texas at Dallas), Arnab Raha (Intel Corporation), Suvadeep Banerjee (Intel Corporation), Robert Jin (NXP Semiconductors), Fei Su (Intel Corporation), and Kanad Basu (University of Texas at Dallas)</i>	
Compact Functional Test Generation for Memristive Deep Learning Implementations using Approximate Gradient Ranking .....	239
<i>Soyed Tuhin Ahmed (Karlsruhe Institute of Technology, Germany) and Mehdi B. Tahoori (Karlsruhe Institute of Technology, Germany)</i>	
Multi-die Parallel Test Fabric for Scalability and Pattern Reusability .....	249
<i>Arani Sinha (Intel Corporation), Yonsang Cho (Intel Corporation), Jonathan Easter (Intel Corporation), and Meizel V. Leiva Rojas (Intel Corporation)</i>	
A Path Selection Flow for Functional Path Ring Oscillators using Physical Design Data .....	258
<i>Tobias Kilian (Infineon Technologies AG, Germany; Technical University of Munich, Germany), Markus Hanel (Technical University of Munich, Germany), Daniel Tille (Infineon Technologies AG, Germany), Martin Huch (Infineon Technologies AG, Germany), and Ulf Schlichtmann (Technical University of Munich, Germany)</i>	
ML-Assisted Bug Emulation Experiments for Post-Silicon Multi-Debug of AMS Circuits .....	268
<i>Jun-Yang Lei (Georgia Institute of Technology, USA) and Abhijit Chatterjee (Georgia Institute of Technology, USA)</i>	
A Multi-Level Approach to Evaluate the Impact of GPU Permanent Faults on CNN's Reliability....	278
<i>Josie E. Rodriguez Condia (Politecnico di Torino, Italy), Juan-David Guerrero-Balaguera (Politecnico di Torino, Italy), Fernando F. dos Santos (University of Rennes - INRIA, France), Matteo Sonza Reorda (Politecnico di Torino, Italy), and Paolo Rech (University of Trento, Italy)</i>	

Language Driven Analytics for Failure Pattern Feedforward and Feedback .....	288
<i>Min Jian Yang (University of California, Santa Barbara, USA), Yueling Zeng (University of California at Santa Barbara, USA), and Li-C. Wang (University of California at Santa Barbara, USA)</i>	
DEFCON: Defect Acceleration Through Content Optimization .....	298
<i>Suriyaprakash Natarajan (Intel Corporation, USA), Abhijit Sathaye (Intel Corporation, USA), Chaitali Oak (Intel Corporation, USA), Nipun Chaplot (Intel Corporation, USA), and Suvadeep Banerjee (Intel Corporation, USA)</i>	
Test Generation for an Iterative Design Flow with RTL Changes .....	305
<i>Jerin Joe (Purdue University, USA), Nilanjan Mukherjee (Siemens Digital Industries Software, USA), Irith Pomeranz (Purdue University, USA), and Janusz Rajska (Siemens Digital Industries Software, USA)</i>	
PEPR: Pseudo-Exhaustive Physically-Aware Region Testing .....	314
<i>Chris Nigh (Carnegie Mellon University), R.D. Blanton (Carnegie Mellon University), Danielle Duvalsaing (Carnegie Mellon University), Wei Li (Carnegie Mellon University), and Subhasish Mitra (Stanford University)</i>	
Error Model (EM)—A New Way of Doing Fault Simulation .....	324
<i>Nirmal Saxena (NVIDIA, USA) and Atieh Lotfi (NVIDIA, USA)</i>	
Comprehensive Power-Aware ATPG Methodology for Complex low-Power Designs .....	334
<i>Khader Abdel-Hafez (Synopsys Inc, California), Michael Dsouza (Synopsys Inc, California), Likith Kumar Manchukonda (Synopsys Inc, California), Elddie Tsai (Synopsys Inc, California), Karthikeyan Natarajan (Synopsys Inc, California), Ting-Pu Tai (Synopsys Inc, Taiwan), Wenhao Hsueh (MediaTek Inc, Taiwan), and Smith Lai (MediaTek Inc, Taiwan)</i>	
Scaling Physically Aware Logic Diagnosis to Complex High Volume 7nm Server Processors .....	340
<i>Bharath Nandakumar (Cadence Design Systems, India), Madhur Maheshwari (Cadence Design Systems, India), Sameer Chillarige (Cadence Design Systems, India), Robert Redburn (IBM, USA), Jeff Zimmerman (IBM, USA), Nicholai L'Esperance (IBM, USA), and Edward Dziarcak (IBM, USA)</i>	
Using Custom Fault Models to Improve Understanding of Silicon Failures .....	348
<i>Subhadip Kundu (Qualcomm Technologies Inc.), Gaurav Bhargava (Qualcomm Technologies Inc), Lesly Endrinal (Qualcomm Technologies Inc.), and Lavakumar Ranganathan (Qualcomm Technologies Inc.)</i>	
An Innovative Strategy to Quickly Grade Functional Test Programs .....	355
<i>Francesco Angione (Politecnico di Torino, Italy), Paolo Bernardi (Politecnico di Torino, Italy), Andrea Calabrese (Politecnico di Torino, Italy), Lorenzo Cardone (Politecnico di Torino, Italy), Alessandro Niccoletti (Politecnico di Torino, Italy), Davide Piumatti (Politecnico di Torino, Italy), Stefano Quer (Politecnico di Torino, Italy), Davide Appello (STMicroelectronics, Italy), Vincenzo Tancorre (STMicroelectronics, Italy), and Roberto Ugioli (STMicroelectronics, Italy)</i>	

Probeless DfT Scheme for Testing 20k I/Os of an Automotive Micro-LED Headlamp Driver IC .....	365
<i>Hans Martin von Staudt (Dialog Semiconductor - A Renesas Company, Germany), Luai Tarek Elnawawy (Dialog Semiconductor - A Renesas Company, Germany), Sarah Wang (Dialog Semiconductor - A Renesas Company, USA), Larry Ping (Dialog Semiconductor - A Renesas Company, USA), and Jung Woo Choi (Dialog Semiconductor - A Renesas Company, USA)</i>	
Understanding Vmin Failures for Improved Testing of Timing Marginalities .....	372
<i>Adit D. Singh (Auburn University, USA)</i>	
IEEE P1687.1: Extending the Network Boundaries for Test .....	382
<i>Michael Laisne (Dialog Semiconductor – A Renesas Company, USA), Alfred Crouch (Amida Technology Solutions, Inc., USA), Michele Portolan (Univ Grenoble Alpes, France), Martin Keim (Siemens Digital Industries Software, USA), Hans Martin von Staudt (Dialog Semiconductor – A Renesas Company, Germany), Bradford Van Treuren (VT Enterprises Consulting Services, USA), Jeff Rearick (Advanced Micro Devices, USA), and Songlin Zuo (Facebook, USA)</i>	
Fine-Grained Built-In Self-Repair Techniques for NAND Flash Memories .....	391
<i>Shyue-Kung Lu (National Taiwan University of Science and Technology, Taiwan), Shi-Chun Tseng (National Taiwan University of Science and Technology, Taiwan), and Kohei Miyase (Kyushu Institute of Technology, Japan)</i>	
Accelerating RRAM Testing with Low-cost Computation-in-Memory based DFT .....	400
<i>Abhairaj Singh (Technische Universiteit Delft, the Netherlands), Moritz Fieback (Technische Universiteit Delft, the Netherlands), Rajendra Bishnoi (Technische Universiteit Delft, the Netherlands), Filip Bradarić (Technische Universiteit Delft, the Netherlands), Anteneh Gebregiorgis (Technische Universiteit Delft, the Netherlands), Rajiv Joshi (IBM, USA), and Said Hamdioui (Technische Universiteit Delft, the Netherlands)</i>	

## **IP Long**

New R&R Methodology in Semiconductor Manufacturing Electrical Testing .....	410
<i>Lorella Bordogna (STMicroelectronics, Italy), Fabio Bremilla (STMicroelectronics, Italy), Alberto Paganí (STMicroelectronics, Italy), and Marco Spinetta (STMicroelectronics, Italy)</i>	
Industry Evaluation of Reversible Scan Chain Diagnosis .....	420
<i>Soumya Mittal (Qualcomm Technologies, Inc., US), Szczepan Urban (Siemens EDA, Poznan, Poland), Kun Young Chung (Qualcomm Technologies, Inc., USA), Jakub Janicki (Siemens EDA, Poznan, Poland), Wu-Tung Cheng (Siemens EDA, USA), Martin Parley (Qualcomm Technologies, Inc., USA), Manish Sharma (Siemens EDA, USA), and Shaun Nicholson (Qualcomm Technologies, Inc., USA)</i>	

Defect-Directed Stress Testing Based on Inline Inspection Results .....	427
<i>Chen He (NXP Semiconductors, USA), Paul Gorsch (NXP Semiconductors, USA), Onder Anilturk (NXP Semiconductors, USA), Joyce Witowski (NXP Semiconductors, USA), Carl Ford (NXP Semiconductors, USA), Rahul Kaylan (NXP Semiconductors, USA), John Robinson (KLA Corporation, USA), David Price (KLA Corporation, USA), Jay Rathert (KLA Corporation, USA), Barry Saville (KLA Corporation, USA), and Dave Lee (KLA Corporation, USA)</i>	
Application of Sampling in Industrial Analog Defect Simulation .....	436
<i>Mayukh Bhattacharya (Synopsys, Inc., USA), Beatrice Solignac (Synopsys, Inc., France), and Michael Durr (Synopsys, Inc., USA)</i>	
Low Capture Power At-Speed Test with Local Hot Spot Analysis to Reduce Over-Test .....	446
<i>Ankush Srivastava (Qualcomm India Pvt Ltd, India) and Jais Abraham (Qualcomm India Pvt Ltd, India)</i>	
Challenges for High Volume Testing of Embedded IO Interfaces in Disaggregated Microprocessor Products .....	456
<i>Esteban Garita-Rodriguez (Intel Corporation, Costa Rica), Renato Rimolo-Donadio (Intel Corporation, Costa Rica), and Rafael Zamora-Salazar (Intel Corporation, Costa Rica)</i>	
Achieving Automotive Safety Requirements Through Functional In-Field Self-Test for Deep Learning Accelerators .....	465
<i>Takumi Uezono (Hitachi Ltd., Japan), Yi He (University of Chicago, USA), and Yanjing Li (University of Chicago, USA)</i>	

## **Short Paper**

Transforming an n-Detection Test Set into a Test Set for a Variety of Fault Models .....	474
<i>Irith Pomeranz (Purdue University, USA)</i>	
Hardware Root of Trust for SSN-Based DFT Ecosystems .....	479
<i>Janusz Rajski (Siemens Digital Industries Software), Maciej Trawka (Siemens Digital Industries Software), Jerzy Tyszer (Poznan University of Technology, Poland), and Bartosz Włodarczak (Poznan University of Technology, Poland)</i>	
A Comprehensive Learning-Based Flow for Cell-Aware Model Generation .....	484
<i>P. d'Hondt (STMicroelectronics, France), A. Ladhar (STMicroelectronics, France), P. Girard (LIRMM – Univ. of Montpellier / CNRS, France), and A. Virazel (LIRMM – Univ. of Montpellier / CNRS, France)</i>	
DFT-Enhanced Test Scheme for Spin-Transfer-Torque (STT) MRAMs .....	489
<i>Ze-Wei Pan (National Central University, Taiwan) and Jin-Fu Li (National Central University, Taiwan)</i>	
GreyConE: Greybox Fuzzing + Concolic Execution Guided Test Generation for High Level Designs .....	494
<i>Mukta Debnath (Indian Statistical Institute, India), Animesh Basak Chowdhury (New York University, USA), Debasri Saha (Calcutta University, India), and Susmita Sur-Kolay (Indian Statistical Institute, India)</i>	

Efficient Low Cost Alternative Testing of Analog Crossbar Arrays for Deep Neural Networks .....	499
<i>Kwondo Ma (Georgia Institute of Technology, Atlanta), Anurup Saha (Georgia Institute of Technology, Atlanta), Chandramouli Amarnath (Georgia Institute of Technology, Atlanta), and Abhijit Chatterjee (Georgia Institute of Technology, Atlanta)</i>	
RIBoNN: Designing Robust In-Memory Binary Neural Network Accelerators .....	504
<i>Shamik Kundu (University of Texas at Dallas, USA), Akul Malhotra (Purdue University, USA), Arnab Raha (Intel Corporation, USA), Sumeet K. Gupta (Purdue University, USA), and Kanad Basu (University of Texas at Dallas, USA)</i>	
Optimal Order Polynomial Transformation for Calibrating Systematic Errors in Multisite Testing .....	509
<i>Praise Ololade Farayola (Iowa State University, USA), Isaac Bruce (Iowa State University, USA), Shravan K. Chaganti (Texas Instruments Inc.), Abalhassan Sheikh (Texas Instruments Inc.), Srivaths Ravi (Texas Instruments Inc.), and Degang Chen (Iowa State University, USA)</i>	
Low Cost High Accuracy Stimulus Generator for On-Chip Spectral Testing .....	514
<i>Kushagra Bhatheja (Iowa State University, USA), Shravan Chaganti (Iowa State University, USA), Degang Chen (Iowa State University, USA), Xiankun Robert Jin (NXP Semiconductors, USA), Chris C. Dao (NXP Semiconductors, USA), Juxiang Ren (NXP Semiconductors, USA), Abhishek Kumar (NXP Semiconductors, USA), Daniel Correa (NXP Semiconductors, USA), Mark Lehmann (NXP Semiconductors, USA), Thomas Rodriguez (NXP Semiconductors, USA), Eric Kingham (NXP Semiconductors, USA), Joel R. Knight (NXP Semiconductors, USA), Allan Dobbin (NXP Semiconductors, USA), Scott W. Herrin (NXP Semiconductors, USA), and Doug Garrity (NXP Semiconductors, USA)</i>	
The Impact of On-Chip Training to Adversarial Attacks in Memristive Crossbar Arrays .....	519
<i>Bijay Raj Paudel (Southern Illinois University Carbondale, USA) and Spyros Tragoudas (Southern Illinois University Carbondale, USA)</i>	
Runtime Fault Diagnostics for GPU Tensor Cores .....	524
<i>Saurabh Hukerikar (NVIDIA Corporation, USA) and Nirmal Saxena (NVIDIA Corporation, USA)</i>	
Fault-Coverage Maximizing March Tests for Memory Testing .....	529
<i>Ryan Feng (University of Southern California, USA), Yunkun Lin (University of Southern California, USA), Yunfei Lou (University of Southern California, USA), Lei Gao (University of Southern California, USA), Vaibhav Gera (University of Southern California, USA), Boxuan Li (University of Southern California, USA), Vennela Chowdary Nekkanti (University of Southern California, USA), Aditya Rajendra Pharande (University of Southern California, USA), Kunal Sheth (University of Southern California, USA), Meghana Thommondru (University of Southern California, USA), Guizhong Ye (University of Southern California, USA), and Sandeep Gupta (University of Southern California, USA)</i>	
Analyzing the Electromigration Challenges of Computation in Resistive Memories .....	534
<i>Mahta Mayahirnia (Karlsruhe Institute of Technology (KIT), Germany), Mehdi Tahoori (Karlsruhe Institute of Technology (KIT), Germany), Manu Perumkunnil (IMEC, Belgium), Kristof Croes (IMEC, Belgium), and Francky Catthoor (IMEC, Belgium)</i>	

Circuit-to-Circuit Attacks in SoCs via Trojan-Infected IEEE 1687 Test Infrastructure .....	539
<i>Michele Portolan (Université Grenoble Alpes, CNRS, Grenoble INP, TIMA, France), Antonios Pavlidis (Sorbonne Université, CNRS, LIP6, France), Giorgio Di Natale (Université Grenoble Alpes, CNRS, Grenoble INP, TIMA, France), Eric Faehn (ST Microelectronics, France), and Haralampos-G. Stratigopoulos (Sorbonne Université, CNRS, LIP6, France)</i>	

## IP Short

Enhanced Data Pattern to Detect Defects in Flash Memory Address Decoder .....	544
<i>Weng Joe Soh (NXP Semiconductors, Malaysia) and Chen He (NXP Semiconductors, USA)</i>	
Wafer Defect Pattern Classification with Explainable-Decision Tree Technique .....	549
<i>Ken Chau-Cheung Cheng (NXP Semiconductors Taiwan Ltd., Taiwan), Katherine Shu-Min Li (National Sun Yat-Sen University, Taiwan), Sying-Jyan Wang (National Chung Hsing University, Taiwan), Andrew Yi-Ann Huang (NXP Semiconductors Taiwan Ltd., Taiwan), Chen-Shiun Lee (NXP Semiconductors Taiwan Ltd., Taiwan), Leon Li-Yang Chen (NXP Semiconductors Taiwan Ltd., Taiwan), Peter Yi-Yu Liao (NXP Semiconductors Taiwan Ltd., Taiwan), and Nova Cheng-Yen Tsai (NXP Semiconductors Taiwan Ltd., Taiwan)</i>	
Yield-Enhanced Probe Head Cleaning with AI-Driven Image and Signal Integrity Pattern Recognition for Wafer Test .....	554
<i>Nadun Sinhabahu (NXP Semiconductors Taiwan Ltd., Taiwan), Katherine Shu-Min Li (National Sun Yat-Sen University, Taiwan), Jian-De Li (National Chung Hsing University, Taiwan), J.R. Wang (NXP Semiconductors Taiwan Ltd., Taiwan), and Sying-Jyan Wang (National Chung Hsing University, Taiwan)</i>	
Virtual Prototyping: Closing the Digital gap Between Product Requirements and Post-Si Verification .....	559
<i>Manuel Harrant (Infineon Technologies, Germany), Thomas Nirmaier (Infineon Technologies, Germany), Marc Huppmann (Infineon Technologies, Germany), Wendy You (Infineon Technologies, Germany), and Georg Pelz (Infineon Technologies, Germany)</i>	
4.5 Gbps MIPI D-PHY Receiver Circuit for Automatic Test Equipment .....	563
<i>Seongkwan Lee (Samsung Electronics, South Korea), Cheolmin Park (Samsung Electronics, South Korea), Minho Kang (Samsung Electronics, South Korea), Jun Yeon Won (Samsung Electronics, South Korea), HyungSun Ryu (Samsung Electronics, South Korea), Jaemoo Choi (Samsung Electronics, South Korea), and Byunghyun Yim (Samsung Electronics, South Korea)</i>	
Improvements in Automated IC Socket Pin Defect Detection .....	568
<i>Vijayakumar Thangamariappan (Advantest America Inc., USA), Nidhi Agrawal (Advantest America Inc., USA), Jason Kim (Advantest America Inc., USA), Constantinos Xanthopoulos (Advantest America Inc., USA), Ken Butler (Advantest America Inc., USA), Ira Leventhal (Advantest America Inc., USA), and Joe Xiao (Essai Inc., USA)</i>	

Accurate Failure Rate Prediction Based on Gaussian Process using WAT Data .....	573
<i>Makoto Eiki (Sony Semiconductor Manufacturing Corporation, Japan; Nara Institute of Science and Technology, Japan), Tomoki Nakamura (Sony Semiconductor Manufacturing Corporation, Japan), Masuo Kajiyama (Sony Semiconductor Manufacturing Corporation, Japan), Michiko Inoue (Nara Institute of Science and Technology, Japan), and Michihiro Shintani (Kyoto Institute of Technology, Japan)</i>	
Optimization of Tests for Managing Silicon Defects in Data Centers .....	578
<i>David Lerner (Intel Corporation), Benson Inkley (Intel Corporation), Shubhada Sahasrabudhe (Intel Corporation), Ethan Hansen (Intel Corporation), Luis Rojas Munoz (Intel Corporation), and Arjan van de Ven (Intel Corporation)</i>	
Zero Trust Approach to IC Manufacturing and Testing .....	583
<i>Brian Buras (Advantest America Inc.), Constantinos Xanthopoulos (Advantest America Inc.), Ken Butler (Advantest America Inc.), and Jason Kim (Advantest America Inc.)</i>	
Improving Structural Coverage of Functional Tests with Checkpoint Signature Computation .....	587
<i>Benjamin Nieuwenhuis (Texas Instruments, USA) and Devanathan Varadarajan (Texas Instruments, USA)</i>	

## ITC-Asia

Fault Resilience Techniques for Flash Memory of DNN Accelerators .....	591
<i>Shyue-Kung Lu (National Taiwan University of Science and Technology, Taiwan), Yu-Sheng Wu (National Taiwan University of Science and Technology, Taiwan), Jin-Jua Hong (National University of Kaohsiung, Taiwan), and Kohei Miyase (Kyushu Institute of Technology, Japan)</i>	
Improving Test Quality of Memory Chips by a Decision Tree-Based Screening Method .....	601
<i>Ya-Chi Cheng (National Cheng Kung University, Taiwan), Pai-Yu Tan (National Tsing Hua University, Taiwan), Cheng-Wen Wu (National Tsing Hua University, Taiwan; National Cheng Kung University, Taiwan), Ming-Der Shieh (National Cheng Kung University, Taiwan), Chien-Hui Chuang (Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan), and Gordon Liao (Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan)</i>	

## TTTC-PhD

Next Generation Design For Testability, Debug and Reliability Using Formal Techniques .....	609
<i>Sebastian Huhn (University of Bremen) and Rolf Drechsler (University of Bremen)</i>	
Testing of Analog Circuits using Statistical and Machine Learning Techniques .....	619
<i>Supriyo Srimani (School of VLSI Technology, IIEST, Shibpur) and Hafizur Rahaman (School of VLSI Technology, IIEST, Shibpur)</i>	
AI-Driven Assurance of Hardware IP Against Reverse Engineering Attacks .....	627
<i>Prabuddha Chakraborty (University of Florida, USA) and Swarup Bhunia (University of Florida, USA)</i>	

## **ART Workshop**

High-Coverage DfT and Reliability Enhancements for Automotive Floating Gate OTP Beyond AEC-Q100 .....	637
<i>Hans Martin von Staudt (Dialog Semiconductor - A Renesas Company, Germany), Franz Schuler (Dialog Semiconductor - A Renesas Company, Germany), Rohitaswa Bhattacharya (Dialog Semiconductor - A Renesas Company, Germany), Justin Wei-Lin Cheng (eMemory Technology Inc.), Cheng-Da Huang (eMemory Technology Inc.), and Parker Chih-Chun Chen (eMemory Technology Inc.)</i>	
A Novel Protection Technique for Embedded Memories with Optimized PPA .....	642
<i>Costas Argyrides (AMD, USA), Vilas Sridharan (AMD, USA), Hayk Danoyan (Synopsys, Armenia), Gurgen Harutyunyan (Synopsys, Armenia), and Yervant Zorian (Synopsys, USA)</i>	
In-field Data Collection System through Logic BIST for large Automotive Systems-on-Chip .....	646
<i>Giusy Iaria (Politecnico di Torino), Gabriele Filippone (Politecnico di Torino), Matteo Sonza Reorda (Politecnico di Torino), Davide Appello (STMicroelectronics), Vincenzo Tancorre (STMicroelectronics), and Giuseppe Garozzo (STMicroelectronics)</i>	

## **SLM Workshop**

An Efficient Test Strategy for Detection of Electromigration Impact in Advanced FinFET Memories .....	650
<i>Mahta Mayahinia (Karlsruhe Institute of Technology (KIT), Germany), Mehdi Tahoori (Karlsruhe Institute of Technology (KIT), Germany), Gurgen Harutyunyan (Synopsys), Grigor Tshagharyan (Synopsys), and Karen Amirkhanyan (Synopsys)</i>	
High Speed IO Access for Test forms the foundation for Silicon Lifecycle Management .....	656
<i>Amit Pandey (Amazon), Brendan Tully (Amazon), and Karthikeyan Natarajan (Synopsys)</i>	
In search of Vmin for dynamic power management and reliable operation in mission mode .....	661
<i>Firooz Massoudi (Synopsys Inc)</i>	
<b>Author Index .....</b>	<b>665</b>