2023 28th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC 2023)

Beijing, China
16-19 July 2023

IEEE Catalog Number: CFP23012-POD
ISBN: 979-8-3503-0577-7

Copyright © 2023 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP23012-POD
ISBN (Print-On-Demand):	979-8-3503-0577-7
ISBN (Online):	979-8-3503-0576-0
ISSN:	2643-1394

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

2023 28th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC 2023)

Table of Contents

Message from the Organizing Committee ..... **v**
Organizing Committee ..... **vii**
Fresh Ideas Papers ..... **ix**

Chapter 1: Asynchronous Pipelines, Test, Security, Fault Tolerance, and Case Study

Opportunistic Mutual Exclusion 1

Karthi Srinivasan [1], Yoram Moses [2], Rajit Manohar [1]

[1] Department of Electrical Engineering, Yale University, New Haven, USA
[2] Department of Electrical Engineering, Technion-Israel Institute of Technology, Haifa, Israel

Timed Signalling Processes 10

Rajit Manohar [1], Yoram Moses [2]

[1] Yale University, New Haven, CT 06520, USA
[2] Technion-Israel Institute of Technology, Haifa 32000, Israel

Case Study for Skewing MTNCL Circuits 20

Cole Sherrill, Kyle Orman, Nicholas Brown, Jia Di

Computer Science and Computer Engineering Department, University of Arkansas, Fayetteville, AR, USA

Chapter 2: CAD Tools for Asynchronous Design, Synthesis, Analysis, and Optimization

Designing Self-timed Asynchronous Circuits with Chisel 27

Jilin Zhang, Chunqi Qian, Dexuan Huo, Jian Zhang, Hong Chen

School of Integrated Circuits, Tsinghua University, Beijing, China

Yak: An Asynchronous Bundled Data Pipeline Description Language 34

Carsten Nielsen [1], Zhe Su [2], Giacomo Indiveri [2]

[1] Institute of Neuroinformatics, University of Zurich and ETH Zurich and SynSense AG, Zurich, Switzerland
[2] Institute of Neuroinformatics, University of Zurich and ETH Zurich, Zurich, Switzerland

A 28nm Energy-efficient Asynchronous SNN Accelerator with On-chip Learning for Gas Recognition 42

Dexuan Huo, Jilin Zhang, Jian Zhang, Hong Chen

School of Integrated Circuits, Tsinghua University

Chapter 3: Asynchronous Pipelines, Architectures, CPUs, and Circuits

ζ: A Novel Approach for Mitigating Single Event Transient Effects in Quasi Delay Insensitive Logic 48

Zaheer Tabassam, Andreas Steininger, Robert Najvirt, Florian Huemer

Institute for Computer Engineering, TU Wien, Vienna, Austria

Chapter 4: Formal Methods for Verification and Performance/Power Analysis

A QDI Interconnect for 3D Systems Using Industry Standard EDA and Cell Libraries 58

Matheus Trevisan Moreira, William Koven, Tony F. Wu, H. Ekin Sumbul, Edith Beigne

Reality Labs, Meta (Formerly known as Facebook Inc), Menlo Park, CA, USA

Cyclic Timing Path Evaluation Using Commercial Static Timing Analysis Algorithms 60

Mackenzie J. Wibbels, Baudouin Chauviere, Kenneth S. Stevens

University of Utah, Salt Lake City, USA

A Novel Asynchronous Network-On-Chip Based on Source Asynchronous Signaling 71

Venkata Nori, Baudouin Chauviere, Mackenzie J. Wibbels, Kenneth S. Stevens

Department of Electrical and Computer Engineering, University of Utah, Salt Lake City, USA

Verification-Driven Design for Asynchronous VLSI.....78

Xiang Wu, Rajit Manohar

Yale University, New Haven, CT, USA

Chapter 5: Asynchronous Design for Neural Networks and Machine Learning Applications

Core Interface Optimization for Multi-core Neuromorphic Processors 89

Zhe Su [1], Hyunjung Hwang [2], Tristan Torchet [2], Giacomo Indiveri [1]

[1] Institute of Neuroinformatics, University of Zurich and ETH Zurich, Zurich, Switzerland
[2] ETH Zurich, Zurich, Switzerland

An Efficient Data Structure for Sparse Bit-Vectors with Applications in Neuromorphic Computing 99

Prafull Purohit [1], Johannes Leugering [2], Rajit Manohar [1]

[1] Electrical Engineering, Yale University, New Haven, CT, United States
[2] Broadband and Broadcastdept, Fraunhofer Institute for Integrated Circuits (IIS), Erlangen, Germany

Chapter 6: Mixed-timed Circuits, Clock Domain Crossing, GALS Systems, Network-on-chip, and Multi-chip Interconnects

Flexible Compilation and Refinement of Asynchronous Circuits.....109

Ebelechukwu Esimai, Marly Roncken

Asynchronous Research Center and Computer Science Department
Maseeh College of Engineering and Computer Science, Portland State University, Portland, Oregon, USA

Author Index