# 2023 IEEE 41st International Conference on Computer Design (ICCD 2023)

Washington, DC, USA 6-8 November 2023



IEEE Catalog Number: CFP23ICD-POD ISBN: 979-8-3503-4292-5

## Copyright © 2023 by the Institute of Electrical and Electronics Engineers, Inc. All Rights Reserved

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

\*\*\* This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.

 IEEE Catalog Number:
 CFP23ICD-POD

 ISBN (Print-On-Demand):
 979-8-3503-4292-5

 ISBN (Online):
 979-8-3503-4291-8

ISSN: 1063-6404

#### Additional Copies of This Publication Are Available From:

Curran Associates, Inc 57 Morehouse Lane Red Hook, NY 12571 USA

Phone: (845) 758-0400 Fax: (845) 758-2633

E-mail: curran@proceedings.com Web: www.proceedings.com



# 2023 IEEE 41st International Conference on Computer Design (ICCD) ICCD 2023

#### **Table of Contents**

wiessage from the General Chairs xix
Message from the Program Chairsxx
Organizing Committeexxii
Program Committee xxiii
Keynotes xxviii
Sponsorsxxxii
Session 1A: Verification & Security
Leveraging Firmware Reverse Engineering for Stealthy Sensor Attacks via Binary  Modification
A Compressed and Accurate Sparse Deep Learning Based Workload-Aware Timing Error Model9 Styliani Tompazi (Queen's University Belfast, UK) and Georgios Karakonstantis (Queen's University Belfast, UK)
Transcend Adversarial Examples: Diversified Adversarial Attacks to Test Deep Learning  Model
REMU: Enabling Cost-Effective Checkpointing and Deterministic Replay in FPGA-based Emulation
Yuxiao Chen (State Key Lab of Processors, Institute of Computing Technology, CAS, China; University of Chinese Academy of Sciences, China), Yisong Chang (State Key Lab of Processors, Institute of Computing Technology, CAS, China; University of Chinese Academy of Sciences, China), Ke Zhang (State Key Lab of Processors, Institute of Computing Technology, CAS, China; University of Chinese Academy of Sciences, China), Mingyu Chen (State Key Lab of Processors, Institute of Computing Technology, CAS, China; University of Chinese Academy of Sciences, China), and Yungang Bao (State Key Lab of Processors, Institute of Computing Technology, CAS, China; University of Chinese Academy of Sciences, China)

Model Checking TileLink Cache Coherence Protocols By Murphi  Zimin Li (Institute of Software, Chinese Academy of Sciences, China;  Hangzhou Institute for Advanced Study, China), Yongjian Li (Institute of Software, Chinese Academy of Sciences, China), Kaifan Wang (Institute of Computer Technology, Chinese Academy of Sciences, China; Beijing Institute of Open Source Chip, China), Kun Ma (Institute of Software, Chinese Academy of Sciences, China), and Shizhen Yu (Institute of Software, Chinese Academy of Sciences, China)	30
Session 1B: Logic and Circuit Design	
MNHOKA - PPA Efficient M-Term Non-Homogeneous Hybrid Overlap-Free Karatsuba Multiplier for GF (2^n) Polynomial Multiplier	or 38
ApproxCNN: Evaluation Of CNN With Approximated Layers Using In-Exact Multipliers	46
ACET: An Adaptive Clock Scheme Exploiting Comprehensive Timing Slack for Reconfigurable Processors  Shuya Ji (Shanghai Jiao Tong University, China), Weidong Yang (Shanghai Jiao Tong University, China), Jianfei Jiang (Shanghai Jiao Tong University, China), Naifeng Jing (Shanghai Jiao Tong University, China), Weiguang Sheng (Shanghai Jiao Tong University, China), Ang Li (Shanghai Jiao Tong University, China), and Qin Wang (Shanghai Jiao Tong University, China)	54
SFDoP: A Scalable Fused BFloat16 Dot-Product Architecture for DNN  Jing Zhang (National University of Defense Technology, China),  Hongbing Tan (National University of Defense Technology, China), and  Libo Huang (National University of Defense Technology, China)	62
ImprLM: An Improved Logarithmic Multiplier Design Approach via Iterative Linear-Compensation and Modified Dynamic Segment	66
Session 2A: Brain-Inspired Circuits	
MindCrypt: The Brain as a Random Number Generator for SoC-Based Brain-Computer Interfaces ! Guy Eichler (Columbia University, USA), Biruk Seyoum (Columbia University, USA), Kuan-Lin Chiu (Columbia University, USA), and Luca P. Carloni (Columbia University, USA)	70

BrainTTA: A 28.6 TOPS/W Compiler Programmable Transport-Triggered NN SoC	78
Session 2B: Quantum Computing	
HiSEP-Q: A Highly Scalable and Efficient Quantum Control Processor for Superconducting Qubits	86
Xiaorang Guo (Technical University of Munich), Kun Qin (Technical University of Munich), and Martin Schulz (Technical University of Munich; Leibniz Supercomputing Centre, Germany)	JC
Enhancing Virtual Distillation with Circuit Cutting for Quantum Error Mitigation	94
Session 3A: SRAM & NVM	
ICON: An IR Drop Compensation Method at OU Granularity with Low Overhead for eNVM-based Accelerators	)2
Resonant Compute-In-Memory (rCIM) 10T SRAM Macro for Boolean Logic	10
Small Footprint 6T-SRAM Design with MIV-Transistor Utilization in M3D-IC Technology	18
Session 3B: Cache Memory	
Offline and Online Algorithms for Cache Allocation with Monte Carlo Tree Search and a Learned Model	26

Morpheus: An Adaptive DRAM Cache with Online Granularity Adjustment for Disaggregated Memory
Locality-Aware Speculative Cache for Fast Partial Updates in Erasure-Coded Cloud Clusters14: Hai Zhou (Huazhong University of Science and Technology, China), Yuchong Hu (Huazhong University of Science and Technology, China), Dan Feng (Huazhong University of Science and Technology, China), Wei Wang (Hikvision, China), and Huadong Huang (Hikvision, China)
Session 4A: Accelerators
A Cost-Efficient Failure-Tolerant Scheme for Distributed DNN Training 150 Menglei Chen (Huazhong University of Science and Technology, China), Yu Hua (Huazhong University of Science and Technology, China), Rong Bai (Huazhong University of Science and Technology, China), and Jianming Huang (Huazhong University of Science and Technology, China)
RealArch: A Real-Time Scheduler for Mapping Multi-Tenant DNNs on Multi-Core Accelerators 158 Xuhang Wang (Shanghai Jiao Tong University, China), Zhuoran Song (Shanghai Jiao Tong University, China), and Xiaoyao Liang (Shanghai Jiao Tong University, China)
Polyform: A Versatile Architecture for Multi-DNN Execution via Spatial and Temporal  Acceleration

### Session 4B: Persistent Memory

Accelerating Persistent Hash Indexes via Reducing Negative Searches  Renzhi Xiao (Huazhong University of Science and Technology, China),  Hong Jiang (University of Texas at Arlington, USA), Dan Feng (Huazhong University of Science and Technology, China), Yuchong Hu (Huazhong University of Science and Technology, China), Wei Tong (Huazhong University of Science and Technology, China), Kang Liu (Huazhong University of Science and Technology, China), Yucheng Zhang (Huazhong University of Science and Technology, China), Xueliang Wei (Huazhong University of Science and Technology, China), and Zhengtao Li (Huazhong University of Science and Technology, China)	74
PMA: A Persistent Memory Allocator with High Efficiency and Crash Consistency Guarantee 18 Xiangyu Xiang (Huazhong University of Science and Technology, China), Yu Hua (Huazhong University of Science and Technology, China), and Hao Xu (Huazhong University of Science and Technology, China)	32
Prediction-Guided Metadata Backup for Improving Lifetime on Flash-based Swap	<del>}</del> 0
RWORT: A Read and Write Optimized Radix Tree for Persistent Memory	94
Session 5A: Storage	
	98
Session 5A: Storage  An Effective and Balanced Storage Extension Approach for Sharding Blockchain Systems	

## Session 5B: Memory Systems

PANG: A Pattern-Aware GCN Accelerator for Universal Graphs  Yibo Du (CICS, Institute of Computing Technology, Chinese Academy of Sciences, China; University of Chinese Academy of Sciences, China), Ying Wang (CICS, Institute of Computing Technology, Chinese Academy of Sciences, China; University of Chinese Academy of Sciences, China), Shengwen Liang (SKLP, Institute of Computing Technology, Chinese Academy of Sciences, China; University of Chinese Academy of Sciences, China), Huawei Li (SKLP, Institute of Computing Technology, Chinese Academy of Sciences, China; University of Chinese Academy of Sciences, China; Peng Cheng Laboratory, China), Xiaowei Li (SKLP, Institute of Computing Technology, Chinese Academy of Sciences, China; University of Chinese Academy of Sciences, China), and Yinhe Han (CICS, Institute of Computing Technology, Chinese Academy of Sciences, China; University of Chinese Academy of Sciences, China; Zhejiang Lab, China)	53
Session 6B: File Systems	
HyF2FS: A Filesystem to Fully Exploit the Parallelism of Hybrid Storage	57
SMRTS: A Performance and Cost-Effectiveness Optimized SSD-SMR Tiered File System with Data Deduplication	<sup>7</sup> 5
Low-Latency and Scalable Full-Path Indexing Metadata Service for Distributed File Systems 28 Chao Dong (Huazhong University of Science and Technology, China), Fang Wang (Huazhong University of Science and Technology, China), Yuxin Yang (Huazhong University of Science and Technology, China), Mengya Lei (Huazhong University of Science and Technology, China), Jianshun Zhang (Huazhong University of Science and Technology, China), and Dan Feng (Huazhong University of Science and Technology, China)	33
Session 7A: SSDs	
FlexZNS: Building High-Performance ZNS SSDs with Size-Flexible and Parity-Protected Zones 29 Yu Wang (Huazhong University of Science and Technology, China), You Zhou (Huazhong University of Science and Technology, China), Zhonghai Lu (KTH Royal Institute of Technology, Sweden), Xiaoyi Zhang (Alibaba Group, China), Kun Wang (Alibaba Group, China), Feng Zhu (Alibaba Group, China), Shu Li (Alibaba Group, China), Changsheng Xie (Huazhong University of Science and Technology, China), and Fei Wu (Huazhong University of Science and Technology, China)	)1

LifetimeKV: Narrowing the Lifetime Gap of SSTs in LSMT-based KV Stores for ZNS SSDs300 Biyong Liu (Huazhong University of Science & Technology, China), Yuan Xia (Huazhong University of Science & Technology, China), Xueliang Wei (Huazhong University of Science & Technology, China), and Wei Tong (Huazhong University of Science & Technology, China)
Persimmon: An Append-Only ZNS-First Filesystem
Turn Waste Into Wealth: Alleviating Read/Write Interference in ZNS SSDs
Session 7B: Logic Synthesis
GPT-LS: Generative Pre-Trained Transformer with Offline Reinforcement Learning for Logic Synthesis
Delay-Driven Physically-Aware Logic Synthesis with Informed Search
Adaptive Reconvergence-Driven AIG Rewriting via Strategy Learning
University, China)

#### Session 8A: GPU II

FlexGM: An Adaptive Runtime System to Accelerate Graph Matching Networks on GPUs
NTTFusion: Efficient Number Theoretic Transform Acceleration on GPUs  Zhiwei Wang (State Key Laboratory of Information Security, Institute of Information Engineering, CAS, China; University of Chinese Academy of Sciences, China), Peinan Li (State Key Laboratory of Information Security, Institute of Information Engineering, CAS, China), Rui Hou (State Key Laboratory of Information Security, Institute of Information Engineering, CAS, China), and Dan Meng (State Key Laboratory of Information Security, Institute of Information Engineering, CAS, China)
MixRec: Orchestrating Concurrent Recommendation Model Training on CPU-GPU Platform 366  Jiazhi Jiang (Sun Yat-sen University, China), Rui Tian (Sun Yat-sen  University, China), Jiangsu Du (Sun Yat-sen University, China), Dan  Huang (Sun Yat-sen University, China), and Yutong Lu (Sun Yat-sen  University, China)
Session 8B: Accelerators
HyAcc: A Hybrid CAM-MAC RRAM-based Accelerator for Recommendation Model
ViTframe: Vision Transformer Acceleration via Informative Frame Selection for Video Recognition
ACCO: Automated Causal CNN Scheduling Optimizer for Real-Time Edge Accelerators
Session 9A: Co-Design

Re-Compact: Structured Pruning and SpMM Kernel Co-Design for Accelerating DNNs on GPUs .. 399 Yuling Zhang (Chongqing University, China), Ao Ren (Chongqing University, China), Xianzhang Chen (Chongqing University, China), Qiu Lin (Chongqing University, China), Yujuan Tan (Chongqing University, China), and Duo Liu (Chongqing University, China)

FLASH-RL: Federated Learning Addressing System and Static Heterogeneity using Reinforcement Learning	
Session 10A: Matrix Multiplication & Sparsity	
PrSpMV: An Efficient Predictable Kernel for SpMV	
Releasing the Potential of Tensor Core for Unstructured SpMM using Tiled-CSR Format	
Tailoring CUTLASS GEMM using Supervised Learning	
Session 10B: Fault Tolerance & Resilience	
Revitalizing Buffered I/O: Optimizing Page Reclaim and I/O Throttling	
ResCheck: Resilient Checkpointing for Energy Harvesting Systems	
Heart: A Scalable, High-Performance ART for Persistent Memory	

DCR: Decomposition-Aware Column Re-Mapping for Stuck-At-Fault Tolerance in ReRAM Arrays 191
Hyeonsu Bang (Sungkyunkwan University, South Korea), Kang Eun Jeon (Sungkyunkwan University, South Korea), Johnny Rhe (Sungkyunkwan University, South Korea), and Jong Hwan Ko (Sungkyunkwan University, South Korea)
Snapshot: Fast, Userspace Crash Consistency for CXL and PM Using Msync
Session 11A: Processing-In-Memory
GIM: Versatile GNN Acceleration with Reconfigurable Processing-in-Memory
PSQ: An Automatic Search Framework for Data-Free Quantization on PIM-based Architecture 507 Fangxin Liu (Shanghai Jiao Tong University, China; Shanghai Qi Zhi Institute, China), Ning Yang (Shanghai Jiao Tong University, China; Shanghai Qi Zhi Institute, China), and Li Jiang (Shanghai Jiao Tong University, China; Shanghai Qi Zhi Institute, China)
Exploiting and Enhancing Computation Latency Variability for High-Performance Time-Domain Computing-in-Memory Neural Network Accelerators
Input-Aware Flow-Based In-Memory Computing
BICEP: Exploiting Bitline Inversion for Efficient Operation-Unit-Based Compute-in-Memory Architecture: No Retraining Needed!
Cerasure: Fast Acceleration Strategies For XOR-Based Erasure Codes  Tianyang Niu (University of Science and Technology of China), Min lyu  (University of Science and Technology of China), Wei Wang (University  of Science and Technology of China), Qiliang Li (University of Science  and Technology of China), and Yinlong Xu (University of Science and  Technology of China)

### **Session 11B: Electronic Design Automation**

A DSP Shared is a DSP Earned: HLS Task-Level Multi-Pumping for High-Performance Low-Resource Designs	
Efficient RISC-V-on-x64 Floating Point Simulation  Niko Zurstraßen (RWTH Aachen University), Nils Bosbach (RWTH Aachen University), Jan Moritz Joseph (RWTH Aachen University), Lukas Jünger (MachineWare GmbH), Jan Henrik Weinstock (MachineWare GmbH), and Rainer Leupers (RWTH Aachen University)	558
HF-LDPC: HLS-Friendly QC-LDPC FPGA Decoder with High Throughput and Yifan Zhang (Huazhong University of Science and Technology, China), Qiang Cao (Huazhong University of Science and Technology, China), Shaohua Wang (Huazhong University of Science and Technology, China), Jie Yao (Huazhong University of Science and Technology, China), and Hong Jiang (University of Texas at Arlington)	Flexibility 566
GNNHLS: Evaluating Graph Neural Network Inference via High-Level Synthes Chenfeng Zhao (Washington University in St. Louis), Zehao Dong (Washington University in St. Louis), Yixin Chen (Washington University in St. Louis), Xuan Zhang (Washington University in St. Louis), and Roger Chamberlain (Washington University in St. Louis)	sis 574
Session 12A: Test & Verification	
Architectural Contracts for Safe Speculation  Franz A. Fuchs (University of Cambridge, UK), Jonathan Woodruff (University of Cambridge, UK), Peter Rugg (University of Cambridge, UK), Marno van der Maas (University of Cambridge, UK), Alexandre Joannou (University of Cambridge, UK), Jessica Clarke (University of Cambridge, UK), Jessica Clarke (University of Cambridge, UK), Nathaniel Wesley Filardo (Microsoft Research Ltd, UK), Brooks Davis (SRI International, USA), John Baldwin (Ararat River Consulting, USA), Peter G. Neumann (SRI International, USA), Simon W. Moore (University of Cambridge, UK), and Robert N. M. Watson (University of Cambridge, UK)	578

Execute on Clear (EoC): Enhancing Security for Unsafe Speculative Instructions by Precise  Identification and Safe Execution	•
RunSAFER: A Novel Runtime Fault Detection Approach for Systolic Array Accelerators	
Session 12B: Compression & Accelerators	
BIRD: A Lightweight and Adaptive Compressor for Communication-Efficient Distributed Learning Using Tensor-Wise Bi-Random Sampling	;
MultiFuse: Efficient Cross Layer Fusion for DNN Accelerators with Multi-Level Memory Hierarchy	•
DEQ: Dynamic Element-Wise Quantization for Efficient Attention Architecture	,
CNN Inference Accelerators with Adjustable Feature Map Compression Ratios	
Author Index	