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[1]Sungkyunkwan University, Korea
[2]Samsung Electronics Co., Ltd, Korea

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[1]Incheon National University, Korea
[2]Bellarmine College Preparatory, USA

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Chair: Min-Jae Seo (Gachon University, Korea)

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[1]Daegu Gyeongbuk Institute of Science & Technology(DGIST), Korea
[2]Ulsan National Institute of Science & Technology (UNIST), Korea
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[1]SK Hynix Inc., Korea
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[1]TU Dresden, Germany
[2]Racyics GmbH Dresden, Germany

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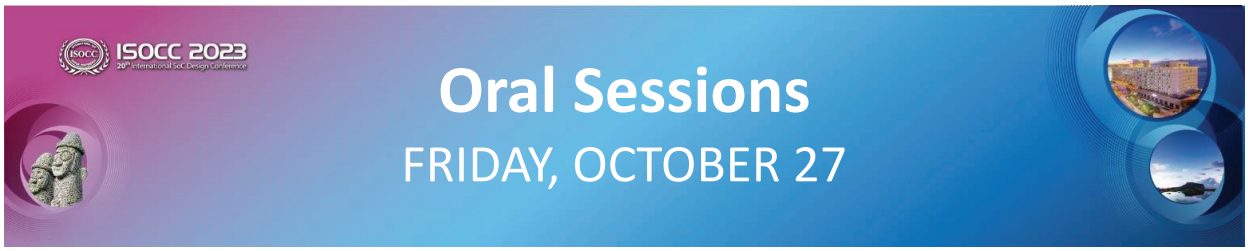

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[1]National Yunlin University of Science and Technology, Taiwan
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Grand Ballroom2 (2F)

SS1 Advancements in Intelligent System Semiconductors

Organizer: Prof. Sung-Wan Hong (Sogang University, Korea)

Abstract: The special session on "Advancements in Intelligent System Semiconductors" focuses on the latest developments in both hardware and software aspects of intelligent system semiconductors. This session explores cutting-edge innovations in hardware architectures, chip designs, intelligent SoC solutions, algorithms, and deep learning frameworks. The session aims to facilitate knowledge exchange, collaboration, and discussion on challenges and opportunities in the field, while promoting advancements in intelligent system semiconductors for diverse real-world applications.

Chair: Sung-Wan Hong (Sogang University, Korea)

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SS2 Hardware and software design techniques for AI processing platforms

Organizers: Prof. Won-Young Lee (Seoul National University of Science and Technology, Korea)

Abstract: In recently years, artificial intelligence (AI) is known as the core driving force of the next industrial revolution, and its applications have been advanced in many fields such as computer vision, language understanding, auto-driving, and robotics. Since AI software has grown in complexity, demands on reliable and high performance computing systems consistently are growing. Therefore, the advanced hardware and software techniques beyond von Neumann computers have been studied for AI processing platform to execute AI algorithms at reasonable speed. In this special session, five papers will discuss emerging techniques for enhancements of AI processing platforms regarding AI algorithm, processing architecture, hardware implementation and software development.

Chair: Won-Young Lee (Seoul National University of Science and Technology, Korea)

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SS3 Circuits, Systems, and Devices for Optical Communication Technology for 6G and Beyond Future Communications

Organizers: Prof. Shintaro Arai (Okayama University of Science, Japan)
Prof. Byung Wook Kim (Changwon National University, Korea)

Abstract: This special session will discuss the optical wireless and wired communication technologies required to realize the 6th generation mobile communication systems (6G) and beyond future communication systems, focusing on the device circuits and hardware implementations that form the basis of these technologies. Communication technologies, especially mobile communication technology systems, have been evolving decade by decade, and we can now use the 5th generation mobile communication system (5G) services. The next generation system is 6G, which is currently being researched and developed worldwide for introduction in the 2030s. In order to realize 6G while effectively using radio waves, it is essential to not only rely on radio waves but also to combine them with optical wireless and wired communication technologies. We have conceived this special session to discuss the characteristics of each transmission medium and how they can be utilized to realize 6G.

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SS4 Simulation and Analysis for Nonlinear Problems

Organizer: Prof. Hiroo Sekiya (Chiba University, Japan)

Abstract: Nonlinearity introduces complexity to the behavior of a system. However, this complexity can hold various benefits, such as enabling intelligent information processing. Circuits are one example of physical systems that exhibit nonlinear behavior. Their high reproducibility makes them effective tools for investigating the nature of nonlinearity.
The purpose of this special session is to discuss the latest techniques for simulating and analyzing nonlinear phenomena. The discussions in this session are applicable not only for understanding the essence of nonlinear phenomena but also for designing real circuit systems geared towards nonlinear applications.

Chair: Hiroo Sekiya (Chiba University, Japan)

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[1]Chukyo University, Japan
[2]Okayama University of Science, Japan

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Jiaying Lin[1], Ryuji Nagazawa[1], Kien Nguyen[1], Hiroo Sekiya[1], Mikio Hasegawa[2], Hiroyuki Torikai[3], and Won-Joo Hwang[4]
[1]Chiba University, Japan
[2]Tokyo University of Science, Japan
[3]Hosei University, Japan
[4]Pusan National University, Korea

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[1]Chiba University, Japan
[2]Chiba Institute of Technology, Japan

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Tokushima University, Japan

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A hardware-efficient wireless functional electrical stimulation system based on ergodic cellular automaton dynamics...169
Masaya Kudo, and Hiroyuki Torikai
Hosei University, Japan

SS5 Emerging Techniques in Algorithm and Architecture for Advanced High-Performance Circuit Design

Organizers: Prof. Yuan-Ho Chen (Chang Gung University, Taiwan)
Prof. Chung-Yi Li (Chang Gung University, Taiwan)

Abstract: As artificial intelligence (AI) applications continue to grow, there is an increasing need for advanced algorithms and architectures in high-performance circuit designs. Our conference delves into topics such as quantum-inspired annealing, heart disease recognition via lightweight convolutional neural networks, hybrid CNN-LSTM networks for ECG classification, and novel driver architectures for power converters, aiming to boost the execution speed of edge AI devices while reducing hardware costs and power consumption. Through the exploration of suitable algorithmic and architectural schemes, we seek to simplify neural network operations, consequently leading to improvements in area and energy efficiency in hardware acceleration designs.

Chair: Yuan-Ho Chen (Chang Gung University, Taiwan)

15:00~16:30, THURSDAY_OCTOBER 26, 2023

Mara Hall (2F)

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[1]Chang Gung University, Taiwan
[2]Institute for Information Industry, Taiwan
[3]Chang Gung Memorial Hospital, Taiwan

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Song-Nien Tang[1], Yuan-Ho Chen[2], Yu-Wei Chang[1], Yu-Ting Chen[1], and Shuo-Hung Chou[1]

[1]Chung Yuan Christian University, Taiwan
[2]Chang Gung University, Taiwan

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Chang Gung University, Taiwan

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[1]National Yunlin University of Science and Technology, Taiwan
[2]National Formosa University, Taiwan
[3]Nanhua University, Taiwan

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Chung-Yi Li[1,2], Tzu-Yu Chen[1], Deng-fong Lu[1], Yue-Liang Chou[3], Hung-Chi Chen[3], and Shinn-Yn Lin[2]

[1]Chang Gung University, Taiwan
[2]Chang Gung Memorial Hospital, Taiwan
[3]National Yang Ming Chiao Tung University, Taiwan

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Ying-Hsiu Hung[1,2], Yen-Ching Chang[2], Szu-Ting Wang[1], Jeng-Dao Lee[1], Wen-Ho Juang[1], Ming-Hwa Sheu[2], and Shin-Chi Lai[1]

[1]*National Formosa University, Taiwan*
[2]*National Yunlin University of Science and Technology, Taiwan*

SS6 Design, Analysis and Tools for Integrated Circuits and Systems (DATICS)

Organizers: Prof. Ka Lok Man (Xi'an Jiaotong-Liverpool University, China)

Abstract: DATICS workshops/special sessions were initially created by a network of researchers and engineers both from academia and industry in the areas of Design, Analysis and Tools for Integrated Circuits and Systems (DATICS). The proposed DATICS-ISOCC'23 special session will focus on emerging Circuits and Systems (CAS) topics that will strongly lead human life revolutions, especially in CMOS technologies, communication technologies and biomedical technologies. Human life revolutions come along with economic opportunities. The market for these emerging
topics is also forecast to grow to a multi-billion dollar market in the coming decade. The special session will highlight the potential and current developments of these CAS topics, along with pressing challenges. The proposed session is coherent and complementary to the conference theme and areas of interest of ISOCC. The main target of DATICS-ISOCC'23 is to bring together engineering researchers and people from industry to exchange theories, ideas, techniques and experiences. In addition, DATICS Yearly Special Session has been carried out at ISOCC since 2012.

Chair: Ka Lok Man (Xi'an Jiaotong-Liverpool University, China)

15:00~16:45, THURSDAY_OCTOBER 26, 2023

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[1]Polytechnic University of Bari, Italy
[2]Xi'an Jiaotong-Liverpool University, China

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Sogang University, Korea

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[1]Xi'an Jiaotong-Liverpool University, China
[2]University of Liverpool, United Kingdom

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Yu Du[1], Ka Lok Man[1], Jeremy S. Smith[2], and Eng Gee Lim[1]

[1]*Xi'an Jiaotong-Liverpool University, China*
[2]*University of Liverpool, United Kingdom*

SS7 Emerging techniques for neuromorphic, non-linear, and bio-sensing circuits and systems

Organizer: Prof. Kyeong-Sik Min (Kookmin University, Korea)
Prof. Hyunsun Mo (Kookmin University, Korea)

Abstract: In this special session, emerging techniques of neuromorphic, neural networks, non-linear circuits, bio-sensing techniques, and so on are discussed and presented. Based on emerging devices such as memristors, potential hardware solutions are presented for implementing neuromorphic and neural network systems. For deep understanding of brain-mimicking circuits, a non-linear analytic method is shared and discussed at the session. And new bio-sensing techniques are presented and explained for future applications of health care systems.

Chair: Kyeong-Sik Min (Kookmin University, Korea)

13:00~14:00, FRIDAY _OCTOBER 27, 2023

Grand Ballroom4 (2F)

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Hyunsun Mo, Jungho Joo, Youngsu Hwang, Hyoyuong Park, Minsoo Kim, Dae Hwan Kim, and Daejeong Kim

Kookmin University, Korea

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Yoko Uwate and Yoshifumi Nishio

Tokushima University, Japan

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Seokjin Oh, Rina Yoon, Seungmyeong Cho, and Kyeong-Sik Min

Kookmin University, Korea

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Jerald Yoo[1,2]

[1]National University of Singapore, Singapore
[2]The N.1 Institute for Health, Singapore

SS8 Circuits and Systems for Artificial Intelligence and Homomorphic Encryption

Organizer: Prof. Hanho Lee (Inha University, Korea)

Abstract: Artificial intelligence (AI) and homomorphic encryption are playing an increasingly crucial role in the IoT, 5G/6G, and smart mobility applications, and they have also become the fundamental components of modern intelligent society. The applications of AI and homomorphic encryption for IoT, 5G/6G and smart mobility need to be portable, lightweight, low-latency and high-speed to provide reliable service. Meanwhile, massive devices connected to the edge of communication networks should be post-quantum safe and secure, because emerging quantum computers can easily crack the traditional public-key ciphers. To meet the requirements of high-throughput and diverse application scenarios of next-generation communications and autonomous mobility, it is necessary to resort to configurable and low-latency algorithms and architectures of AI and homomorphic encryption. The high-performance, low-latency domain specific architecture has become a trend of circuits and systems design in the post-Moore era, which can also be applied to the AI and security in a wide range of applications.

Chair: Hanho Lee (Inha University, Korea)

13:00~14:15, FRIDAY _OCTOBER 27, 2023

Mara Hall (2F)

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Ulsan National Institute of Science & Technology (UNIST), Korea

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Inha University, Korea

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Sungkyunkwan University, Korea

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Chulwoo Lee, Hanyoung Lee, Phap Duong-Ngoc, and Hanho Lee
Inha University, Korea

SS8-5 (237)
14:00-14:15
Optimizing Image Classification with Inverse Depthwise Separable Convolution for Edge Devices...211
Akshay Kumar Sharma, and Kyung Ki Kim
Daegu University, Korea

SS9 Chiplet Heterogeneous Integration Technology

Organizer: Dr. Youngsu Kwon (Electronics and Telecommunications Research Institute, Korea)

Abstract: Artificial Intelligence is advancing towards achieving superhuman intelligence. Hyperscale transformer neural networks with billions of parameters are gaining immense interest and penetrating a wide range of applications, as their AI performance far exceeds that of previous networks. The training and inference of these hyper-AI models require a new computing paradigm called Data explosion computing, which demands AI computers composed of widescale parallelized AI NPUs, Neural Processing Units. The Chiplet AI processor architecture is the most viable semiconductor solution for hyperscale AI, enabling the chip to accommodate multiple NPUs in tandem with a multitude of high-throughput memories for hyperscale AI performance. This special session presents researches on the AI processor's Chiplet architecture design, 2.5D and 3D integration process, Signal Integrity, Power Integrity, Thermal Integrity, and Thermomechanical Analysis of Chiplet Processors on Advanced Packaging.

Chair: Youngsu Kwon (Electronics and Telecommunications Research Institute, Korea)

13:00~14:45, FRIDAY _OCTOBER 27, 2023

Udo Hall (2F)

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Jiwon Yoon[1], Hyunwoo Kim[1], Boogyo Sim[1], Hyunwook Park[2], Yigyeong Kim[3], Sujin Park[3], Youngsu Kwon[3], and Joungho Kim[1]

[1]*Korea Advanced Institute of Science and Technology (KAIST), Korea*
[2]*Missouri University of Science and Technology (MST), USA*
[3]*Electronics and Telecommunications Research Institute (ETRI), Korea*

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Sujin Park, Young-Deuk Jeon, Yi-Gyeong Kim, Min-Hyung Cho, Jinho Han, Jaehoon Chung, Jaewoong Choi, and Youngsu Kwon

Electronics and Telecommunications Research Institute (ETRI), Korea

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Youngsu Kwon

Electronics and Telecommunications Research Institute (ETRI), Korea

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Jae Young Hwang[1], Hakjun Kim[1], Young-Chang Joo[1], Hyejin Jang[1], Sangwoo Park[2], and Sarah Eunkyung Kim[2]

[1]*Seoul National University, Korea*
[2]*Seoul National University of Science and Technology, Korea*

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Yong-Nam Koh, Ju-Hyung Kim, Soo-Jeong Kim, Ju-Hwan Jang, Jae-Sung Lim, and Jayden Donghyun Kim

HANA Micron, Inc., Korea

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Seoul National University of Science and Technology, Korea

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Ruhan E. Ustad[1], Honggyun Kim[1], Vijay D. Chavan[1], Kyeong-Keun Choi[2], and Deok-kee Kim[1]

[1]*Sejong University, Korea*
[2]*Pohang University of Science and Technology(POSTECH), Korea*

SS10 Design and Analysis of Nonlinear Circuits and Networks

Organizer: : Prof. Yoshifumi Nishio (Tokushima University, Japan)

Abstract: In recent years, nonlinear circuits and networks become more and more important, because intelligent and flexible systems for future electronic systems require complex nonlinear circuits and networks. From the beginning of the 20th century, plenty of simulation and analysis methods for nonlinear circuits and networks have been developed over 100 years. However, we need more powerful tools to design low cost power electronic circuits, to analyze large scale complex nonlinear networks, and to realize more intelligent artificial neural networks. In this special session, 6 papers are invited to show examples of recent works on simulation and analysis of such nonlinear circuits and networks.

Chair: Yoshifumi Nishio (Tokushima University, Japan)

14:30~16:00, FRIDAY _OCTOBER 27, 2023

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Hosei University, Japan

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Takahiro Hattori, Yoko Uwate, and Yoshifumi Nishio
Tokushima University, Japan

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Hosei University, Japan

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Tokushima University, Japan

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Tokushima University, Japan

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Yuki Matsubara, Yuki Ishikawa, Yoko Uwate, and Yoshifumi Nishio
Tokushima University, Japan

SS11 Enabling High Performance Ultra-Dense Storage Systems

Organizer: Prof. Chun-Feng Wu (National Yang Ming Chiao Tung University, Taiwan)
Prof. Yi-Shen Chen (National Taiwan University of Science and Technology, Taiwan)

Abstract: In the era of big data, cloud providers like Google Cloud and Microsoft Azure consistently require large amounts of inexpensive storage capacity to accommodate as many data as possible. To meet this demand, non-volatile devices such as Solid State Drives (SSDs) and Shingled Magnetic Recording (SMR) drives are extensively employed to expand storage capabilities. For instance, cloud providers configure SSDs as swap areas to effectively extend DRAM-based main memory at a lower cost. Additionally, they also substitute conventional Hard Disk Drives (HDDs) with SMR drives to increase storage capacity at a reduced price. However, the trade-off of performance is always a concern when using non-volatile devices to expand memory and storage capacity. In light of this, we are motivated to organize a special session that focuses on "Enabling High Performance Ultra-Dense Storage Systems" to explore ways of achieving the best of both worlds: large capacity and high performance.

Chair: Chun-Feng Wu (National Yang Ming Chiao Tung University, Taiwan)

14:30~16:00, FRIDAY _OCTOBER 27, 2023

Grand Ballroom4 (2F)

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Yong-Cheng Liaw[1], Shuo-Han Chen[1], and Hsin-Yun Su[2]
[1]National Yang Ming Chiao Tung University, Taiwan
[2]National Taipei University of Technology, Taiwan

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[1]National Taipei University of Technology, Taiwan
[2]National Yang Ming Chiao Tung University, Taiwan

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Yi-Shen Chen, Ying-Jui Shih, and Jen-Wei Hsieh
National Taiwan University of Science and Technology, Taiwan

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Lee Chang[1], Chien-Chung Ho[2], and Tei-Wei Kuo[1,3]
[1]National Taiwan University, Taiwan
[2]National Cheng Kung University, Taiwan
[3]Mohamed bin Zayed University of Artificial Intelligence, United Arab Emirates

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[1]National Tsing Hua University, Taiwan
[2]National Chung Cheng University, Taiwan
[3]National Taiwan University, Taiwan
[4]Institute of Information Science, Taiwan

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Yi-Syuan Lin[1], Chin-Yu Lo[2], Yi-Chao Shih[1], and Tseng-Yi Chen[3]

[1]National Tsing Hua University, Taiwan
[2]Yuan Ze University, Taiwan
[3]National Central University, Taiwan

SS12 Bio-Inspired Computation in Circuits and Systems

Organizer: Prof. Yoko Uwate (Tokushima University, Japan)

Abstract: Bio-inspired computing has recently been attracting attention in the field of engineering research. Algorithms and systems inspired by living organisms, rather than conventional mathematical methods, have been shown to be effective for large-scale optimization problems. In this special session, we will present several biological computing research results toward circuit models. One is an investigation of synchronization phenomena in circuit systems using memristors for coupling. Next is a study of reservoir computing. Reservoir neural networks learn only the weights of the reservoir and output layers, so they can reduce the power consumption of the circuit. Further research on circuit models of cochlear and analog neuron models will be presented. Research on the development of bioinspired computing circuits is very important for the future engineering applications.

Chair: Yoko Uwate (Tokushima University, Japan)

14:30~15:45, FRIDAY _OCTOBER 27, 2023

Mara Hall (2F)

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Yukinojo Kotani, Yoko Uwate and Yoshifumi Nishio

Tokushima University, Japan

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Yui Kishimoto, and Hiroyuki Torikai

Hosei University, Japan

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Kengo Hosoi, and Hiroyuki Torikai

Hosei University, Japan

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Haruki Terakawa[1], Hideyuki Kato[1], Yoshihiro Yonemura[2], and Yuichi Katori[2]

[1]*Oita University, Japan*

[2]*Future University Hakodate, Japan*

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15:30-15:45

A Study of Changes in Prediction Performance Influenced by Attractor State in Oscillator Reservoir Computing...259

Kazuki Yasufuku, Yoko Uwate, and Yoshifumi Nishio

Tokushima University, Japan

Poster Session

Chair: Jungrae Kim (Sungkyunkwan University, Korea)

Standing Time 09:45~10:25, FRIDAY OCTOBER 27, 2023

Exhibition Time 10:25~16:00, FRIDAY OCTOBER 27, 2023

Ballroom Lobby (2F)

Analog Circuits

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Jaehun Jeong, Jonghyuk Chae, Seungju Lee, and Jinwook Burm
Sogang University, Korea

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Jonghyuk Chae, Jaehun Jeong, Byeongha Park, Jinwook Burm
Sogang University, Korea

PS-3 (115) **An Analog Integrate-and-Fire Neuron with Robust Soft Reset Mechanism...265**
Jia Park, and Woo-Seok Choi
Seoul National University, Korea

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Electrical and Electronics Engineering Institute University of the Philippines Diliman, Philippines

PS-5 (117) **A high CMRR, high input impedance current-feedback instrumentation amplifier (CFIA) in 22-nm UTBB FD-SOI for signal conditioning of MEMS piezoresistive pressure sensors...269**
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Electrical and Electronics Engineering Institute University of the Philippines Diliman, Philippines

Circuits and Systems for Emerging Technologies

Data Converters

Digital Circuits, Architecture, and Systems

Machine Learning and AI

SoC Design Methodology and CAD

Wireline