

2019 24th Asia and South Pacific Design Automation Conference (ASP-DAC 2019)

**Tokyo, Japan
21 – 24 January 2019**



**IEEE Catalog Number: CFP19ASP-POD
ISBN: 978-1-5386-8268-5**

**Copyright © 2019, Association for Computing Machinery (ACM)
All Rights Reserved**

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

| | |
|-------------------------|-------------------|
| IEEE Catalog Number: | CFP19ASP-POD |
| ISBN (Print-On-Demand): | 978-1-5386-8268-5 |
| ISBN (Online): | 978-1-4503-6007-4 |
| ISSN: | 2153-6961 |

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

TABLE OF CONTENTS

| | |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| A Wide Conversion Ratio, 92.8% Efficiency, 3-Level Buck Converter with Adaptive On/Off-Time Control and Shared Charge Pump Intermediate Voltage Regulator..... | 1 |
| <i>Kousuke Miyaji, Yuki Karasawa, Takanobu Fukuoka</i> | |
| Towards Cognitive Obfuscation: Impeding Hardware Reverse Engineering Based on Psychological Insights | 3 |
| <i>Carina Wiesen, Nils Albartus, Max Hoffmann, Steffen Becker, Sebastian Wallat, Marc Fyrbiak, Nikol Rummel, Christof Paar</i> | |
| A Low-Voltage CMOS Electrophoresis IC using Electroless Gold Plating for Small-Form-Factor Biomolecule Manipulation | 11 |
| <i>Kiichi Niitsu, Yuuki Yamaji, Atsuki Kobayashi, Kazuo Nakazato</i> | |
| Insights into the Mind of a Trojan Designer: The Challenge to Integrate a Trojan into the Bitstream | 13 |
| <i>Maik Ender, Pawel Swierczynski, Sebastian Wallat, Matthias Wilhelm, Paul Martin Knopp, Christof Paar</i> | |
| GraphSAR: A Sparsity-Aware Processing-in-Memory Architecture for Large-Scale Graph Processing on ReRAMs..... | 21 |
| <i>Guohao Dai, Tianhao Huang, Yu Wang, Huazhong Yang, John Wawrzyniek</i> | |
| ParaPIM: A Parallel Processing-In-Memory Accelerator for Binary-Weight Deep Neural Networks | 28 |
| <i>Shaahin Angizi, Zhezhi He, Deliang Fan</i> | |
| A Low-Voltage Low-Power Multi-Channel Neural Interface IC using Level-Shifted Feedback Technology | 34 |
| <i>Liangjian Lyu, Yu Wang, Chixiao Chen, C.-J. Richard Shi</i> | |
| CompRRAE: RRAM-Based Convolutional Neural Network Accelerator with Reduced Computations Through a Runtime Activation Estimation..... | 36 |
| <i>Xizi Chen, Jingyang Zhu, Jingbo Jiang, Chi-Ying Tsui</i> | |
| CuckooPIM: An Efficient and Less-Blocking Coherence Mechanism for Processing-In-Memory Systems..... | 43 |
| <i>Sheng Xu, Xiaoming Chen, Ying Wang, Yinhe Han, Xiaowei Li</i> | |
| AERIS: Area/Energy-Efficient 1T2R ReRAM Based Processing-In-Memory Neural Network System-on-a-Chip..... | 49 |
| <i>Jinshan Yue, Yongpan Liu, Fang Su, Shuangchen Li, Zhe Yuan, Zhibo Wang, Wenyu Sun, Xueqing Li, Huazhong Yang</i> | |
| Development of a High Stability, Low Standby Power Six-Transistor CMOS SRAM Employing a Single Power Supply | 55 |
| <i>Nobuaki Kobayashi, Tadayoshi Enomoto</i> | |
| IR-ATA: IR Annotated Timing Analysis, a Flow for Closing the Loop Between PDN Design, IR Analysis & Timing Closure | 57 |
| <i>Ashkan Vakil, Houman Homayoun, Avesta Sasan</i> | |
| Learning-Based Prediction of Package Power Delivery Network Quality | 65 |
| <i>Yi Cao, Andrew B. Kahng, Joseph Li, Abinash Roy, Vaishnav Srinivas, Bangqi Xu</i> | |

| | |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| Tackling Signal Electromigration with Learning-Based Detection and Multistage Mitigation..... | 72 |
| <i>Wei Ye, Mohamed Baker Alawieh, Yibo Lin, David Z. Pan</i> | |
| Design of Heterogeneously-Integrated Memory System with Storage Class Memories and NAND Flash Memories | 78 |
| <i>Chihiro Matsui, Ken Takeuchi</i> | |
| ROBIN: Incremental Oblique Interleaved ECC for Reliability Improvement in STT-MRAM Caches | 80 |
| <i>Elham Cheshmikhani, Hamed Farbeh, Hossein Asadi</i> | |
| Aging-Aware Chip Health Prediction Adopting an Innovative Monitoring Strategy | 86 |
| <i>Yun-Ting Wang, Kai-Chiang Wu, Chung-Han Chou, Shih-Chieh Chang</i> | |
| Compiling SU(4) Quantum Circuits to IBM QX Architectures | 92 |
| <i>Alwin Zulehner, Robert Wille</i> | |
| A 65-nm CMOS Fully-Integrated Circulating Tumor Cell and Exosome Analyzer using an On-Chip Vector Network Analyzer and a Transmission-Line-Based Detection Window | 98 |
| <i>Taiki Nakanishi, Maya Matsunaga, Shunya Murakami, Atsuki Kobayashi, Kiichi Niitsu</i> | |
| Quantum Circuit Compilers using Gate Commutation Rules..... | 100 |
| <i>Toshinari Itoko, Rudy Raymond, Takashi Imamichi, Atsushi Matsuo, Andrew W. Cross</i> | |
| Scalable Design for Field-Coupled Nanocomputing Circuits | 106 |
| <i>Marcel Walter, Robert Wille, Frank Sill Torres, Daniel Große, Rolf Drechsler</i> | |
| BDD-Based Synthesis of Optical Logic Circuits Exploiting Wavelength Division Multiplexing..... | 112 |
| <i>Ryosuke Matsuo, Jun Shiomi, Tohru Ishihara, Hidetoshi Onodera, Akihiko Shinya, Masaya Notomi</i> | |
| Low Standby Power CMOS Delay Flip-Flop with Data Retention Capability | 119 |
| <i>Nobuaki Kobayashi, Tadayoshi Enomoto</i> | |
| Hybrid Binary-Unary Hardware Accelerator..... | 121 |
| <i>S. Rasoul Faraji, Kia Bazargan</i> | |
| Fault Tolerance in Neuromorphic Computing Systems | 127 |
| <i>Mengyun Liu, Lixue Xia, Yu Wang, Krishnendu Chakrabarty</i> | |
| Build Reliable and Efficient Neuromorphic Design with Memristor Technology | 135 |
| <i>Bing Li, Bonan Yan, Chenchen Liu, Haihelen Li</i> | |
| Accelerate Pattern Recognition for Cyber Security Analysis | 141 |
| <i>Mohammad Tahghighi, Wei Zhang</i> | |
| Reliable In-Memory Neuromorphic Computing using Spintronics..... | 143 |
| <i>Christopher Münch, Rajendra Bishnoi, Mehdi B. Tahoori</i> | |
| A Staircase Structure for Scalable and Efficient Synthesis of Memristor-Aided Logic | 150 |
| <i>Alwin Zulehner, Kamalika Datta, Indranil Sengupta, Robert Wille</i> | |
| On-Chip Memory Optimization for High-Level Synthesis of Multi-Dimensional Data on FPGA..... | 156 |
| <i>Daewoo Kim, Sugil Lee, Jongeun Lee</i> | |
| HUBPA: High Utilization Bidirectional Pipeline Architecture for Neuromorphic Computing..... | 162 |
| <i>Houxiang Ji, Li Jiang, Tianjian Li, Naifeng Jing, Jing Ke, Xiaoyao Liang</i> | |

| | |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| FPGA Laboratory System Supporting Power Measurement for Low-Power Digital Design..... | 168 |
| <i>Marco Winzker, Andrea Schwandt</i> | |
| Efficient Sparsification of Dense Circuit Matrices in Model Order Reduction..... | 170 |
| <i>Charalampos Antoniadis, Nestor Evmorfopoulos, Georgios Stamoulis</i> | |
| Spectral Approach to Verifying Non-Linear Arithmetic Circuits | 176 |
| <i>Cunxi Yu, Tiankai Su, Atif Yasin, Maciej Ciesielski</i> | |
| S ² -PM: <u>S</u> emi- <u>S</u> upervised Learning for Efficient <u>P</u> erformance <u>M</u> odeling of Analog and Mixed Signal Circuits..... | 183 |
| <i>Mohamed Baker Alawieh, Xiyuan Tang, David Z. Pan</i> | |
| Towards Limiting the Impact of Timing Anomalies in Complex Real-Time Processors | 189 |
| <i>Pedro Benedicte, Jaume Abella, Carles Hernandez, Enrico Mezzetti, Francisco J. Cazorla</i> | |
| Energy-Efficient, Low-Latency Realization of Neural Networks Through Boolean Logic Minimization | 195 |
| <i>Mahdi Nazemi, Ghasem Pasandi, Massoud Pedram</i> | |
| Log-Quantized Stochastic Computing for Memory and Computation Efficient DNNs..... | 201 |
| <i>Hyeonuk Sim, Jongeun Lee</i> | |
| Cell Division: Weight Bit-Width Reduction Technique for Convolutional Neural Network Hardware Accelerators | 207 |
| <i>Hanmin Park, Kiyoun Choi</i> | |
| LithoROC: Lithography Hotspot Detection with Explicit ROC Optimization..... | 213 |
| <i>Wei Ye, Yibo Lin, Meng Li, Qiang Liu, David Z. Pan</i> | |
| Detecting Multi-Layer Layout Hotspots with Adaptive Squish Patterns..... | 220 |
| <i>Haoyu Yang, Piyush Pathak, Frank Gennari, Ya-Chieh Lai, Bei Yu</i> | |
| A Three-Dimensional Millimeter-Wave Frequency-Shift Based CMOS Biosensor using Vertically Stacked Spiral Inductors in LC Oscillators | 226 |
| <i>Maya Matsunaga, Taiki Nakanishi, Atsuki Kobayashi, Kiichi Niitsu</i> | |
| A Local Optimal Method on DSA Guiding Template Assignment with Redundant/Dummy via Insertion..... | 228 |
| <i>Xingquan Li, Bei Yu, Jianli Chen, Wenxing Zhu</i> | |
| Deep Learning-Based Framework for Comprehensive Mask Optimization..... | 234 |
| <i>Bo-Yi Yu, Yong Zhong, Shao-Yun Fang, Hung-Fei Kuo</i> | |
| AxDNN: Towards the Cross-Layer Design of Approximate DNNs..... | 240 |
| <i>Yinghui Fan, Xiaoxi Wu, Jiyong Dong, Zhi Qi</i> | |
| Simulate-the-Hardware: Training Accurate Binarized Neural Networks for Low-Precision Neural Accelerators..... | 246 |
| <i>Jiajun Li, Ying Wang, Bosheng Liu, Yinhe Han, Xiaowei Li</i> | |
| An N-Way Group Association Architecture and Sparse Data Group Association Load Balancing Algorithm for Sparse CNN Accelerators..... | 252 |
| <i>Jingyu Wang, Zhe Yuan, Ruoyang Liu, Huazhong Yang, Yongpan Liu</i> | |

| | |
|------------------------------------------------------------------------------------------------------------------------------------------|-----|
| SeRoHAL: Generation of Selectively Robust Hardware Abstraction Layers for Efficient Protection of Mixed-Criticality Systems..... | 258 |
| <i>Petra R. Kleeberger, Juana Rivera, Daniel Mueller-Gritschneider, Ulf Schlichtmann</i> | |
| Maximizing Power State Cross Coverage in Firmware-Based Power Management..... | 264 |
| <i>Vladimir Herdt, Hoang M. Le, Daniel Große, Rolf Drechsler</i> | |
| Improving Scan Chain Diagnostic Accuracy using Multi-Stage Artificial Neural Networks..... | 270 |
| <i>Mason Chern, Shih-Wei Lee, Shi-Yu Huang, Yu Huang, Gaurav Veda, Kun-Han Hans Tsai, Wu-Tung Cheng</i> | |
| Testing Stuck-Open Faults of Priority Address Encoder in Content Addressable Memories | 276 |
| <i>Tsai-Ling Tsai, Jin-Fu Li, Chun-Lung Hsu, Chi-Tien Su</i> | |
| ScanSAT: Unlocking Obfuscated Scan Chains..... | 281 |
| <i>Lilas Alrahis, Muhammad Yasin, Hani Saleh, Baker Mohammad, Mahmoud Al-Qutayri, Ozgur Sinanoglu</i> | |
| CycSAT-Unresolvable Cyclic Logic Encryption using Unreachable States | 287 |
| <i>Amin Rezaei, You Li, Yuanqi Shen, Shuyu Kong, Hai Zhou</i> | |
| Routing in Optical Network-On-Chip: Minimizing Contention with Guaranteed Thermal Reliability | 293 |
| <i>Mengquan Li, Weichen Liu, Lei Yang, Peng Chen, Duo Liu, Nan Guan</i> | |
| Bidirectional Tuning of Microring-Based Silicon Photonic Transceivers for Optimal Energy Efficiency | 299 |
| <i>Yuyang Wang, M. Ashkan Seyedi, Jared Hulme, Marco Fiorentino, Raymond G. Beausoleil, Kwang-Ting Cheng</i> | |
| Redeeming Chip-Level Power Efficiency by Collaborative Management of the Computation and Communication | 305 |
| <i>Ning Lin, Hang Lu, Xin Wei, Xiaowei Li</i> | |
| A High-Level Modeling and Simulation Approach using Test-Driven Cellular Automata for Fast Performance Analysis of RTL NoC Designs | 311 |
| <i>Moon Gi Seok, Hessam S. Sarjoughian, Daejin Park</i> | |
| A Sharing-Aware L1.5D Cache for Data Reuse in GPGPUs..... | 317 |
| <i>Jianfei Wang, Li Jiang, Jing Ke, Xiaoyao Liang, Naifeng Jing</i> | |
| Partitioned and Overhead-Aware Scheduling of Mixed-Criticality Real-Time Systems..... | 323 |
| <i>Yuanbin Zhou, Soheil Samii, Petru Eles, Zebo Peng</i> | |
| NeuralHMC: An Efficient HMC-Based Accelerator for Deep Neural Networks..... | 329 |
| <i>Chuhan Min, Jiachen Mao, Hai Li, Yiran Chen</i> | |
| Boosting Chipkill Capability Under Retention-Error Induced Reliability Emergency | 335 |
| <i>Xianwei Zhang, Rujia Wang, Youtao Zhang, Jun Yang</i> | |
| SRAF Insertion via Supervised Dictionary Learning | 341 |
| <i>Hao Geng, Haoyu Yang, Yuzhe Ma, Joydeep Mitra, Bei Yu</i> | |
| A Fast Machine Learning-Based Mask Printability Predictor for OPC Acceleration..... | 347 |
| <i>Bentian Jiang, Hang Zhang, Jinglei Yang, Evangeline F. Y. Young</i> | |
| Semi-Supervised Hotspot Detection with Self-Paced Multi-Task Learning..... | 355 |
| <i>Ying Chen, Yibo Lin, Tianyang Gai, Yajuan Su, Yayi Wei, David Z. Pan</i> | |

| | |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| Exploring Emerging CNFET for Efficient Last Level Cache Design | 361 |
| <i>Dawen Xu, Li Li, Ying Wang, Cheng Liu, Huawei Li</i> | |
| Mosaic: An Automated Synthesis Flow for Boolean Logic Based on Memristor Crossbar | 367 |
| <i>Lei Xie</i> | |
| Layout Recognition Attacks on Split Manufacturing | 373 |
| <i>Wenbin Xu, Lang Feng, Jeyavijayan Rajendran, Jiang Hu</i> | |
| Design of 385 × 385 μm ² 0.165V 270pW Fully-Integrated Supply-Modulated OOK Transmitter in 65nm CMOS for Glasses-Free, Self-Powered, and Fuel-Cell-Embedded Continuous Glucose Monitoring Contact Lens..... | 379 |
| <i>Kenya Hayashi, Shigeki Arata, Ge Xu, Shunya Murakami, Cong Dang Bui, Takuyoshi Doike, Maya Matsunaga, Atsuki Kobayashi, Kiichi Niitsu</i> | |
| Execution of Provably Secure Assays on MEDA Biochips to Thwart Attacks | 381 |
| <i>Tung-Che Liang, Mohammed Shayan, Krishnendu Chakrabarty, Ramesh Karri</i> | |
| TAD: Time Side-Channel Attack Defense of Obfuscated Source Code | 388 |
| <i>Alexander Fell, Hung Thinh Pham, Siew-Kei Lam</i> | |
| Leakage-Aware Thermal Management for Multi-Core Systems using Piecewise Linear Model Based Predictive Control..... | 394 |
| <i>Xingxing Guo, Hai Wang, Chi Zhang, He Tang, Yuan Yuan</i> | |
| 2D Optical Imaging using Photosystem Photosensor Platform with 32x32 CMOS Biosensor Array | 400 |
| <i>Kiichi Niitsu, Taichi Sakabe, Mariko Miyachi, Yoshinori Yamanoi, Hiroshi Nishihara, Tatsuya Tomo, Kazuo Nakazato</i> | |
| Multi-Angle Bended Heat Pipe Design using X-Architecture Routing with Dynamic Thermal Weight on Mobile Devices | 402 |
| <i>Hsuan-Hsuan Hsiao, Hong-Wen Chiou, Yu-Min Lee</i> | |
| Fully-Automated Synthesis of Power Management Controllers from UPF | 408 |
| <i>Dustin Peterson, Oliver Bringmann</i> | |
| Integrated Flow for Reverse Engineering of Nanoscale Technologies | 414 |
| <i>Bernhard Lippmann, Michael Werner, Niklas Unverricht, Aayush Singla, Peter Egger, Anja Dübotzky, Horst Gieser, Martin Rasche, Oliver Kellermann, Helmut Graeb</i> | |
| Design of Gate-Leakage-Based Timer using an Amplifier-Less Replica-Bias Switching Technique in 55-nm DDC CMOS..... | 422 |
| <i>Atsuki Kobayashi, Yuya Nishio, Kenya Hayashi, Shigeki Arata, Kiichi Niitsu</i> | |
| NETA: When IP Fails, Secrets Leak..... | 424 |
| <i>Travis Meade, Jason Portillo, Shaojie Zhang, Yier Jin</i> | |
| Machine Learning and Structural Characteristics for Reverse Engineering | 430 |
| <i>Johanna Baehr, Alessandro Bernardini, Georg Sigl, Ulf Schlichtmann</i> | |

Author Index