

2024 27th International Symposium on Design & Diagnostics of Electronic Circuits & Systems (DDECS 2024)

**Kielce, Poland
3 – 5 April 2024**



**IEEE Catalog Number: CFP24DDE-POD
ISBN: 979-8-3503-5935-0**

**Copyright © 2024 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP24DDE-POD
ISBN (Print-On-Demand):	979-8-3503-5935-0
ISBN (Online):	979-8-3503-5934-3
ISSN:	2334-3133

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

TABLE OF CONTENTS

Exploring Quantization and Mapping Synergy in Hardware-Aware Deep Neural Network Accelerators.....	1
<i>Jan Klhufek, Miroslav Safar, Vojtech Mrazek, Zdenek Vasicek, Lukas Sekanina</i>	
Performance and Error Tolerance of Stochastic Computing-Based Digital Filter Design.....	7
<i>Roshwin Sengupta, Ilia Polian, John P. Hayes</i>	
Early Detection of Permanent Faults in DNNs Through the Application of Tensor-Related Metrics	13
<i>V. Turco, A. Ruospo, E. Sanchez, M. Sonza Reorda</i>	
SAFFIRA: A Framework for Assessing the Reliability of Systolic-Array-Based DNN Accelerators.....	19
<i>Mahdi Taheri, Masoud Daneshtalab, Jaan Raik, Maksim Jenihhin, Salvatore Pappalardo, Paul Jimenez, Bastien Deveautour, Alberto Bosio</i>	
An Autonomous Clock Frequency Supervision Circuit.....	25
<i>Clemens Scharwitzl, Andreas Steininger</i>	
A New Reliability Analysis of RISC-V Soft Processor for Safety-Critical Systems.....	31
<i>Giorgio Cora, Corrado De Sio, Daniele Rizzieri, Sarah Azimi, Luca Sterpone</i>	
The Impact of Well-Edge Proximity Effect on PMOS Threshold Voltage in Various Submicron CMOS Technologies.....	37
<i>Marika Grochowska, Witold A. Pleskacz</i>	
A Low-Noise High-Voltage Rail-To-Rail Operational Amplifier with Gain Stabilization and Slew-Rate Enhancement.....	41
<i>Jie Pan, Fanyang Li, Yidong Yuan, Tianting Zhao, Hongwei Shen, Liguo Wen, Yi Hu, Jiazhen Jin, Shuwen Wu</i>	
Hardware Honeypot: Setting Sequential Reverse Engineering on a Wrong Track.....	47
<i>Michaela Brunner, Hye Hyun Lee, Alexander Hepp, Johanna Baehr, Georg Sigl</i>	
Fault-Simulation-Based Flip-Flop Classification for Reverse Engineering	53
<i>Michael Mildner, Michaela Brunner, Michael Gruber, Johanna Baehr, Georg Sigl</i>	
Optimised AES with RISC-V Vector Extensions	57
<i>Mahnaz Namazi Rizi, Nusa Zidaric, Lejla Batina, Nele Mentens</i>	
Xoodyak Under SCA Siege	61
<i>Parisa Amiri Eliasi, Silvia Mella, Léo Weissbart, Lejla Batina, Stjepan Picek</i>	
PaGoRi:A Scalable Parallel Golomb-Rice Decoder	67
<i>Mounika Vaddeboina, Endri Kaja, Alper Yilmazer, Uttal Ghosh, Wolfgang Ecker</i>	
Improving Virtual Prototype Driven Hardware Optimization by Merging Instruction Sequences.....	73
<i>Jan Zielasko, Rune Krauss, Marcel Merten, Rolf Drechsler</i>	
ABACUS: ASIP-Based Avro Schema-Customizable Parser Acceleration on FPGAs	79
<i>Tobias Hahn, Daniel Schüll, Stefan Wildermann, Jürgen Teich</i>	
A Comparison of Logic Extraction Methods in Hardware-Translated Neural Networks	86
<i>Jan Schmidt, Petr Fišer, Miroslav Skrbek</i>	

QDI Binary Comparator Networks and Their Application in Combinational Logic	92
<i>Florian Huemer</i>	
An Efficient Approach for STLs Development of Automotive SoCs using Colored Petri Nets.....	98
<i>Ernesto Cristopher Villegas Castillo, Felipe Augusto Da Silva, Michael Glaß</i>	
TCC: GPGPU Architecture for Instruction Decoder and Control Flow Error Detection	104
<i>Raghunandana K K, Yogesh Prasad K R, M. Sonza Reorda, Virendra Singh</i>	
On the Fault Tolerance of Self-Supervised Training in Convolutional Neural Networks	110
<i>Rosario Milazzo, Vincenzo De Marco, Corrado De Sio, Sophie Fosson, Lia Morra, Luca Sterpone</i>	
On-Chip Cross-Layer Infrastructure to Leverage System Reliability for Aero-Space Applications	116
<i>Fabian Luis Vargas</i>	
Choose Your Path: Control of Ring Oscillators EMFI Susceptibility Through FPGA P&R Constraints.....	118
<i>Sami El Amraoui, Régis Leveugle, Paolo Maistri</i>	
Evaluating the Reliability of Integer Multipliers with Respect to Permanent Faults.....	124
<i>Nikolaos I. Deligiannis, Riccardo Cantoro, Matteo Sonza Reorda, S. E. D. Habib</i>	
Adaptive Input Normalization for Quantized Neural Networks.....	130
<i>Jan Schmidt, Petr Fišer, Miroslav Skrbek</i>	
Interface Protection Against Transient Faults.....	136
<i>Ján Mach, Lukáš Kohútka, Pavel Cicák</i>	
An Efficient High-Level Synthesis Implementation of the MUSIC DoA Algorithm for FPGA	142
<i>Sakari Lahti, Tuomas Aaltonen, Elizaveta Rastorgueva-Foi, Jukka Talvitie, Bo Tan, Timo D. Hämläinen</i>	
A ML-Based Approach for Finding the Product Definition Space of Microelectronic Power Switches	148
<i>Seyedbehnam Beladi, Linus Maurer, Jonas Stricker, Georg Pelz</i>	
Constant Voltage Maximum Power Point Tracking Method for Fully Integrated Solar-Powered Energy Harvester	152
<i>Adam Hudec, Robert Ondica, Richard Ravasz, Viera Stopjakova</i>	

Author Index