

2024 IEEE 40th International Electronics Manufacturing Technology (IEMT 2024)

**Penang, Malaysia
16-18 October 2024**



**IEEE Catalog Number: CFP24IEU-POD
ISBN: 979-8-3503-8883-1**

**Copyright © 2024 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP24IEU-POD
ISBN (Print-On-Demand):	979-8-3503-8883-1
ISBN (Online):	979-8-3503-8882-4

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

TABLE OF CONTENTS

Pushing the Limits of Miniaturization in Microelectronic Packaging Via the Application of Ultra-Thin Micro Dam Structures	1
<i>Patrick Schirmer, Severin Ringelstetter, Kian Chong Tai, Muizzuddin Azfar, Tobias Königer, Kilian Kreul</i>	
Enhanced Control of WLCSP Wafer Dicing Through Big Data Automation and Analysis.....	9
<i>J W Seah, L M Shong, Arisha Mohd Azhar, Kevin Choy</i>	
Exploring the Patent Landscape of Sintered Metal Technologies: An Analysis Using LLM-Based AI Patent Search	18
<i>Kim S Siew, Weijie Wang, Raihana Bahru, Xu Long, Hing Wah Lee</i>	
Alpha Emission Rate Characterization and Risk Evaluation of Substrate Materials Used in Memory Packages	22
<i>Chen Yu Huang, Chi Yung Chen, Chong Leong Gan, Tracy Tennant</i>	
Enhanced Fault Localization Strategies Through Versatile Sample Preparation Techniques for Electro Migration Defect Preservation and Characterization	27
<i>Farisal Abdullah</i>	
Feasibility Study on Real Time Electrostatic Charge Monitoring in Wafer Form Process with Potential Triboelectrification Motion at Dicing Saw	33
<i>Jian Liang Lim, Qiu Yin Wong, Mohamad Syafiq Bin Mokhtar, Jayanth Reddy Ramireddy, Mun Seng Wong, Chong How Ng, Kim Chuan Lee, Bh Moon</i>	
Determining Organic Solvent Bath Lifespan in Lead-Frame Cleaning.....	39
<i>Guan Tatt Yeoh, Chun Tat Lok, Mohamad Husaini Bin Zainol</i>	
Chemical Identification of Sub 10- μ m Defects and Contamination in Packaging	49
<i>Michael K. F. Lo, Eoghan P. Dillon, James A. Anderson</i>	
High-Density Flip Chip Solder Bump Bridging Detection Using YOLOv7	53
<i>Lau Wei Theng, Lee Jun-On, Lam Pooi Kit</i>	
Novel Bond-Wire Optimization Method for PISI and Yield Improvement.....	59
<i>Rishi Bhooshan, Ajay Kumar Sharma, Jasmine Lim, Yin Kheng Au, Swapnil Tiwari</i>	
Pressure and Pressure-Less Cu Sintering Paste Developed for Next Generation Interconnection Material	63
<i>Min Yao, Li Ma, Hongyun Li, Yan Wu, Xuelian Han, Xiaoqin Lu, Zhongrui Zhao, Meng Li, Fen Chen, Yan Liu</i>	
Process Integration of Unique Identification Marks Using Inkjet Technologies for Backside Coating Tape	69
<i>Sayaka Matsuno, Ken Takano, Tadatomo Yamada, Shinya Takyu</i>	
Industrialization of a New Adhesion Promoter Process for Leadframe.....	74
<i>Paolo Crema, Din Ghee Neoh, Riccardo Villa, Boon Seong Lee, Christian Ohde</i>	
Galvanic Corrosion Behavior of Ag-Filled Electrically Conductive Adhesive on Sn-Plated of Surface Mount Chip Resistor	81
<i>Onanong Phosri, Kornteenee Pairpisit, Chayathorn Saklang, Kittichai Fakpan, Amar Mavinkurve</i>	

Impact of Thermomechanical Fatigue and Creep on the Reliability of BGA Lead-Free Solder Joints in Electronic Modules.....	86
<i>Joshua A Depiver, Sabuj Mallik, Emeka H Amalu</i>	
Intel's Affordable Industrial Internet of Things(IoT) for Equipment Predictive Maintenance	93
<i>Ee Boon Yee, Lee Hai Liang Duncan, Masterson Barry, Puvanesvaran Shanmugan, Wong Shaw Fong</i>	
Analytical Approach for Preliminary Deformation Investigation.....	99
<i>Roseanne Duca</i>	
Wafer Level Plasma as an Alternative for Wafer Pre Thin Process	104
<i>Jekan Asokumaran, Siva Balan A-L Joega Nathan</i>	
Compute Dynamic Random Access Memory (DRAM) Silicon Spacer Elimination - A Process Simplification Approach.....	109
<i>Ravinder Singh Sidhu, Siva Balan A-L Joega Nathan</i>	
New Enhanced Loop Formation for Compute DRAM Package: An Innovative Solution to Enhance Robustness of Wire Loop and Enable Design Rule Limitation	114
<i>Ling Luo Ing, Aldin-John Andam Tuazon, Kwok Ting Sheng</i>	
Base Loop Characterization to Alleviate Short Tail Issue in Stack Die Package	119
<i>Nisha Veloo, Aldin-John Andam Tuazon, Amnani Rosland</i>	
Developing a Simulation Model to Improve Strip Warpage Performance Predictability	123
<i>Vaishnavi Shah, Jer Jian Wong</i>	
Effect of Anti-Epoxy Bleed Out Concentration and Leadframe Plating Condition Towards Die Attach Glue Bleed Out Performance	129
<i>Mohamad Syahirul Syafiq Ali, Muhammad Danial Afiq Mohamad Ghazali, Cheeyee Heng</i>	
C5 Reflow and Flux Clean Characterization for Automotive FCBGA	133
<i>Muhammad Syakir Turiman, Cai Hui Tan, Dominic Koey Poh Meng</i>	
Effect of Lead Lock Tape Mirror Tool (LLT) Towards Machine Performance & Yield.....	140
<i>Cheeyee Heng, Mohamadhidayat Halim, Yeechong Chua, Mohdridwan Johari</i>	
Improvement of Laser Groove Bottom Width in Complementary Metal-Oxide-Semiconductor (CMOS) Low-K Wafer Technology	143
<i>Mohd Fauzi Bin Mohd Noh</i>	
Laser Ablation Dicing Revolutionizes Ultra-Thin Wafer Saws Beyond the Capability of Blade Dicing	147
<i>Siang Miang Yeo</i>	
Energy Saving in Semiconductor Packaging Plating Processes Through Chemical Deflashing Process Optimization.....	153
<i>Arieff Yusoff</i>	
Effective Approach to Achieve Zero Interfacial Delamination on High-Power Automotive Devices After Reliability Test	157
<i>Chin Joo Tan, Azamer Kastor, Mohd Hasrul Zulkifli, Ahmad Shahril Khamarazaman, Kwang Jun Lee, Mee Sing Tiong, Boo Wei Tan</i>	
An Innovative Hybrid Cleaning Approach for Contaminant Removal in Semiconductor Packaging	162
<i>Chun Yuan Lim, Meng Kong Heng, Mee Sing Tiong, Kwang Jun Lee</i>	

Synergistic Interactions Between Water-Soluble Solder Paste and Ultrasonic Flux Cleaning in Producing Zero Solder Ball Rejects	168
<i>Nurrul Anis Syuhada Abd Latif</i>	
Warpage Simulation Including the Effect of Molding Compound Cure Shrinkage	173
<i>Bin Gu, Jing-En Luan, Phone Maw Hla</i>	
Breakthrough Bundle X-Out Fiducial Design for Multi-Up PCB	176
<i>Fook Loon Wooi</i>	
Innovative RF Shield Rework Method for Wireless Module in Ultrathin Notebook	179
<i>Fook Loon Wooi</i>	
Strip Lasermarking Offset Marking Defect Improvement for Small Outline Packages	183
<i>Devar Raja Ramalingam, Chee Aung Koo, Mohd Aizat Bin Abas</i>	
Enhancement of 8mm Carrier Tape Sealing Performance for Small Diode (SOD) Package Via Carrier Tape Material and Sealing Shoe Selection	187
<i>Mohd Rozaini Mohd Zali, Mohd Aizat Bin Abas</i>	
The Effect of Ion Implantation on Carbon Diffusion Through Si/SiO _x Layer	192
<i>Pui Key Poon, Tatt Wai Wan, Chan Lik Tan, Kuan Yew Cheong</i>	
Computational Fluid Dynamics Approach to Enhance Capillary Underfill Encapsulant Process in Heterogenous Package.....	197
<i>Muhammad Aqil Azman, Loh Wei Keat, Ooi Chun Keang, Mohd Zulkifly Abdullah</i>	
An Innovative Approach to Scanning Acoustic Microscopy (SAM) for Layered Structures in Wafer Level Chip Scale Package (WLCSP)	202
<i>Pravin Vijayan, Mohd Safwan Bin Md Nor, Mohd Nurhisham Bin Abdullah, Subashini Periasamy</i>	
Voiding Control of Lead-Free Soldering at Quad-Flat No-Lead Package Components.....	209
<i>Li Ma, Jinjin Bai, Fen Chen, Yan Liu</i>	
Leadframe Strip Stiffness Simulation for Identification of Issues During Package Singulation Process.....	213
<i>M. A. A. Afripin, B. T. Y. Fang, J. J. M. Zaal</i>	
Overshoot Concerns for Fixed Voltage Rails with High Layout Resistance (Rpath) in Advanced SoCs	218
<i>Sze Geat Pang, Han Kung Chua</i>	
Auto Phase Management Optimization of Multiphase Voltage Regulator to Improve ErP Lot 3 Performance Per Watt.....	223
<i>Han Kung Chua, Fazli Lut Ahmad Fuad, Vega Liu, Ivan B Wang</i>	
Study of Solder Ball Hardness on Wafer Level Chip Size Packages.....	229
<i>Aye Aye Mon, Daniel Yap</i>	
High Density Interconnect (HDI) Socket Dynamic Warpage Prediction by Mori-Tanaka Model	235
<i>Chun Keang Ooi, Muhammad Naqib Nashrudin, Philip Chang, Wen Li Xu, Lili Ding, Pierre-Louis Toussaint, Yan Yz Lin, Devon Heil, Wei Keat Loh, Haley Fu</i>	
Real Time Inferencing of Semiconductor Wafer Probing Process Using Machine Learning.....	242
<i>Michael Thavarajah</i>	

Functional Validation on Complex Power Integrity Network Design	248
<i>Dilukshan Karunatilaka, Fern Nee Tan, Mohamad Shahrir Tamrin, Sze Geat Pang</i>	
Micro Bumping Via Paste Dispensing Technology for Advanced Packaging	252
<i>Senthil Kumar Balasubramanian, Yam Lip Huei, Edrina Risson Olakkankal, Zhang Rui Fen, Tai Kian Chong, Muizzuddin Azfar</i>	
The Challenges and Solutions to the Development of Light Shielding Mask Glass from Design Phase to Process Optimization for CMOS Image Sensors	257
<i>May May Gan, Ying Heong Chiew, Kok Inn Hoo, Teck Siang Lim</i>	
Investigating Crystallography and Thickness Distribution of Aluminium Nitride Thin Films Prepared by Magnetron Sputtering on Silicon Wafer	263
<i>Zulkifli Azman, Nafarizal Nayan, Muhammad Khairin Shafiq Shaiful Nazri, Ahmad Shuhaimi Abu Bakar, Riyaz Ahmad Mohamed Ali, Faezahana Mohkhter, Norain Sahari, Mohd Rofei Mat Hussin</i>	
Die Placement Process Optimization in Reducing Occurrence of Solder Short Between Flip-Chip Die Pad	268
<i>Sze Theng Chin</i>	
Effect of Fluorine Implant Energy on the Performance of P+/N-Junction, Poly-Si Resistor, and PMOS	271
<i>Lee Sai Link, Mohamed Fauzi Packer Mohamed, Tan Chan Lik</i>	
Enhancing AOI with AI for Printed Circuit Board Assembly – a Comprehensive Industry Study	275
<i>Wayne Zhang, Feng Xue, Romain Roux, Philip Aguilar Reyes, Jorg Richstein, Tatu Qvist, Harri Sievola, Zambri Samsudin, Chwee Liang Tee, Yassin Roslan, Kah Seng Adrian Leong, Daniel Tan, Aersi Aierzhati, Charlie Zhu, Stephan Pimer, Mehdi Hamid, Haley Fu</i>	
Peripheral Component Interconnect Express (PCIe) Transmitter Preset Coefficient Autotune Algorithm	280
<i>Lim Yin Chung, Wong Yeng Bin, Oh Loo Wen, Tan Jared</i>	
Recent iNEMI Research on Electromigration in Tin-Bismuth Solder.....	287
<i>Prabjit Singh, Larry Palmer, Thomas Wassick, Raiyo Aspandiar, Brian Franco, Lavanya Ashok Swaminathan, Haley Fu, Faramarz Hadian, Richard Coyle, Terry Munson, Steve Middleton, Hongwen Zhang, Anna Lifton, Keith Howell, Vasu Vasudevan, Kei Murayama, Sarangapani Murali</i>	
Low- And Mid-Temperature Pb-Free Solder Preform Technology in Substrate Attach Application for Improved Thermomechanical Performance.....	294
<i>Sunny Neoh, Joseph Hertline, Ryan Mayberry, Alexander Russell</i>	
Decoupling Capacitor Booster Module	298
<i>Kean Huat Leong, Nik Mohd Syaeran Roslan</i>	
Die Cost Reduction Through Re-Architecting Power Delivery Network Design and Enabling Common Package Footprint	302
<i>Jia Yun Chuah, Fern Nee Tan, Mohamad Shahrir Tamrin</i>	
Introduction to Power Tunnel Innovation in PCB & Package for Better Platform Power Delivery.....	307
<i>Khai Ern See, Chan Kim Lee, Jia Lin Liew, Thim Khuen Wong, Yi How Ooi, Chee How Lim, Seok Ling Lim, Jaffar Hazwani</i>	

Exploration on Miniaturization of Immersion Cooling Technology for Client Desktop and Edge Devices	313
<i>Khai Ern See, Baomin Liu, Eng Kwong Lee, Chin Kung Goh, Cora Nien, Chun Keang Ooi, Jia Yan Go</i>	
A Journey of Bringing Portability to Desktop AIO PC: The Experience & Key Learning	318
<i>Khai Ern See, Chin Kung Goh, Jia Yan Go, Chin Seong Khor, Boon Ping Koh, Chee How Lim, Yew San Lim, Wei Suen, Sam Tsai, Jeffrey Ho</i>	
Manufacturability of a Novel Vertical Interconnect Design for High-Speed Signaling	324
<i>Jackson Kong, Bok Eng Cheah, Kok Hou The, Hong Cheah Ho</i>	
Wave Solder Process Characterization in PCBA.....	328
<i>Jui Ang Tan, Chee Chuan Tan, Kum Foo Leong</i>	
Cost Effective Hostless System for Add-In-Card (AIC) Post-Silicon Electrical Validation.....	332
<i>Hooi Leong Lim, Adrian Kang Mouk Pio, Jo En Kang, Bridget Chia Mei Tham</i>	
Investigation of PMOS Transistor Threshold Voltage Shift in BCD Technology.....	336
<i>Tang Khang Seng, Samail Deyline, Hamzah Zool Helmi, Oh Guan Kai, Kamaruddin Mohd Hanif</i>	
Development of Panel Level Packaging for Multi-Chip Modules with High-Precision Redistribution Layer.....	340
<i>Zeyu Ma, Di He, Gaolin Li, Junbo Jiang, Xuan Gao, Qiang Tang, Yuhang Peng, Tao Sun, Hu</i>	
Signal and Power Integrity Challenges in PCB for System-On-Chip(SoC) Based Automotive Applications and the Need for Chiplet Based Designs.....	344
<i>Harini Manoharan, Frank Ebert, Dhanasekar Chinnappan</i>	
+Architecting for the First Low Power Double Data Rate 5 (LPDDR5) Memory Module.....	350
<i>Luis Carlos Alvarez Mata, Min Suet Lim, Mohamad Zaki Zulkifli, Frank Kern, Stephen Christianson, Rijo Kizhakkedathu Avarachan, Eng Same Tan</i>	
Deposition of AlGaN Thin Film Using HIPIMS and RF Co-Sputtering Technique.....	360
<i>Nafarizal Nayan, Nur Afiqah Othman, Zulkifli Azman, Riyaz Ahmad Mohamed Ali, Megat Muhammad Ikhsan Megat Hasnan, Mohd Zamri Mohd Yusop, Mohd Yazid Ahmad, Mohd Hafiz Mamat, Ahmad Shuhaimi Abu Bakar</i>	
Impacts of Saw Blade Selection, Dressing and Dicing Parameters on Die Sidewall Quality	363
<i>Teck Beng Lau, Andersen Yu-Jen Tien, Poh Leng Eu, Jhen Wei Seah, David Renouf, Dzafir Shariff, Enrique Ellorin Sarile, Julius Guele Hermano, Joel Billodo Ofalsa</i>	
Fluorine Residue Reduction in Plasma Dicing	369
<i>Chua Rho Wen, Lau Teck Beng, Taki Fang, Li Shi Zheng, Li Si Yuan, Eu Poh Leng</i>	
Influence of Moisture Variation on SAC405 Solder Ball Oxidation Characteristic in WLCSP	373
<i>Chofu Liu, Eu Poh Leng, Lau Teck Beng, Viola Lee, Steve Hsieh, S Lee Ming Shong, Simon Jude Madelo Burgos</i>	
Multi Row QFN Wire Gap Clearance Improvement Using Improved Mold Compound.....	378
<i>Chantana Tangcharoensuk, Pey Fang Hiew, Eu Poh Leng, Kanna Krishnasamy, Natawat Kasikornrungroj, Panumard Thammavet</i>	
Exploring the Correlation Between Post-Die Bond Epoxy Void and Bond Line Thickness and Other Factors on Power Packaging with Silver Sintered Epoxy	382
<i>Jae Yun Kim, Azham Mohd Sukemi, Eu Poh Leng, Seongkuk Kang, Sunkyong Kim</i>	

Challenges and Resolutions of 28nm Copper Wire Bond Process for Automotive Application	387
<i>Pey Fang Hiew, Tsung-Nan Lo, Poh Leng Eu, Shih-Shuang Huang, Sam Lai, Howard Liu, Krassavan Tantirittisak, Jw Chen</i>	
Investigation of Laser Pulse Energy and Grinding Tool Characteristic on Marking Legibility of FOPLP	392
<i>Andersen Tien Yu Jen, Huang Wen Hung, Eu Poh Leng, Kay Hsu Che Kai, David Renouf, Wu Tsung Yuan, George Lin Chung Chih, Vita Wu Yun Te</i>	
Moisture Effect on Adhesion Between Polybenzoxazole and Sputtering Titanium in WLCSP	397
<i>Fang Che Ming, Eu Poh Leng, Huang Wen Hung, Liu Jian Hong, Yao Ren Jie, Zhang Fong</i>	
Investigation of Package Delamination Behavior in Large Quad Flat No-Lead Package	401
<i>Tsung Nan Lo, Chang Hao Liu, Pey Fang Hiew, Wen Hung Huang, Poh Leng Eu, Shih Shuang Huang</i>	
Rheological Characterisation of Graphene Filled Isotropic Conductive Adhesives.....	405
<i>Richard Ang Giap Leng, Rajkumar Durairaj</i>	
Study of Glue Creeping Behavior on Die Surface for Thin Die Using Roughen Pre-Plated Leadframe.....	411
<i>Nara Tappetch, Yothin Komchuad, Kanthorn Sarpitthak, Watcharapol Kundalaputra, Pairat Sungchoom, Kornteenee Pairpisit, Akkachai Potitaram, Ittipon Intamart</i>	
Automotive High Power Flip Chip Quad Flat No-Leads Package Robustness Study.....	415
<i>Wen Yuan Chuang, Wen Hung Huang, Eu Poh Leng, Ade Tsai, Fenny Li, Daisuke Hosoda</i>	
PFAS Free Die Attach for Robust Manufacturability of Large Body Semiconductor Packages	418
<i>Avin Dhoble, Senthil Kanagavel, Elisia Siew</i>	
Refined Wire Bond Pad Cratering Testing Method	422
<i>Andrea Goh, Leong Chung Ling</i>	
FCLGA Study with Polymide (PI) Removal from Chip Surface	427
<i>David Liu, Lok Sook Kuen, Eu Poh Leng, Gao Zhenpeng, Lu Jian, Chin Teck Siong</i>	
Development of Robust Cu Wire Looping for Small Sensor QFN Package with Higher Dual Die Stack	434
<i>Antonio A. M. Macatangay, Pey Fang Hiew, Eu Poh Leng, Chayathorn Saklang, Lo Hsiang, Tai Po Huang, Chi Hao Lin</i>	
Illuminating Precision: Enhancing Clip Attach Vision Accuracy in Semiconductor Manufacturing	440
<i>Mahenthren Palaniappan</i>	
Effective Lead Lock Tape Solution for Mitigating Leadframe's Lead Bend in Semiconductor Packaging	445
<i>Mahenthren Palaniappan, Dhanaraj Perumal, Nur Amirah Zainal Abdin, Wai Leong Khiew, Lim Zikang, Nur Aqilah Husin</i>	

Author Index