2024 IEEE 33rd Asian Test Symposium (ATS 2024)

Ahmedabad, India
17-20 December 2024

IEEE Catalog Number: CFP24067-POD
ISBN: 979-8-3315-2917-8

Copyright © 2024 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP24067-POD
ISBN (Print-On-Demand):	979-8-3315-2917-8
ISBN (Online):	979-8-3315-2916-1
ISSN:	1081-7735

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

2024 IEEE 33rd Asian Test Symposium (ATS)

Table of Contents

Message from the Chairs
Steering Committee
Organizing Committee
Tutorials
Keynotes
Sponsors

MTCX : Ultra-high Throughput TRNG Based on Mesh topology of Coupled-XOR...1
lu yingchun[1], Enpu Xu[1], Huaguo Liang[1], Cuiyun Jiang[1], Lixiang Ma[2], Liang Yao[2]
[1] Hefei University of Technology
[2] Anhui Institute of Information Technology

Trojan Horse Detection for RISC-V Cores Using Cross-Auditing...5
Wei-Po Huang[1], Shi-Yu Huang[1], Chi-Kang Chen[2], Siang-ChengHu Huang[1]
[1]National Tsing Hua University
[2]TESDA

An FPGA-Based Emulation Platform for Functional Safety Verification in Automotive SoC Systems...11
Yutao Sun[1], Wang Zhijun[1], Zean huang[1], Liping Liang[1]
[1]Beijing University of Posts and Telecommunications

Effective Runtime Fault Detection for DNN Accelerators...17
Wei-Kai Liu[1], Jonti Talukdar[2], Krishnendu Chakrabarty[3], Benjamin Tan[4]
[1]Duke University
[2]NVIDIA
[3]Arizona State University
[4]University of Calgary

Reliability Enhancement of Memristor-Based Neural Networks with Fault-Injected Training...23
Md. Sihabul Islam[1], Ryota Eguchi[1], Michiko Inoue[1]
[1]Nara Institute of Science and Technology

Methods and Apparatus to Support Multiple Synchronous Clocks with a Single Clock Mesh...29
Shubham Shrivastava[1], Sainath Yeshagol[1], Harry Linzer[1]
[1]Marvell India Pvt. Ltd.

A Formal Approach and Testing Process for Failure Modes in Intelligent Algorithms...33
Nishan Xie[1], Hongping Ren[2], Rui Li[2], Qian Dong[2], Lingzhong Meng[2]
[1]University of Chinese Academy of Sciences
[2]Institute of Software Chinese Academy of Science

Boosting Self-Repair Workflow with Brainstorming for Code Generation...39
Zhaoming Jin[1], Zhixin Shi[1]
[1]Institute of Information Engineering, Chinese Academy of Sciences

Low-Cost Generation of RF Test Stimuli from Baseband Digital Signals...45
Kamilia Tahraoui[1], Florence Azais[1]
[1]LIRMM, Univ. Montpellier, CNRS

A Novel Multi-Scope Characterization Method for Automotive LPDDR4 Controller...51
Vasavi Ghanta[1], Vinodh Rakesh[1]
[1]Infineon Technologies

Automotive Microcontroller Characterization Hardware – Challenges and Solutions...58
Jithesh K[1], Vinodh Rakesh[1], Prince Thachil[1], Timmy Peter[1], Vasavi Ghant[1]
[1]Infineon Technologies Semiconductor India Private Limited

High Performance Advanced Fault Model Diagnosis...64
Vaibhav Mishra[1], Bharath Nandakumar[1], Sameer Chillarige[1]
[1]Cadence Design Systems

Carbon Quantum Dot Fluorescent Stickers for Biochip Authentication...71
Navajit Baban[1], Mohammed Abdelhameed[1], Mahmoud Elbeh[1], Khalil Ramadi[1], Yong Ak Song[1], Sukanta Bhattacharjee[2], Ramesh Karri[1], Krishnendu Chakrabarty[3]
[1]New York University Abu Dhabi
[2]IIT Guwahati
[3]Arizona State University

Hacking the Fabric: Targeting Partial Reconfiguration for Fault Injection in FPGA Fabrics...77
Jayeeta Chaudhuri[1], Hassan Nassar[2], Dennis Gnad[2], Joerg Henkel[2], Mehdi Tahoori[2], Krishnendu Chakrabarty[1]
[1]Arizona State University
[2]Karlsruhe Institute of Technology

Post-silicon Trace Signal Selection Using Genetic Algorithm...83
Hanxu Feng[1], Yuanhang Bu[1], Jing Zhou[1], Shuo Wang[1], Lei Chen[1], Zhuoli Wang[1], [1]Beijing Microelectronics Technology Institute

Preferential Fault-Tolerant based TF32 Floating Point Adder for Mission Critical Systems...87
Raghavendra Kumar Sakali[1], Noor Mahammad Sk[2]
[1]Sri Sivasubramaniya Nadar College of Engineering, India
[2]Indian Institute of Information Technology Design and Manufacturing (IIITDM) Kancheepuram, India

Fault Tolerance in Stochastic Circuits for Recurrent Sequential Neural Networks...92
Roshwin Sengupta[1], Ilia Polian[1], John P. Hayes[2]
[1]University of Stuttgart
[2]University of Michigan

Optimized Detection of Marginal Defects in Standard Cells Using Unsupervised Learning...98
Karthik Pandaram[1] , Hussam Amrouch[2], Ilia Polian[1] (University of Stuttgart) [1]University of Stuttgart
[2]Techincal University of Munich

Power Aware test methodology for Test Power hungry complex SoCs...104
Piyushkumar Chaniyara[1], Pervez Garg[1]
[1]Texas Instruments, India

Optimizing LBIST Run Time for a Safety Critical SoC: A Practical Approach...108
Sujeet Maurya[1] , Gedupudi Bharghav Ram[2]
[1]Texas Instruments, India
[2]MNIT Jaipur, India

A Complete Security Protocol to Safeguard IJTAG Architecture...113
Niranjana Ithal[1], Adharsh Natarajan[1], Sudeendra Kumar[1], P Anurup[1]
[1]PES University, Bangalore, India

Automated System for Testing and Result Analysis for Payload Controller...119
Anirban Paul[1], Jimit Gadhia[1], Aashish Agrawal[1], Ashok Kumar[1], Ashutosh Mishra[1], Sandip Paul[1], Ashish Misra[1], Sanjeev Mehta[1], Anuj Srivastava[1],
[1]Space Applications Centre

Large Language Model Driven Logic Locking: A Generative Approach to Secure IC Design...125
Jugal Gandhi[1], Diksha Shekhawat[2], M. Santosh[1], Jaya Dofe[2], Jai Gopal Pandey[1], Gandhi[1]
[1]Academy of Scientific and Innovative Research
[2]CSUF

A Novel TSV Repair Framework for 3-D Stacked ICs...129
Dr. Tanusree Kaibartta[1], Debesh K. Das[2]
[1]IIT DHANBAD
[2]Jadavpur University Kolkatta

SAMURAI: Safeguarding against Malicious Usage and Resilience of AI...135
Habibur Rahaman[1], Atri Chatterjee[1], Swarup Bhunia[1]
[1]University of Florida

LATENT: Leveraging Automated Test Pattern Generation for Hardware Trojan Detection...141
Sudipta Paria[1], Pravin Gaikwad[1], Aritra Dasgupta[1], Swarup Bhunia[1]
[1]University of Florida

FORTUNE: A Negative Memory Overhead Hardware-Agnostic Fault TOleRance TechniqUe in DNNs...147
Samira Nazari[1], Mahdi Taheri[2], Ali Azarpeyvand[1], Masoud Daneshtalab[3], Christian Herglotz[4], Mohsen Afsharchi[5], Tara Ghasempouri3, Maksim Jenihhin[3]
[1]University of Zanjan
[2]Tallinn university of technology
[3]Taltech
[4]Brandenburgische-Technische Universität Cottbus-Senftenberg
[5]ZNU

PATROL: An Evolutionary Approach to Automatic Test Pattern Generation for Hardware Trojan Detection Leveraging PSO-GA Hybrid Techniques...153
mostafa hosseini[1], Ali Azarpeyvand[1], Tara Ghasempouri[2]
[1]University of Zanjan
[2]Tallinn University of Technology

Design and Simulation of Fault Detection Technique for NAND Based Memory Array...159
JAMUNA S[1], Murali Bharadwaja[1], Kishore Kumar Kalluri[1], Madhura R[1]
[1]Dayananda Sagar College of Engineering, India

A Testability Improvement Method of Combinational Circuits Based on the SDC Conditions...163
Yang Zeng[1,] Xiaole Cui[1]
[1]Peking University Shenzhen Graduate School

RTL design of 16-bit RISC Processor Using Vedic Mathematics...169
Nikitha S[1], Peram Varshitha[1], Niveditha K M[1], Mayuri Bhat K[1], Madhura R[1] [1]Dayananda Sagar college of Engineering

Improving At-Speed Test Coverage without compromising Test Time and reducing Test Cost in multi-partition SCAN Design...173
Jayesh Popat[1], Ramesh Devani[1], Jay Gohil[1]
[1]Microcircuits Innovations Pvt Ltd

Enhancing SRAM Array Security Through Transmission Gate-Based Logic Obfuscation...178
Bhavin Bhavani[1], Anupam Mathur[1], Sreeja Rajendran[1], Vinay Palaparthy[1], Yash Agrawal[1]
[1]Dhirubhai Ambani Institute of Information and Communication Technology

A Novel Differential 12T SRAM Bit-cell Structure with Improved SNM in 16nm FinFET Technology...182
Jay Gohil[1], Ramesh Devani[1], Jayesh Popat[1]
[1]Microcircuits Innovations Pvt Ltd

Testing Method for Embedded UltraRAM in Field Programmable Gate Arrays...189
Jiaqi Guo[1]
[1]School of Microelectronics, Fudan University, Shanghai

Design, Implementation and Characterization of a Novel Robust-by-Construction Arbiter PUF Circuit on Xilinx FPGAs...195
Sreekanth Balijabudda Venkata[1], Indrajit Chakrabarti[1], Rajat Subhra Chakraborty[1] [1]IIT Kharagpur

MEMFD: A Multi-EDT Multi-Fault Scan Chain Diagnosis Methodology with Deep Learning...201
Saman Aijaz Siddiqui[1], Uzair Ruhulamin Patel[1], Utsav Jana[2], Binod Kumar[1]
[1] IIT Jodhpur
[2] SUTD

SFCM-HT: Hardware Trojan Detection Based on Sequence Features with a Combination Model...207
Li Zhenghao[1], Yang Zhang[1], Xing Hu[1], Jialong Song[1], Shaoqing Li[1], Bin Liang[1]
[1]National University of Défense Technology

Accelerating Sequential Circuit Simulation with Spatial Locality Enhancement and Redundant Event Reduction...213
Jiaping Tang[1], Jing Ye[1], Huawei Li[1], Xiaowei Li[1]
[1]Institute of Computing Technology, Chinese Academy of Sciences

Improving Self-Fault-Tolerance Capability of Memristor Crossbar Using a Weight-Sharing Approach...219
DEV YADAV[1], Phrangboklang Lyngton Thangkhiew[2], F Lalchhandama[3], Kamalika Datta[4], Rolf Drechsler[5], Indranil Sengupta[6]
[1]National Institute of Technology Rourkela
[2]Indian Institute of Technology Guwahati
[3]Jawaharlal Nehru University
[4]DFKI
[5]University of Bremen, Germany
[6]IIT Kharagpur

LLM-aided Front-End Design Framework for Early Development of Verified RTLs...225
Vyom Gupta[1], Abhishek Yadav[2], Masahiro Fujita[3], Binod Kumar[2]
[1]Indian Institute of Information Technology Allahabad
[2]IIT-JODHPUR
[3]The University of Tokyo

ML Based Diagnosis for Fault Location in Digital Circuits...231
Habibur Rahaman[1], Sudip Ghosh[2], Subhajit Chatterjee[2]
[1]Indian Institute of Technology, Kharagpur
[2]Indian Institute of Engineering Science and Technology, Shibpur

Evaluating Different Fault Injection Abstractions on the Assessment of DNN SW Hardening Strategies...237
Giuseppe Esposito[1], Matteo Sonza Reorda[1], Juan-David Guerrero-Balaguera[1], Josie-Esteban Rodriguez-Condia[1]
[1]Politecnico di Torino

Towards Formal Verification for MAC-based In-Memory Computing...243
Fatemeh Shirinzadeh[1], Kamalika Datta[2], Saeideh Shirinzadeh[1], Abhoy Kole[1], Rolf Drechsler[2]
[1]DFKI
[2]University of Bremen, Germany

RTL Agent: An Agent-Based Approach for Functionally Correct HDL Generation via LLMs...249
Sriram Ranga[1], Rui Mao[1], Debjyoti Bhattacharjee[2], Erik Cambria[1], Anupam Chattopdhyay[1]
[1]Nanyang Technological University
[2]Imec

LLMs for Hardware Verification: Frameworks, Techniques, and Future Directions...255

Khushboo Qayyum[1], Sallar Ahmadi-Pour[2], Chandan Kumar Jha[2], Muhammad Hassan[2], Rolf Drechsler[2]
[1]DFKI GmbH
[2]University of Bremen

Security Concerns of Machine Learning Hardware...261
Chandan Karfa[1], Nilotpola Sarma[1], E Bhabani Eswar Reddy[1]
[1]IIT Guwahati

LLM vs HLS for RTL Code Generation: Friend or Foe?...267
Chandan Karfa[1], Sutirtha Bhattacharjee[2]
[1]IIT Guwahati
[2]Indian Association for the Cultivation of Science

Finite Element Analysis (FEA) Based Design Optimization of Ultrastable, High Finesse Optical Cavities for Portable Optical Atomic Clock Applications...273
Arijit Sharma[1], Himanshu Miriyala[1], Rishabh Pal[1]
[1]Indian Institute of Technology Tirupati

Experimental Realization of Quantum Memory and EPS-QKD...279
Kapil Jaiswal[1]
[1]Quantum AI Global

Quantum Key Distribution-Based Framework for Securing Encrypted Communications in Address Resolution Protocol Packet Capture...285
Amlan Chakrabarti[1]
[1]University of Calcutta

The Future is Hybrid: Next Generation Data Structures for Formal Verification...291
Rolf Drechsler[1], Christina Plump[2], Martha Schnieber[1]
[1]University of Bremen, Germany
[2]DFKI GmbH

Security Vulnerabilities in AI Hardware: Threats and Countermeasures...297
Rijoy Mukherjee[1], Sneha Swaroopa[1], Subhra Chakraborty[1]
[1]IIT Kharagpur

Secure AI Systems: Emerging Threats and Defense Mechanisms...303
Habibur Rahaman[1], Atri Chatterjee[1], Swarup Bhunia[1]
[1]University of Florida

Fault Testing in AI-Accelerators: A Review...309
Hafizur Rahaman[1], Bhargab B. Bhattacharya[2], Debesh K. Das[3], Subhajit Chatterjee[1]
[1] Indian Institute of Engineering Science and Technology, Shibpur
[2]ISI, India
[3]Jadavpur University Kolkatta