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TE1-2	A Simulation Study for Optimal Conditions of Singlemode Polymer Optical Waveguides in Chip-to-Chip Connections	Hiroki Ito, Yuji Furuta, Kenji Yanagisawa, Masaharu Kato, Hisashi Kaneda, Tomoharu Fujii, Shinko Electric Industries / Japan	**147**
TE1-3	Refractive Index Profile Analysis of Single Mode Polymer Optical Waveguide by Using Propagation-Mode Near Field Method	Masaki Matsumoto, Tomoharu Fujii, Kazuhiro Yoshida, Shinko Electric industries / Japan	**149**

TE2: Optoelectronics-2

11:30-13:10 Thurday, April 17

TE2-1	Reflowable Ceramics Multifiber Ferrule for Co-Packaged Optics	Alexander William Setiawan Putra, Kentaro Matsuda, Motohito Takezaki, Hakusan / Japan	**151**
TE2-2	Novel Passive Alignment Implementation Using 41°-Cleaved Fiber Array for Silicon Photonic Micro-Transceiver	Michiyo Kubo, Shigeru Kobayashi, Koichi Takemura, Makoto Kuwata, Kazuhiko Kurata, AIO Core / Japan	**153**
TE2-3 <Session Invited>	Fabrication and Transient Optical Response of 910nm Broadband Near-IR Remote Phosphor-converted LED	Atsushi Okuno[1], Jang Uk An[2], [1]Green Planets / Japan, [2]ALLIX / Korea	**-**

TE3: DMR-M-1

14:00-15:40 Thurday, April 17

TE3-1	A Novel FOWLP Process Emulator for Predicting Time-Dependent Plastic Effects in Multi-Step Accumulated Thermal-Mechanical Asymmetric Warpage	Shang-Feng Hsu, Kuo-Shen Chen, National Cheng-Kung University / Taiwan	**155**
TE3-2	Warpage Control Strategy of Embedded Die Packaging on SESUB Technology	Wei-Hong Lai, Chun-Yu Yen, Chung-Hung Lai, Tsung-Yuan Yang, Chin-Li Kao, Chen-Chao Wang, Advanced Semiconductor Engineering (ASE) / Taiwan	**157**
TE3-3	Micro-Bump Connection and Chip Warpage Control Using the Reflow Process	T. Igarashi, M. Togawa, M. Nakazawa, H. Iwamoto, Sony Semiconductor Solutions / Japan	**159**
TE3-4	Warpage Behavior of Three-Phase SiC MOSFET Power Module During Fabrication	Y. H. Liao[1], H. C. Cheng[1], Y. L. Liu[1], Y. C. Liu[2], K. S. Kao[2], T. C. Chang[2], [1]Feng Chia University, [2]Industrial Technology Research Institute / Taiwan	**161**

TE4: DMR-M-2

16:00-17:40 Thurday, April 17

TE4-1	Silica Fillers Embedded in Epoxy Molding Compound Cause Inner Stress Concentration	Ayumi Haginiwa[1], Masaya Ukita[1], Keisuke Wakamoto[1], Yuya Shitashige[2], Keizo Arai[2], Ken Nakahara[1], [1]ROHM, [2]Resinous Kasei / Japan	**163**
TE4-2	Direct Observation of Copper Oxidation as a Cause of Delamination at the Interface of Copper and Epoxy Molding Compounds	Keisuke Wakmaoto, Masaya Ukita, Ayumi Haginiwa, Ken Nakahara, ROHM / Japan	**165**
TE4-3	Comparasion of Thermomigration Velocity between Sn-Cu$_{0.7}$ and Ternary Sn-Bi-In Solder	Yifan Yao[1], Xingchao Mao[1], Yuanxing Duan[1], Qinglei Sun[1,2], K. N. Tu[1], Yingxia Liu[1], [1]City University of Hong Kong, [2]China University of Geosciences / China	**167**
TE4-4	Predictive Validity for Sintered Die-Attach Performance based on Cross-Sectional Morphology	Runhua Gao[1], Hiroaki Tatsumi[1], Takanori Kobatake[2], Minoru Ueshima[2], Hiroshi Nishikawa[1], [1]The University of Osaka, [2]Daicel / Japan	**169**

FA1: Advanced Packaging and Thermal

10:10-11:50 Friday, April 18

FA1-1 <Session Invited>	Innovations in Hybrid Bonding and Thermal Management for Advanced Packaging	Kuan-Neng Chen, National Yang Ming Chiao Tung University / Taiwan	**-**
FA1-2 <Session Invited>	Multistacking bonding technologies, die-level co-integration and their technical challenges	Masahisa Fujino, Institute of Microelectronics, A*STAR / Singapore	**-**
FA1-3 <Session Invited>	AI-Accelerated Multiscale Thermal & Mechanical Simulations for Advanced Packaging and IC Design	Alexander J Gabourie, DeepSim / US	**-**
FA1-4 <Session Invited>	Micro- and Nano-Scale Thermal Property Measurements for Advanced Semiconductor Packages Using Frequency-Domain Thermoreflectance Microscopy	Tomoya Uchiyama, ScienceEdge / Japan	**-**

FA2: Die Level Hybrid Bonding Technology

12:40-14:20 Friday, April 18

FA2-1 <Session Invited>	Die to Wafer Hybrid Bonding: from Challenge to a New Industry Standard	Pavel Seroglazov, BESI / Netherlands	**-**
FA2-2 <Session Invited>	Wafer Bonding Advances & 3D Applications	Hiroshi Yamamoto, EV Group / Japan	**-**
FA2-3 <Session Invited>	Suss Direct D2W Hybrid Bonding Solutions	Thomas Schmidt, Philippe Muller, SUSS MicroTec Solutions / Germany	**-**

FA3: Glass PKG-3
14:30-16:10 Friday, April 18

FA3-1	Examination of Panel-Level Manufacturing Methods for Glass Core Substrates	Shun Mitarai, Kiwamu Adachi, Takahiro Igarashi, Kosuke Seki, Naoki Kakoiyama, Yuto Tanaka, Shuichi Oka, Masashi Nakazawa, Hayato Iwamoto, Sony Semiconductor Solutions / Japan	**171**
FA3-2 <Session Invited>	Challenge for Glass Core Substrate with the Stress Analysis and Reliability	Satoru Kuramochi, Dai Nippon Printing / Japan	**-**
FA3-3 <Session Invited>	Multilayer Glass substrate (G-ALCS) for Advancing Packaging Innovation	Akira Tamura, FICT / Japan	**-**
FA3-4 <Session Invited>	Glass PKG Technology Trend & Core Items	Tetsuya Onishi, Grand Joint Technology / Hong Kong	**-**

FA4: Automation Technology for Wafer/Panel Level Process
16:30-18:10 Friday, April 18

FA4-1 <Session Invited>	Reimaging and Transforming Package Assembly and Test Manufacturing	Jeffrey S Pettintao[1,2], [1]Intel / US, [2]SATAS / Japan	**-**
FA4-2 <Session Invited>	Automated Material Handling System (AMHS) as Blood Vessels in a Semiconductor Factory	Kenji Kumagai, Wataru Kitamura, Murata Machinery / Japan	**-**
FA4-3 <Session Invited>	Automation Technology for Wafer/Panel Level Process	Shinichi Nakashima, DAIFUKU / Japan	**-**
FA4-4 <Session Invited>	Automated Material Handling System	Mitsunori Harada, SHARP / Japan	**-**
FA4-5 <Session Invited>	Automatic Transportation AMR (Autonomous Mobile Robot) System For Advanced Back-end Processes	Kazuma Nakaguchi, SINFONIA TECHNOLOGY / Japan	**-**

FB1: Glass/Plating Process
10:10-11:50 Friday, April 18

FB1-1 <Session Invited>	JPCA Technology Roadmap for Glass Substrates	Henry H. Utsunomiya, Interconnection Technologies / Japan	**-**
FB1-2 <Session Invited>	Low CTE Copper Electrodeposit	Kazuo Kondo, Anh Nahat, Fine Feature Electrodeposition Laboratory / Japan	**-**
FB1-3	Laser Applications in Micro-machining of Glass Material Substrates	Hsiang-Chen Hsu[1], Shih-Jeh Wu[1], Wen-Fei Lin[2], Shui-Cheng Huang[1], Pei-Chieh Chin[1], [1]I-Shou University, [2]E&R Engineering / Taiwan	**173**
FB1-4	Predicted Cu Plating Thickness Distribution in Fanout Panel Level Package with Global/Local Model	Yi-Lun Hung, Yung-Sheng Lin, Min-Yan Tsai, Mingtzung Kuo, Ling-yuan Chang, Chen-Chao, Wang, Ping-Feng Yang, Chin-Pin Hung, Advanced Semiconductor Engineering (ASE) Group / Taiwan	**175**

FB2: Interposer
12:40-14:20 Friday, April 18

FB2-1	Multi-Stepped Solder Resist Patterning Technology for Advanced Packaging	Meiten Koh[1], Raimu Kasuga[1], Yuji Toyoda[2], [1]Taiyo Ink Mfg, [2]Mitsubishi Paper Mills / Japan	**177**
FB2-2	Moisture Diffusion Analysis of FOCoS Package During Assembly Processes	Dao-Long Chen, Tang-Yuan Chen, Fan-Yu Min, Wei-Hang Tai, Chen-Hung Lee, Chen-Chao Wang, Chih-Ping Hung, Advanced Semiconductor Engineering / Taiwan	**179**
FB2-3	Anti-Oxidation for Copper by Galvanic Replacement	Yu-hao Chou, Kun-yuan Zeng, Shih-kang Lin, National Cheng Kung University / Taiwan	**181**
FB2-4	Adhesion Characteristics of Directly Sputtered Copper Seed Layer on Cycloolefin Polymer with Atmospheric Pressure Plasma Treatment	A. Shimizu[1,2], S. Endo[1], [1]Ushio, [2]Gifu University / Japan	**183**

FB3: Printing Process

14:30-16:10 Friday, April 18

FB3-1	Evaluation of Printing Chracteristics of Inks Containg Plasmonic Nanoparticles	Akinobu Yamaguchi[1], Toshiya Yasunaga[2], Kyoko Namura[3], Motofumi Suzuki[3], Takao Fukuoka[3,4], [1]Toyo University, [2]Aichi Gakuin University, [3]Kyoto University, [4]Archilys / Japan	**185**
FB3-2	Silver-Based Metal-Organic Decomposition with 3D Inkjet Printing for Selective Package-level EMI Shielding	M. H. Chen, W. H. Wang, R. J. Kao, Y. E. Yeh, Advanced Semiconductor Engineering / Taiwan	**187**
FB3-3	Inducing Dynamic Percolation of Stretchable Printed Wires During Three-dimensional Forming	Rina Aida, Masahiro Inoue, Gunma University / Japan	**189**
FB3-4	Fine Printing by Gravure Offset Using Lowtemperature Sintered Copper	Shingo Ohshima, Chisato Oyama, Yoshihiro Ohyama, Ikeda Hideki, KOMORI / Japan	**191**

FB4: Adv. Cu Interconnect Technologies for Chiplets

16:30-18:10 Friday, April 18

FB4-1 <Session Invited>	Chip-let Heterogeneous Integration Packaging Based on Fan-Out Interposer Technology	Jung Won Lee, nepes / Korea	**-**
FB4-2 <Session Invited>	Advanced Substrate for High Performance AI Computing System	Yu-Hua Chen, Unimicron / Taiwan	**-**
FB4-3 <Session Invited>	Integrated Systems Approach from an Equipment Supplier's Perspective in the Advanced Packaging Era	Hirotaka Satori, Ji Chul Yang, EBARA / Japan	**-**
FB4-4 <Session Invited>	High-Resolution Direct-Write System for Advanced Package by Unique Spatial Light Modulator	Yuichi Nishimoto, SCREEN Holdings / Japan	**-**

FC1: Advanced Packaging-5

10:10-11:50 Friday, April 18

FC1-1	Elimination of Leakage in NaOH-activated Cu/SiO_2 Hybrid Bonding for Plasma-Free Surface Activation Scheme	Huai-En Lin[1], Yu-Xiang Huang[1], Wei-Lan Chiu[2], Hsiang-Hung Chang[2], Chih Chen[1], [1]National Yang Ming Chiao Tung University (NYCU), [2]Industrial Technology Research Institute (ITRI) / Taiwan	**193**
FC1-2	Sub 100 nm Grain Size Electroplated Copper for Low Temperature Bonding Applications	Jian-Yuan Huang[1], Dinh-Phuc Tran[1], Kang-Ping Lee[1], Tsung-Chuan Chen[2], Yao-Tsung Chen[2], Emile Kuo[2], Stream Chung[2], Chih Chen[1], [1]National Yang Ming Chiao Tung University, [2]Chemleaders / Taiwan	**195**
FC1-3	Sintered Cu-to-Cu Joints Using Cu Dendritic Structure Formed by a Dynamic Hydrogen Bubble Template with Cetyltrimethylammonium Bromide	Ji-Hyun Kim, Hiroaki Tatsumi, Hiroshi Nishikawa, The University of Osaka / Japan	**197**
FC1-4	Investigation of Cu-to-Cu Bonding Featuring Indium Passivation and a Tin Diffusion Barrier Layer	Y. C. Tseng[1], Y. S. Lin[2], Y. C. Hung[2], C. R. Kao[1], [1]National Taiwan University, [2]Advanced Semiconductor Engineering (ASE) Group / Taiwan	**199**

FC2: Advanced Packaging-6

12:40-14:20 Friday, April 18

FC2-1	Development of Warpage Control Techniques in Multi-Chip Fan-Out System-in Package (SiP) Using Redistribution Layer Technology	Jr-Wei Peng, Chih-Cheng Hsiao, Chin-Hung Wang, Industrial Technology Research Institute (ITRI) / Taiwan	**201**
FC2-2	Advanced Packaging Solutions by Integrating 2.5D/3D Chiplet, Wafer Panel Level Package	K. Izusawa, S. Teramoto, Y. Kajikawa, S. Hayashiguchi, T. Kubota, TOWA / Japan	**203**
FC2-3	Cu Pilliar Plating Process on Large Panel Fan-Out for High Performance Computing Application	Powei Lu, Ming Tzung Kuo, Jeffrey Yang, Yuan Feng Chiang, Jen Kuang Fang, Advanced Semiconductor Engineering (ASE) / Taiwan	**205**
FC2-4	A Novel UV Curable Wafer Back Side Protection Film	Jun Maeda, Toshiki Inoue, Soki Sato, Shigeyuki Yamashita, Shinya Takyu, LINTEC / Japan	**207**

FC3: Advanced Packaging-7

14:30-16:10 Friday, April 18

FC3-1 <Session Invited>	PLP Market Trend	Yik YeeTan, Yole Group / France	**-**
FC3-2	Next Generation Chiplet Technology Development: Focusing on Fine RDL Patterning	M. Sasago[1,6], H. Nishizawa[2,4,6], T. Doi[2,6], M. Ozono[3,6], H. Kimuro[3,6], S. Yamamoto[2,4], K. Suzuki[4], S. Takahashi[5,6], Y. Minami[5,6], M. Yasuda[1,6], Y. Hirai[1,6], T. Saito[1,6], [1]Osaka Metropolitan University (OMU), [2]Doi Laboratory, [3]National Institute of Advanced Industrial Science and Technology (AIST), [4]Kyushu Institute of Technology, [5]Lithotech Japan, [6]RCS consortium / Japan	**209**
FC3-3	Investigation from the Lithography of the Possible of Forming Less Than 8 µm Pitch Required for Advanced Packaging	Yu Abe, Naoya Sohara, Ryotaro Takahashi, Toshimitsu Arai, Hirosuke Takamatsu, USHIO / Japan	**211**
FC3-4	Advanced Post Overlay Compensation for Enhanced Lithography Overlay Accuracy for Next-Generation AICS Packaging	John Chang, Keith Best, Xin Song, Timothy Chang, Onto Innovation / US	**213**

FC4: Advanced Packaging-8

16:30-18:10 Friday, April 18

FC4-1	Reliability and Warpage of High Density Package Using Organic Interposer for Heterogeneous Integration	Yoshihiro Kobayashi, Shota Miki, Shinko Electric industries / Japan	**215**
FC4-2	RDL Formation Using Low Df Thermosetting Film (Progress of the Chiplet Integration Platform Consortium in Japan)	Yusuke Naka[1], Meiten Koh[1], Ichiro Kono[2], Yasuhiro Morikawa[3], Takafumi Fukushima[4], Yoichiro Kurita[5], [1]Taiyo Ink MFG, [2]AOI Electronics, [3]ULVAC, [4]Tohoku University, [5]Institute of Science Tokyo / Japan	**217**
FC4-3	Surface Modification for PI-to-PI Direct Bonding	Yu-Kuang Chen, Chang-Ju Hsu, Jenn-Ming Song, National Chung Hsing University / Taiwan	**219**
FC4-4	Advancements in IC Substrate Packaging: A Process to Metallize Embedded Trench for Enhanced Performance and Sustainability	Saminda Dharmarathna[1], Fengqi Zhang[1], Maddux Sy[2], Howard Chu[2], Leslie Kim[1], Brian Gokey[1], Ernie Long[1], [1]MacDermidAlpha Electronics Solutions / US [2]MacDermidAlpha Electronics Solutions / Taiwan	**221**

FD1: 5G, Wiewless & Components

10:10-11:50 Friday, April 18

FD1-1	A 28-GHz 2×2 Antenna Array Integrated with a Butler-Matrix Beamformer IC Based on AiP Technology	Wen-Chun Hsiao, Hong-Sheng Huang, Yu-Chang Hsieh, Chia-Ching Chu, Sheng-Chi Hsieh, Chen-Chao Wang, Advanced Semiconductor Engineering / Taiwan	**223**
FD1-2	Analysis and Optimization of a Compact 1x4 Array Antenna for 5G Application	Hong-Sheng Huang, Wen-Chun Hsiao, Yu-Chang Hsieh, Chia-Ching Chu, Sheng-Chi Hsieh, Chen-Chao Wang, Advanced Semiconductor Engineering / Taiwan	**225**
FD1-3	Evaluation of Effective Permittivity of Multilayer Strip-Line Structure With Air Layers Under Substrate Deformation and Prototype of Deformation Suppression Structure	USHIYAMA Taiyo[1], SASAKI Mai[1], TOMIOKA Sayu[1], HAZEMOTO Tsuyoshi[1], ONO Satoshi[1], MASUI Sho[2], KOJIMA Takafumi[2], SAKAI Takeshi[1], [1]University of Electro-Communication, [2]National Astronomical Observatory Japan / Japan	**227**
FD1-4	Effects of Magnetic Field Exposure on Emotional Responses in Living Organisms	Daiki Hirabayashi, Yuno Matsuyama, Daisuke Yamada, Akiyoshi Saitoh, Takahiko Yamamoto, Tokyo University of Science / Japan	**229**

FD2: Thermal Management-1

12:40-14:20 Friday, April 18

FD2-1 <Session Invited>	Thermal Resistance Cross Interfaces in Electronics	Zhe Cheng, Peking University / China	**-**
FD2-2 <Session Invited>	Enhanced Performance of High-Power Density Semiconductor Chips Using CVD Diamond Heat Spreaders	Ian Friel, Element Six / UK	**-**
FD2-3	Optimization of Baking Temperature for Minimization of Interfacial Thermal Resistance in Polymer/ SiC Bilayer Structure Using Optical-Interference Contactless Thermometry (OICT)	Jiawen Yu, Hiroaki Hanafusa, Seiichiro Higashi, Hiroshima University / Japan	**231**
FD2-4	A fundamental Study on Interfacial Properties of Indium Thermal Interface Materials	Po-hsiang Juan, Kuan-chen Kung, Shih-kang Lin, National Cheng Kung University / Taiwan	**233**

FD3: Thermal Management-2

14:30-16:10 Friday, April 18

FD3-1 <Session Invited>	Two-Phase In-Situ Thin Liquid Film Cooling for Computing Module with 600W/cm^2 Heat Flux	Qidong Wang, IMECAS / China	**-**
FD3-2	Improvement of Air-Cooling Performance Utilizing Breathing Phenomenon Induced by Corrugated Lotus Copper Fins	R. Kubota[1], K. Yuki[1], K. Yuki[1], T. Ogushi[2], M. Murakami[2], T. Ide[2], [1]Tokyo University of Science, [2]Lotus Thermal Solution / Japan	**235**
FD3-3	Cu/Diamond Composite Heat Spreader for Thermal Management of Advanced Electronic Devices	Masato Sakai, Satoshi Teraji, Tasuku Hamano, Ishihara Chemical / Japan	**237**

FD4: Thermal Management-3

16:30-18:10 Friday, April 18

FD4-1 <Session Invited>	Thermal Test Vehicles for Characterization of the Thermal Performance for Large Silicon Chips	Dongkai Shangguan, Thermal Engineering Associates / US	**-**
FD4-2	Power Devices Sandwiched Between Silver-Diamond Parts for High Performance Module	R. Khazaka[1], A. Casado Ramoneda[1,2], Y. Avenas[2], T. Youssef[1], C. Gautier[1], S. Azzopardi[1], T. Murakami[3], M. Tamaru[3], [1]Safran SA, [2]Univ. Grenoble Alpes / France, [3]TECNISCO / Japan	**239**
FD4-3	Thermal Transfer Analysis by Phonon Vibrations at Interface Between Filler and Resin in Thermal Interface Material	Osamu Arao, Masashi Kitsunezuka, Akira Shintai, DENSO / Japan	**241**
FD4-4	Verification of Differences in Thermal Resistance of Cascode Device Packages Due to Heating Power Ratio of Heat Sources	Aiko Shimada, Wasanthamala Badalawa, Yoshitaka Aoki, Tomoaki Hara, Siemens / Japan	**243**

FE1: DMR-M-3

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FE1-1	High-Speed Ball Shear Mechanism on Ni-Au Substrate & Thermal Aging Effect	Nien-Chun Lin, Hsin-Chih Shih, Ching-I Tsai, Chin-Li Kao, Chen-Chao Wang, C.P. Hung, Advanced Semiconductor Engineering (ASE) / Taiwan	**245**
FE1-2	Study on the Global-Local Method with Critical Mesh Size Control for 3D Wafer-Level Packaging Simulation Time Reduction	C. A. Yang, K. N. Chiang, , National Tsing Hua University / Taiwan	**247**
FE1-3	Advanced Short Defect Repair Technique for Enhancing Yield in Packaging Architectures	Adam Ginsburg, Oded Mor, Guy Levi, Guy Amrani, KLA / Israel	**249**
FE1-4	Characterization of Signal Variations During the Self-Sharpening Process of Ceramic Diamond Grinding Wheels	Yu-Kun Lin, Feng Chia University / Taiwan	**251**

FE2: DMR-M-4

12:40-14:20 Friday, April 18

FE2-1	Simulation of CUF Fillet Height and Minimize Void on Reliability	Tzu Chieh Chien, Yuan Hung Sun, Chao Lin Shih, Hui Chung Liu, Lu Ming Lai, Kuang Hsiung Chen, Advanced Semiconductor Engineering / Taiwan	**253**
FE2-2	Sine and Random Vibration Analysis of SAC305 Electronic Assemblies Based on PCB Strain	J-B. Libot, P. Milesi, Hooke Electronics / France	**255**
FE2-3	Thermal Stress-Strain Behavior of Cu on Metallized Si_3N_4 Substrate Under Thermal Cycling Test by Digital Image Correlation	Minh Chu Ngo, Hiroyuki Miyazaki, Kiyoshi Hirao, Tatsuki Ohji, Manabu Fukushima, National Institute of Advanced Industrial Science and Technology (AIST) / Japan	**257**
FE2-4	Optimized Flux-less Bonding Process for High Throughput Using Simplified Equipment	Takayuki Miyoshi[1], Kentaro Mihara[1], Takashi Hare, Katsumi Terada[1], Toyoharu Terada[1], Chienshuo Huang[2], Yuhao Lo[2], Jun Mizuno[2], [1]Toray Engineering / Japan, [2]National Cheng Kung University / Taiwan	**259**

FE3: Materials for High Speed Application

14:30-16:10 Friday, April 18

FE3-1 <Session Invited>	Thin-Film Lithium Niobate Based High-Speed Modulator and Future Perspective	Rai Kou[1], Toshiya Murai[1], Kazumasa Takabayashi[2], Masahiko Imai[2], Guangwei Cong[1], Koji Yamada[1], [1]AIST, [2]Fujitsu Optical Components / Japan	**-**
FE3-2	High-Speed Signal Transmission Rigid Substrate Fabricated by Silver-Seed Semi Additive Process	Rei Tamura, Akira Murakawa, Norimasa Fukazawa, Wataru Fujikawa, DIC / Japan	**261**
FE3-3	Material Property Extraction Using Microstrip Antennas for mm-Wave Applications	Tian-Lin Zhanz, Sung-Mao Wu, Bo-Yang Jheng, Guan-Yu Hong, National University of Kaohsiung / Taiwan	**263**

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P02	Exploring the Potential of Fly Cutting for Polymer Planarization in Cu/PDMS Hybrid Bonding	Suin Jang, Junyoung Choi, Dongmyeong Lee, Hoogwan Lee, Sarah Eunkyung Kim, Seoul National University of Science and Technology / Korea	**267**
P03	Effect of Noble Metal Passivation Deposited by ECD on Cu Surface for Low-Temperature Cu-to-Cu Bonding	Dongmyeong Lee, Junyoung Choi, Suin Jang, Hoogwan Lee, Sarah Eunkyung Kim, Seoul National University of Science and Technology / Korea	**269**
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P05	Study of Low Temperature Cu-to-Cu Bonding using Reducing Plasma	Hoogwan Lee, Dongmyeong Lee, Junyoung Choi, Suin Jang, Sarah Eunkyung Kim, Seoul National University of Science and Technology / Korea	**273**
P06	Low-Temperature Femtosecond Laser Processing for Enhanced Via Hole Morphology in Semiconductor Packaging	Taesik Kim[1,2], Jaebeom Lee[1,2], Seon-Jin Choi[2], Jiyong Park[1,3], [1]Korea Institute of Industrial Technology (KITECH), [2]Hanyang University, [3]Korea National University of Science and Technology (UST) / Korea	**275**
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P08	Simulation of Signal Integration and Power Integration in Advanced Packaging Circuit Design	Shu-Chin Huang, Sung-Mao Wu, National University of Kaohsiung / Taiwan	**279**
P09	Analysis of Parasitic Effects in Packaging with RDL	Jyun-yu Chen, Sung-Mao Wu, Shin-Shian Wu, National University of Kaohsiung / Taiwan	**281**
P10	Parametric Investigation of Surface Morphology in Through Glass Vias (TGVs) Fabricated via Femtosecond Laser Processing	Jaebeom Lee[1,2], Taesik Kim[1,2], Seung Hwan Lee[2], Jiyong Park[1,3], [1]Korea Institute of Industrial Technology (KITECH), [2]Hanyang University, [3]Korea National University of Science and Technology (UST) / Korea	**283**