2025 IEEE 75th Electronic Components and Technology Conference (ECTC 2025)

Dallas, Texas, USA 27-30 May 2025

Pages 1-589



IEEE Catalog Number: ISBN:

CFP25ECT-POD 979-8-3315-3933-7

Copyright © 2025 by the Institute of Electrical and Electronics Engineers, Inc. All Rights Reserved

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

*** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.

IEEE Catalog Number:CFP25ECT-PODISBN (Print-On-Demand):979-8-3315-3933-7ISBN (Online):979-8-3315-3932-0

ISSN: 0569-5503

Additional Copies of This Publication Are Available From:

Curran Associates, Inc 57 Morehouse Lane Red Hook, NY 12571 USA Phone: (845) 758-0400

Fax: (845) 758-2633

E-mail: curran@proceedings.com Web: www.proceedings.com



2025 IEEE 75th Electronic Components and Technology Conference (ECTC) ECTC 2025

Table of Contents

Foreword	lxxiii
ECTC 2025 Executive Committee	
ECTC 2025 Program Committee	. lxxviii
Session 1: Processing and Packaging Articles for 3D Integration	
SoW-X: A Novel System-on-Wafer Technology for Next Generation AI Server Application Po-Chang Shih (Taiwan Semiconductor Manufacturing Company, Ltd, R.O.C.), An-Jhih Su (Taiwan Semiconductor Manufacturing Company, Ltd, R.O.C.), King-Ho Tam (Taiwan Semiconductor Manufacturing Company, Ltd, R.O.C.), Tze-Chiang Huang (Taiwan Semiconductor Manufacturing Company, Ltd, R.O.C.), Kris Chuang (Taiwan Semiconductor Manufacturing Company, Ltd, R.O.C.), and John Yeh (Taiwan Semiconductor Manufacturing Company, Ltd, R.O.C.)	1
Face-Down Bonding and Heterogeneous Chiplet Integration by using Bumpless Chip-on-Wafe (COW) with Waffle Wafer Technology	
Electrical Properties and Reliability of Back-Side Redistribution Layer Based on Inorganic Dielectric in 3D Stacked Memory Package	12

A Novel 3D Heterogeneous Integration using 2 µm Bond Pitch Die-to-Wafer Hybrid Cu Bonding and Wafer Reconstruction Process
Enabling Chip-to-Wafer Hybrid Bonding Scaling to 1um Pitch With Optimal Power Delivery Using New Bond Via Architectures
No Flux Thermocompression Bonding: Adapting to the Future
Integration Solution for Thin D2W Hybrid Bonding for Yield and Reliability
Session 2: Co-Packaged Optics
Heterogeneous Integration of Fiber-Based Co-Packaged Optics with EMIB Technology: Assembly, Performance, and Reliability

6.4Tbps, 224Gbps/Lane Co-Packaged Optical Engines with Fine Pitch Through-Package
Interconnects: Powering AI/ML and Next-Gen Data Centers
Flip-Chip Photonic-Electronic Integration Platform for Co-Packaged Optics using a Glass
Substrate with Vertically-Coupled Beam Expanding Lens Yasutaka Mizuno (Sumitomo Electric Industries, Ltd., Japan), Kunio Kobayashi (Sumitomo Electric Industries, Ltd., Japan), Shingo Nakamura (Sumitomo Electric Industries, Ltd., Japan), Masaki Migita (Sumitomo Electric Industries, Ltd., Japan), Hajime Arao (Sumitomo Electric Industries, Ltd., Japan), Tetsuya Nakanishi (Sumitomo Electric Industries, Ltd., Japan), Hiroshi Uemura (Sumitomo Electric Industries, Ltd., Japan), Keiji Tanaka (Sumitomo Electric Industries, Ltd., Japan), Katsumi Uesaka (Sumitomo Electric Industries, Ltd., Japan), Mami Miyairi (FICT LIMITED, Japan), Yoshikatsu Ishizuki (FICT LIMITED, Japan), and Yoichiro Kurita (Institute of Science Tokyo, Japan)
Optical and Electrical Characterization of a Compact Universal Photonic Engine
Large-Scale Glass Waveguide Circuit for Board-Level Optical Interconnects Between Faceplate and Co-Packaged Optical Transceivers
All-SMF Arrays for Co-Packaged Optics: Optimizing Cost, Complexity and Performance

A +21-dBm per Channel Operation of a 16-Channel CWDM ELSFP Module in Practical Air-Cooling Conditions
Kohei Umeta (Furukawa Electric Co., Ltd., Japan), Taketsugu Sawamura (Furukawa Electric Co., Ltd., Japan), Yuki Shiroishi (Furukawa
Electric Co., Ltd., Japan), and Hideyuki Nasu (Furukawa Electric Co., Ltd., Japan)
Session 3: Hybrid Bonding Materials and Processing for Advanced Packaging
Morphological Microstructure Characterization and Optimisation of Nanocrystalline Copper Deposition for Fine-Pitch Hybrid Bonding Cu/SiO2 at Low Temperature
Wafer-to-Wafer Bonding With Ultralow Thermal Resistance and High Bonding Energy
Novel Polymer for Hybrid Bonding with Precise Tunable Crosslink Density
Hybrid Bonding With Particle Accommodation Using Polymer Dielectric: Design, Process and Yield Study
Characterization of Self-Nanoparticulated Cu-Cu Interconnection for Low-temperature Hybrid Bonding
Ryotaro Kawashima (Tohoku University), Hirokatsu Sakamoto (Daicel Corporation), Bungo Tanaka (Tohoku University), Tetsu Tanaka (Tohoku University), and Takafumi Fukushima (Tohoku University)

AlN Gap-Fill Process by Aerosol Deposition Method for Application in 3D-IC Packaging
Effect of Grain Size on Cu-Cu Bonding Quality for Fine-Pitch Hybrid Bonding Application
Session 4: Large Package Manufacturing and Panel Level Processing
Package Warpage Reduction for Large CoWoS-R Packages
Process Development and Reliability Investigation of 120 mm x 120 mm Large 2.5D Package with Low Melting Temperature Solder
New Silicon Capacitor Solutions with Over 1mm -Thick Core Based Embedded Substrate for Extremely Large Package Platform
Board-Level Assembly Challenges and TIM Selections for the Large-Size FCBGA Packages
Yield Prediction Technology A Game Changer for Cutting Costs and Reducing Ramp Time in FOPLP Lithography

Glass-Core Advanced Packaging Substrate Post-Dicing Die Strengths Comprehensive Comparisons for Different Singulation Methods - Dicing Induced SeWaRe Failures Re-Visited Ten Years Later
Substrate
Session 5: Advanced Design for Heterogeneous Integration
Enabling 20 Tb/s/mm Die-to-Die Bandwidth Density with Advanced Packaging Technologies 161 Zhiguo Qian (Intel Corporation, United States) and Kemal Aygun (Intel Corporation, United States)
Quantifying Signal Return Path Imperfections on Eye Aperture in Die-to-Die Communication 165 Nicolas Izquierdo (Qualcomm Technologies, Inc., USA), Jiawei Zhang (Qualcomm Technologies, Inc., USA), Manoj Rafalia (Qualcomm Technologies, Inc., USA), Jaimeen Shah (Qualcomm Technologies, Inc., INDIA), Eric Foronda (Qualcomm Technologies, Inc., USA), Chan Qian (Qualcomm Technologies, Inc., USA), and Gerardo Romo (Qualcomm Technologies, Inc., USA)
High-speed Packages for the Chiplet Era
Power Integrity and Circuit Characteristics of Integrated Voltage Regulator (IVR) in CoWoS® Advanced Packaging Technology

Multi-Chiplet Power Delivery Network (PDN) Co-optimization Considering Current Spectrum by	
Deep Reinforcement Learning-based Decoupling Capacitor Placement	31
Haeseok Suh (Korea Advanced Institute of Science and Technology	
(KAIST)), Hyunjun An (Korea Advanced Institute of Science and	
Technology (KAIST)), Haeyeon Kim (Korea Advanced Institute of Science	
and Technology (KAIST)), Seonguk Choi (Korea Advanced Institute of	
Science and Technology (KAIST)), Taesoo Kim (Korea Advanced Institute	
of Science and Technology (KAIST)), Keeyoung Son (Korea Advanced	
Institute of Science and Technology (KAIST)), Keunwoo Kim (Korea	
Advanced Institute of Science and Technology (KAIST)), Jiwon Yoon	
(Korea Advanced Institute of Science and Technology (KAIST)),	
Byeongmok Kim (Korea Advanced Institute of Science and Technology	
(KAIST)), Youngsu Yoon (Korea Advanced Institute of Science and	
Technology (KAIST)), Jaegeun Bae (Korea Advanced Institute of Science	
and Technology (KAIST)), and Joungho Kim (Korea Advanced Institute of Science and Technology (KAIST))	
RF Si interposer platform for chiplets based heterogenous systems	39
Xiao Sun (imec, Belgium), Siddhartha Sinha (imec, Belgium), Martijn	
Huynen (UGent-imec, Belgium), Reinier Broucke (UGent-imec, Belgium),	
Melina Lofrano (imec, Belgium), Vladimir Cherman (imec, Belgium),	
Hamideh Jafarpoorchekab (imec, Belgium), Damien Leech (imec, Belgium),	
Angel Uruena (imec, Belgium), Ehsan Shafahian (imec, Belgium), Nelson Pinho (imec, Belgium), Francois Chancerel (imec, Belgium), Koen Kennes	
(imec, Belgium), Sam Lemey (UGent-imec, Belgium), Andy Miller (imec,	
Belgium), Eric Beyne (imec, Belgium), and Nadine Collaert (imec,	
Belgium)	
A Heterogeneous Integrated Low Noise Amplifier with High-Q Si-Interposer Inductor for Dual	דינ
(Ka/V)-Band Millimeter Wave Applications 19	"/
Mei Sun (Agency for Science, Technology and Research (A*STAR), Singapore), Dan Lei Yan (Agency for Science, Technology and Research	
(A*STAR), Singapore), Jun Wei Ong (Agency for Science, Technology and	
Research (A*STAR), Singapore), Pei Siang Lim (Agency for Science,	
Technology and Research (A*STAR), Singapore), Aisyah Binte Kuyob	
(Agency for Science, Technology and Research (A*STAR), Singapore), Jia	
Qi Wu (Agency for Science, Technology and Research (A*STAR),	
Singapore), Yong Liang Ye (Agency for Science, Technology and Research	
(A*STAR), Singapore), Teck Guan Lim (Agency for Science, Technology	
and Research (A*STAR), Singapore), and Tshun Chuan Chai (Agency for	
Science, Technology and Research (A*STAR), Singapore)	
Session 6: AI - ML and Emerging Modeling Methods	
ocsion of the live and emerging wiodening wiemous	
NAND Package Warpage Prediction and Design with Tolerance Through Machine Learning 20)2
Min Lin (Western Digital, USA), Chaolun Zheng (Western Digital, USA),	
Yuhang Yang (Western Digital, USA), Ning Ye (Western Digital, USA), and Bo Yang (Western Digital, USA)	

Compact Models for Nonlinear Thermo-Mechanical Simulations of Chiplets in Automotive
Peridynamics Enabled Digital Image Correlation for Small Scale Defect Detection
DiffChip: Thermally Aware Chip Placement with Automatic Differentiation
Support Vector Algorithm-Driven Simulation for Predicting Mechanical Performance in High-Power Modules
High-Power Modules
Advanced Numerical Modeling of Microstructure Effect on Fine Cu Redistribution Lines Under
Electric Current Stressing
Deep Clustering Based Boundary-Decoder Net for Inter and Intra Layer Stress Prediction of
Heterogeneous Integrated IC Chip
Session 7: High Performance Computing and Design Challenges and Solutions
Fine Pitch High Density CoWoS-R Package with 1.4/1.4um RDL Lines and 3um via CD

Development of Embedded Multi Si Bridge Package in Panel Level Process for HPC/AI	054
Applications Hyeji Han (Samsung Electronics Co, Ltd, Korea), Jieun Park (Samsung Electronics Co, Ltd, Korea), Mijin Park (Samsung Electronics Co, Ltd, Korea), Jeongho Lee (Samsung Electronics Co, Ltd, Korea), Wonkyoung Choi (Samsung Electronics Co, Ltd, Korea), and Dae-Woo Kim (Samsung Electronics Co, Ltd, Korea)	251
Self-Alignment of Active Si Bridge using Solder Joints Capillary Forces	. 256
BBCube 3D: Fully Vertical Heterogeneous Integration of DRAMs and xPUs using a New Power	264
Distribution Highway Norio Chujo (Institute of Science Tokyo, Japan), Hiroyuki Ryoson (Institute of Science Tokyo, Japan), Koji Sakui (Institute of Science Tokyo, Japan), Shinji Sugatani (Institute of Science Tokyo, Japan), Masao Taguchi (Institute of Science Tokyo, Japan), and Takayuki Ohba (Institute of Science Tokyo, Japan)	264
EMIB-TSV Advanced Packaging Technology - EMIBTMS Next Evolution Gang Duan (Substrate Packaging Technology Development, Intel Foundry, USA), Yingying Zhang (Substrate Packaging Technology Development, Intel Foundry USA), Andrey Gunawan (Substrate Packaging Technology Development, Intel Foundry, USA), Yuxin Fang (Substrate Packaging Technology Development, Intel Foundry, USA), Johan Mousavi (Substrate Packaging Technology Development, Intel Foundry, USA), Amey Anant Apte (Chandler Assembly Technology Development, Intel Foundry, USA), Numair Ahmed (Substrate Packaging Technology Development, Intel Foundry, USA), Shruti Sharma (Substrate Packaging Technology Development, Intel Foundry, USA), Sid Alur (Substrate Packaging Technology Development, Intel Foundry, USA), Anil Chandolu (Wafer Assembly Technology Development, Intel Foundry Oregon, USA), Xinyu Li (Substrate Packaging Technology Development, Intel Foundry, USA), Manni Mo (Substrate Packaging Technology Development, Intel Foundry, USA), Jesse Jones (Substrate Packaging Technology Development, Intel Foundry, USA), Robin McRee (Substrate Packaging Technology Development, Intel Foundry, USA), Rungmai Limvorapitux (Substrate Packaging Technology Development, Intel Foundry, USA), Chandra Subramani (Substrate Packaging Technology Development, Intel Foundry, USA), Tarek Ibrahim (Substrate Packaging Technology Development, Intel Foundry, USA), Ravi Eluri (Advanced Design Technology and Systems, Intel Foundry, USA), Sai Agraharam (Advanced Design Technology and Systems, Intel Foundry, USA), and Rahul Manepalli (Substrate Packaging Technology Development, Intel Foundry, USA), Sid Kumar (Advanced Design Technology and Systems, Intel Foundry, USA), and Rahul Manepalli (Substrate Packaging Technology Development, Intel Foundry, USA)	269

Co-Packaged Optics (CPO) Technology Full Module Test Vehicle Demonstrations	<u>?</u> 74
Signal, Power, and Thermal Integrity Co-Design for AI Accelerator ASIC and HBM3 on Silicon Interposer 2.5D-IC Chiplet Integration	282
Session 8: Novel Structures and Processes for Chip-to-Wafer Hybrid Bonding	
 2 μm Pitch Direct Die-to-Wafer Hybrid Bonding using Surface Protection During Wafer Thinning and Die Singluation	287
Innovative SoIC® Cool-Stacking Technology to Overcome the Thermal Wall of Future High Performance Compute	292
Influences of Chip Shape on Scaling in Chip-on-Wafer Hybrid Bonding Koki Onishi (Sony Semiconductor Solutions Corporation, Japan), Sotetsu Saito (Sony Semiconductor Solutions Corporation, Japan), Toru Osako (Sony Semiconductor Solutions Corporation, Japan), Takaaki Hirano (Sony Semiconductor Solutions Corporation, Japan), Takahiro Kamei (Sony Semiconductor Solutions Corporation, Japan), Naoki Ogawa (Sony Semiconductor Solutions Corporation, Japan), Suguru Saito (Sony Semiconductor Solutions Corporation, Japan), Yoshiya Hagimoto (Sony Semiconductor Solutions Corporation, Japan), and Hayato Iwamoto (Sony Semiconductor Solutions Corporation, Japan)	<u>2</u> 97

Warpage Engineering in C2W Hybrid Bonding using Inter-Die Gap Fill Dielectrics for 2.	
Warpage Engineering in C2W Hybrid Bonding using Inter-Die Gap Fill Dielectrics for 2. Integration	302
Kurita (Institute of Science Tokyo, Japan) Hierarchical Multi-Layer and Stacking Vias with Novel Structure by Transferrable Cu/Polymer Hybrid Bonding For High Speed Digital Applications	313

B.S.S. Chandra Rao (Institute of Microelectronics, Agency for Science, Technology and Research, Republic of Singapore), Patrick Lim Yin Wei (Applied Materials Singapore Technology Pte. Ltd, Republic of Singapore), Arvind Sundaram (Institute of Microelectronics, Agency for Science, Technology and Research, Republic of Singapore), Santosh Kumar Rath (Applied Materials Singapore Technology Pte. Ltd, Republic of Singapore), Mishra Dileep Kumar (Institute of Microelectronics, Agency for Science, Technology and Research, Republic of Singapore), Cheemalamarri Hemanth Kumar (Institute of Microelectronics, Agency for Science, Technology and Research, Republic of Singapore), Ratan Bhimrao Umralkar (Institute of Microelectronics, Agency for Science, Technology and Research, Republic of Singapore), Vasarla Nagendra Sekhar (Institute of Microelectronics, Agency for Science, Technology and Research, Republic of Singapore), Vasarla Nagendra Sekhar (Institute of Microelectronics, Agency for Science, Technology and Research, Republic of Singapore), Ye Yong Liang (Institute of Microelectronics, Agency for Science, Technology and Research, Republic of Singapore), Hipona Randy Tupaen (Institute of Microelectronics, Agency for Science, Technology and Research, Republic of Singapore), Gilbert See (Applied Materials Singapore Technology Pte. Ltd, Republic of Singapore), and Vempati Srinivasa Rao (Institute of Microelectronics, Agency for Science, Technology and Research, Republic of Singapore)	318
πεσειτείτ, περίουτε ο Βιτιχαροίτε)	
Session 9: Co-Packaged Optics and Hybrid Bonding Innovations for	HI
Demonstration of Co-Packaged Optics Assembly for Fiber-Based Optical Interconnect	324
Optical Multi-Chip Interconnect Bridge (OMIB TM) Interposer Assembly Process to Enable High-Density Photonic Interconnects for High-Performance Computing Applications	331
Advanced Glass Substrate Fabrication and Metallization Process Technology for Co-Packaged Optics Seong-Ho Seok (Corning Technology Center, Korea), Bo-Kyung Kong (Corning Technology Center, Korea), Lars Brusberg (Corning Research and Development Corporation, USA), Lucas W. Yeary (Corning Research and Development Corporation, USA), Jung-Hyun Noh (Corning Technology Center, Korea), Han-Kyom Lee (Corning Technology Center, Korea), Kyeong-Gon Choi (Corning Technology Center, Korea), and Daniel W Levesque (Corning Research and Development Corporation, USA)	337

Self-formed Barrier using Cu-Mn Alloy Seed applied to a 400nm Pitch Wafer-to-Wafer Hybrid
Bonding Technology
Stefaan Van Huylenbroeck (imec, Belgium), Soon Aik Chew (imec,
Belgium), Boyao Zhang (imec, Belgium), Emmanuel Chery (imec, Belgium),
Joke De Messemaeker (imec, Belgium), Prafulla Gupta (imec, Belgium),
Nicolas Jourdan (imec, Belgium), Sven Dewilde (imec, Belgium), Zaid
El-Mekki (imec, Belgium), Joeri De Vos (imec, Belgium), Gerald Beyer
(imec, Belgium), and Eric Beyne (imec, Belgium)
SiCN CMP Integration for Hybrid Bonding Application
Inter-Die Hybrid Cu/Diamond Microbump Bonding for 3D Heterogenous Integration
First Demonstration of Superior Characteristics of Co-Co Bonding with Passivation Structure at Low Thermal Budget for Advanced Packaging and Ultra-Fine Pitch Applications357 Li Hsin Cheng (National Yang Ming Chiao Tung University, Taiwan), Chiao-Yen Wang (National Yang Ming Chiao Tung University, Taiwan), Kai-Fang Lai (National Yang Ming Chiao Tung University, Taiwan),
Mu-Ping Hsu (National Yang Ming Chiao Tung University, Taiwan), and Kuan-Neng Chen (National Yang Ming Chiao Tung University, Taiwan)
Session 10: High Reliability Applications
Automotive Application-driven Vibration Test Approach: Bridging the Gap Between Module and Board Level Reliability Test Methods
Chip Package Interaction Challenges and Solutions for FOWLP Product Reliability for Automotive Applications
Gaurav Sharma (NXP Semiconductor, USA), Amar Mavinkurve (NXP
Semiconductor, The Netherlands), Michiel van Soestbergen (NXP
Semiconductor, The Netherlands), Greta Terzariol (NXP Semiconductor,
The Netherlands), Taki Fang (NXP Semiconductor, Taiwan), and Nishant
Lakhera (NXP Semiconductor, USA)

Higher Reliability Cu Pillar Bump on ENEPIG Substrate with Suppressed Ni3P for Automotive Applications
Reliability and Microstructure Characterization of Through-Silicon Vias (TSV) at Different Aspect Ratios using EBSD-Raman Spectroscopy
Cryogenic and Wide Temperature Thermal Cycling Reliability Study of QFN and CQFJ Packages for Lunar Missions
The Role of Polymer Shrinkage and Oxidation in Thermal Aging Induced Crack Formation in Glass Fiber Reinforced Printed Circuit Boards
Enhanced AEC Qualification of 5nm AI Processor with Liquid Cooling for Level 4 Autonomous Driving
Session 11: Emerging Trends: Towards High Speed, Secure, Reliable, and Sustainable Packaging
Lumped Element Multiplexer Design and Calibration in Cryogenic Environment for Quantum Reflectometry Applications
Embedded Silicon Chip Capacitors in Glass Package for Vertical Power Delivery
SiPMeter: Active Hardware Metering for System-in-Package in Heterogeneous Integration

Thermoset Packaging Materials Polette Centellas (National Intitute of Standards and Technology, USA), Stian Romberg (National Intitute of Standards and Technology, USA), Ran Tao (National Intitute of Standards and Technology, USA), Alexander K. Landauer (National Intitute of Standards and Technology, USA), Karl F. Schoch (Northrop Grumman, USA), Huong Giang Nguyen (National Intitute of Standards and Technology, USA), Gale Holmes (National Intitute of Standards and Technology, USA), Gery Stafford (National Intitute of Standards and Technology, USA), and Christopher Soles (National Intitute of Standards and Technology, USA)	. 432
Predictive Modeling of IMC Growth in BGA Component Solder Joints using Artificial Neural Networks Under Rework and Temperature Cycling Conditions Adlil Aizat Ismail (SanDisk Corporation, Malaysia), Maria Abu Bakar (Universiti Kebangsaan Malaysia, Malaysia), Azman Jalar (Universiti Kebangsaan Malaysia, Malaysia), Mohd Ridzwan Yaakub (Universiti Kebangsaan Malaysia, Malaysia), Muhammad Iqbal Abu Latiffi (Universiti Kebangsaan Malaysia, Malaysia), Erwan Basiron (SanDisk Corporation, Malaysia), and Muhammad Nizam Ilias (SanDisk Corporation, Malaysia)	. 440
Parameter Degradation Monitoring and Controller Adaptation using Digital Twin	448
Bio-Sourced Unfilled Epoxy for Die-Attach Applications	. 453
Session 12: Advanced Thermal Management Modeling	
Session 12: Advanced Thermal Management Modeling Development of an Embedded 2-Phase Cooling Solution for Two Stacked High-Power Chips in Future HPC & AI Applications	. 460

Enhanced Thermal Management of a 1.2 kV SiC MOSFET Half-Bridge Fan-Out Panel-Level	
Packaging with Nanocopper Sintering Die-Attachment	473
Wei Chen (Fudan University, China), Junwei Chen (Fudan University,	
China), Chao Gu (Fudan University, China), Tiancheng Tian (Fudan	
University, China), Xuejun Fan (Lamar University, USA), Guoqi Zhang	
(Delft University of Technology, the Netherlands), and Jiajie Fan	
(Fudan University, China; Research Institute of Fudan University in	
Ningbo, China)	
Integrated Package-to-System Thermal Solution Evolution for High-Performance 2.5D CoWoS-R Advanced Packaging Technology Development	481
Tsun-Yen Wu (Taiwan Semiconductor Manufacturing Company, Taiwan	
(R.O.C.)), Kuo-Chin Chang (Taiwan Semiconductor Manufacturing Company,	
Taiwan (R.O.C.)), Chien-Chang Wang (Taiwan Semiconductor Manufacturing	
Company, Taiwan (R.O.C.)), Bang-Li Wu (Taiwan Semiconductor	
Manufacturing Company, Taiwan (R.O.C.)), Ching Wang (Taiwan	
Semiconductor Manufacturing Company, Taiwan (R.O.C.)), Kathy Yan	
(Taiwan Semiconductor Manufacturing Company, Taiwan (R.O.C.)),	
Chien-Hsun Lee (Taiwan Semiconductor Manufacturing Company, Taiwan	
(R.O.C.)), Cheng-Chi Hsieh (Taiwan Semiconductor Manufacturing	
Company, Taiwan (R.O.C.)), Jing-Ruei Lu (Taiwan Semiconductor	
Manufacturing Company, Taiwan (R.O.C.)), Ruei-Wun Song (Taiwan	
Semiconductor Manufacturing Company, Taiwan (R.O.C.)), Sing-Da Jiang	
(Taiwan Semiconductor Manufacturing Company, Taiwan (R.O.C.)), and Jun	
He (Taiwan Semiconductor Manufacturing Company, Taiwan (R.O.C.))	
Thermal Management of Heterogeneously Integrated HBM-GPU Module with Step Height Difference	487
Euichul Chung (Georgia Institute of Technology, USA), Madison Manley	
(Georgia Institute of Technology, USA), Wanshu Zeng (Georgia Institute	
of Technology, USA), and Muhannad S. Bakir (Georgia Institute of	
Technology, USA)	
	402
Rapid AI-driven Power-Thermal Intelligent DVFS for HPC Applications	493
Zhi Yang (Groq Inc, USA), Yong Pei (Groq Inc, USA), Mohamed Eldafrawy	
(Groq Inc, USA), Santosh Raghavan (Groq Inc, USA), Liming Gong (Groq	
Inc, USA), Igor Arsovski (Groq Inc, USA), Richard Ozaki (Siemens	
Digital Industry Software, USA), Jimmy He (Siemens Digital Industry	
Software, USA), and Vivian Zheng (VisualizationSolution, USA)	
First Demonstration of Metal-Lidded Integral Microjet Impingement On-Chip Cooling	
Structures with Alternating Feeding and Draining Nozzles for High-Performance Interposer	
Packages	499
Gopinath Sahu (Purdue University, USA), Duc Hoang (Purdue University,	
USA), Ruoyi Li (Purdue University, USA), Akshat Hetal Patel (Purdue	
University, USA), Ketan Yogi (Purdue University, USA), and Tiwei Wei	
(Purdue University, USA)	
(- mini- control or graph of the control of the con	

Session 13: Large Panel FO for High Density Integration

Carrier Warpage Improvement using Non-Photosensitive Dielectric Material for High I/O Density Organic RDL Application in Future Advanced Packaging	505
Next Generation Panel Level RDL Interposer Package for High Density Interconnection	510
M-Series Fan-Out Interposer Technology (MFIT) – Scaling up for HPC & AI Craig Bishop (Deca Technologies, USA), Jan Kellar (Deca Technologies, USA), Andrew Hoetker (Deca Technologies, USA), Ryan Sanden (Deca Technologies, USA), Martin Laliberte (IBM Canada, Canada), Diego Anzola (IBM Research, USA), and Arvind Kumar (IBM Research, USA)	515
Enhancement of the Adhesion in Multilayered Redistribution Layers of Fan-Out Wafer Level Packages for Memory Application	522
Die-to-Die Parallel Interface Optimization Utilizing Deca's Novel M-Series Gen-2 Fan-Out Technology	526
SiO_2-Based Chiplet Reconstitution Technology for Multi-Height Chiplet Integration	531
Advanced Packaging from FOWLP to FOPLP Development of Fanout Chip Last in 300mm Panel . 5 Teck Chong Lee (Advanced Semiconductor Engineering, Inc., Taiwan), Yungshun Chang (Advanced Semiconductor Engineering, Inc., Taiwan), Chih-Pin Hung (Advanced Semiconductor Engineering, Inc., Taiwan), Lihong Cao (Advanced Semiconductor Engineering, Inc., USA), Owen Yang (Advanced Semiconductor Engineering, Inc., Taiwan), Simon YL Huang (Advanced Semiconductor Engineering, Inc., Taiwan), and Yihsien Wu (Advanced Semiconductor Engineering, Inc., Taiwan)	537

Session 14: New Materials and Processes in Wafer-to-Wafer Hybrid Bonding

Integration, Materials and Equipment Innovations to Enable 100 nm Pitch W2W Bonding for Memory-to-Logic and Logic-to-Logic 3D Stacking	. 542
Advanced Memory Wafer-to-Wafer Bonding with Support of Recyclable Carrier Systems	547
Development of Wafer-Level Wet Atomic Layer Etching Process Platform for Cu Surface Topography Control in Hybrid Bonding Applications	. 554
Development of a Novel WoWoW Process for 1/1.3-Inch 50 Megapixel Three-Wafer-Stacked CMO Image Sensor with DNN Circuits	
Wafer-to-Wafer Hybrid Bonding Technology with 300nm Interconnect Pitch Stefaan Van Huylenbroeck (imec, Belgium), Soon Aik Chew (imec, Belgium), Boyao Zhang (imec, Belgium), Lieve Bogaerts (imec, Belgium), Cindy Heyvaert (imec, Belgium), Sven Dewilde (imec, Belgium), Serena Iacovo (imec, Belgium), Michele Stucchi (imec, Belgium), Joeri De Vos (imec, Belgium), Gerald Beyer (imec, Belgium), and Eric Beyne (imec, Belgium)	. 565

Sari Al Zerey (Binghamton University (State University of New York), USA), Alina Bennett (Binghamton University (State University of New York), USA), Morlidhar Patel (Binghamton University (State University of New York), USA), Junghyun Cho (Binghamton University (State University of New York), USA), Roy Yu (IBM Research, USA), Nicholas Polomoff (IBM Research, USA), Luke Darling (IBM Research, USA), and Katsuyuki Sakuma (IBM Research, USA)	570
Novel Selective Metal Capping on Cu pad Enabling Void-Free Hybrid Bonding at Low Thermal Budgets, Irrespective of Cu Topography and Microstructure	
Session 15: Photonics Integration and Subsystems Functional Demonstrator of a 256 Channels Beam Steering Device of a LIDAR for Autonomous Driving Including Silicon Photonics, 3D and Advanced Packaging Features: TSV and Fine	
Driving including silicon rhotonics, 3D and Advanced rackaging reatures : 13v and rine	
Pitch Flip Chip Thierry Mourier (CEA-Leti, Univ. Grenoble Alpes, France), Nadia Miloud-Ali Berchet (CEA-Leti, Univ. Grenoble Alpes, France), Laura Boutafa (CEA-Leti, Univ. Grenoble Alpes, France), Selimen Benahmed (CEA-Leti, Univ. Grenoble Alpes, France), Yacoub Sahouane (CEA-Leti, Univ. Grenoble Alpes, France), Vincent Moulin (CEA-Leti, Univ. Grenoble Alpes, France), Damien Saint Patrice (CEA-Leti, Univ. Grenoble Alpes, France), Edouard Deschaseaux (CEA-Leti, Univ. Grenoble Alpes, France), Daivid Fowler (CEA-Leti, Univ. Grenoble Alpes, France), Sylvain Guerber (CEA-Leti, Univ. Grenoble Alpes, France), Alain Gueugnot (CEA-Leti, Univ. Grenoble Alpes, France) Faugier-Tovar (CEA-Leti, Univ. Grenoble Alpes, France)	582
Pitch Flip Chip Thierry Mourier (CEA-Leti, Univ. Grenoble Alpes, France), Nadia Miloud-Ali Berchet (CEA-Leti, Univ. Grenoble Alpes, France), Laura Boutafa (CEA-Leti, Univ. Grenoble Alpes, France), Selimen Benahmed (CEA-Leti, Univ. Grenoble Alpes, France), Yacoub Sahouane (CEA-Leti, Univ. Grenoble Alpes, France), Vincent Moulin (CEA-Leti, Univ. Grenoble Alpes, France), Damien Saint Patrice (CEA-Leti, Univ. Grenoble Alpes, France), Edouard Deschaseaux (CEA-Leti, Univ. Grenoble Alpes, France), Daivid Fowler (CEA-Leti, Univ. Grenoble Alpes, France), Sylvain Guerber (CEA-Leti, Univ. Grenoble Alpes, France), Alain Gueugnot (CEA-Leti, Univ. Grenoble Alpes, France),	I/ML

Development of Transfer-Printed III-V C-Band Lasers on Silicon Photonic Integrated Circuits for Multi-Project Wafer Offering	0
Low-Cost Transceiver Integration for Next Generation Passive Optical Network	5
Stress, Thermal and Optical Performance (STOP) Analysis of Co-Packaged Optical Processor with FPGA-Memory-Optics-Power Integration	0
Direct Flip-Chip on Board (FCOB) Assembly for Optical Transceivers	5
Session 16: Manufacturing and Thermal Management Reliability	
Influence of Sn-Bi Solder Joint Microstructure on the Electrical and Joule Heat Properties of the Joint	0
A Study on the Improvement of Solder Joint Reliability of Module Products by IPL Soldering Method	5

Improving the Quality and Yield Performance of Vacuum Fluxless Reflow Soldering for High-Density AI Chips
Additive Low-Temperature Assembly on Sustainable Substrates Circuit Reliability Performance and Stability Interactions
Investigation on Joule Heating of Plated Through Hole (PTH) Via
Thermo-Mechanical Stability of High-Performance Chip Integration: Structure-Induced Stress in Complex System Structures
Enhanced Electromigration Reliability of Cu/SiO2 Hybrid Joints Fabricated by (111)-Oriented Nanotwinned Cu
Session 17: Signal Integrity / Power Integrity for Advanced Packaging Technologies
Simulation and Optimization of 32 Gbps On-Interposer Interconnects with Novel Deep Trench Passive Equalizer

Mixed-Mode Distributed Physical Based Transmission Line Model of 5G Connectors for Fast Signal Integrity Analysis on Ground Resonances and 112 Gbps PAM4	. 664
Signal Integrity Analysis of Differential Through-Silicon Via (TSV) with Silicon Dioxide Well (SDW) for Impedance Compensation in the Serdes Interface	. 672
Software-defined Power Integrity (PI) Analysis for 2.5D/3D Packages	. 676
Power Integrity Design of a 56Gb/s Si-Photonic Optical Link for Memory Applications	681
Signal Integrity Design of a High-Performance, High-Frequency (10MHz to 11GHz), 3dB Bandwidth High-Speed ADC Driver Amplifier	687
Compact Tri-Band Stub Filter using Advanced Bridged-CRLH Transmission Line for 5G Applications Junhyuk Yang (University of Florida, USA), Hanna Jang (University of Florida, USA), Alexander Wilcher (University of Florida, USA), and Yong-Kyu Yoon (University of Florida, USA)	. 695

Session 18: Simulations and Validation on Reliability Challenges of High Performance Packages

Simulation and Experimental Validation of Microstructure Evolution of Sintered Ag Layer During Thermal Aging using a Hybrid Potts-Phase Field Model	199
Enabling Comprehensive Study of Electromigration and Diffusion Induced Failure Mechanisms in Lead-Free Solder Joint by Frame of Phase Field Modeling	'05
In-Situ Confocal Raman Spectroscopy Assisted Interfacial Residual Stress Characterization in SiC Chip Sintered on AMB Substrate with Nanocopper Paste	'11
Additively Manufactured In-Mold Electronics Reliability Under Thermal Cycling and Sustained High Temperature	'18
Thermal-Mechanical Modeling of Package Reflow for Cooling of Future CPU and GPU Devices7 Ercan M. Dede (Toyota Research Institute of North America, USA), Paul Paret (National Renewable Energy Laboratory, USA), Suhas Rao Tamvada (University of Florida, USA), Gilberto Moreno (National Renewable Energy Laboratory, USA), Patrick McCluskey (University of Maryland, USA), Shailesh N. Joshi (Toyota Research Institute of North America, USA), Sreekant Narumanchi (National Renewable Energy Laboratory, USA), and Saeed Moghaddam (University of Florida, USA)	'26
Development and Optimization of a Flexible Printed Coplanar Capacitive Sensor for Accurate Twisting Motion Detection	732

Isothermal Shock Testing on Flip-Chip Interconnects	7
Session 19: Chiplet Integration and Advanced Thermal Solutions	
Direct-to-Silicon Liquid Cooling Integrated on CoWoS® Platform Yu-Jen Lien (Taiwan Semiconductor Manufacturing Company, Ltd., R.O.C.), Sing-Da Jiang (Taiwan Semiconductor Manufacturing Company, Ltd., R.O.C.), Cheng-Chieh Hsieh (Taiwan Semiconductor Manufacturing Company, Ltd., R.O.C.), Han-Jong Chia (Taiwan Semiconductor Manufacturing Company, Ltd., R.O.C.), Tsunyen Wu (Taiwan Semiconductor Manufacturing Company, Ltd., R.O.C.), Chien-Chih Lin (Taiwan Semiconductor Manufacturing Company, Ltd., R.O.C.), Ke-Han Shen (Taiwan Semiconductor Manufacturing Company, Ltd., R.O.C.), Szu-Wei Lu (Taiwan Semiconductor Manufacturing Company, Ltd., R.O.C.), Kathy Yan (Taiwan Semiconductor Manufacturing Company, Ltd., R.O.C.), Kuo-Chung Yee (Taiwan Semiconductor Manufacturing Company, Ltd., R.O.C.), and Douglas C.H. Yu (Taiwan Semiconductor Manufacturing Company, Ltd., R.O.C.)	3
A Novel Approach of Multi-Chip FOPKG Chiplet Interconnection using a Land-Side Si Bridge 748 Sungoh Ahn (Samsung Electronics Co, Ltd, Republic of Korea), Sangsub Song (Samsung Electronics Co, Ltd, Republic of Korea), Heeyoub Kang (Samsung Electronics Co, Ltd, Republic of Korea), Seokbeom Yong (Samsung Electronics Co, Ltd, Republic of Korea), Dongsuk Kim (Samsung Electronics Co, Ltd, Republic of Korea), Dae-Woo Kim (Samsung Electronics Co, Ltd, Republic of Korea), Sangkyu Lee (Samsung Electronics Co, Ltd, Republic of Korea), Jongyoun Kim (Samsung Electronics Co, Ltd, Republic of Korea), Junghoo Yun (Samsung Electronics Co, Ltd, Republic of Korea), and Eunyoung Lee (Samsung Electronics Co, Ltd, Republic of Korea)	3
Mid-BEOL Heterogeneous Integration Through Sub-1um Pitch Hybrid Bonding & Advanced Silicon Carrier Technologies for AI & Compute Applications	3
The Study and Challenges of Backside Metal Interface Material to Enhance Fan-Out Embedded Bridge Die Package (FO-EB) Thermal Performance	1

Thermal Impact of BSPDN for 3D Memory and Logic Integration Melina Lofrano (imec, Begium), Herman Oprins (imec, Begium), Geert Van der Plas (imec, Begium), and Eric Beyne (imec, Begium)	767
Inter-Die Gap-Filling with Varying Aspect Ratio using PECVD Oxide for 3D Packaging: Model Prediction and Experimental Validation	773
Modeling and Validation of an Integrated Package Solution (iPaS) for Next Generation Power Supply Systems Akitomo Takahashi (Murata Manufacturing Co., Ltd., Japan), Shuhei Yamada (Murata Manufacturing Co., Ltd., Japan), Yuuki Yabuhara (Murata Manufacturing Co., Ltd., Japan), Masafumi Tanaka (Murata Manufacturing Co., Ltd., Japan), Kazuki Itoyama (Murata Manufacturing Co., Ltd., Japan), Koshi Himeda (Murata Manufacturing Co., Ltd., Japan), and Atsushi Yamamoto (Murata Manufacturing Co., Ltd., Japan)	780
Session 20: Novel Technologies for High Density RDL Interposers	
Pillar-Suspended Bridge (PSB); Transmission Simulation and Fabrication Process of 2-Micron Diameter / 5-Micron Pitch Dry Etched Stacked Via in Low-k Polymer for High Performance Redistribution Layer Bridge (RDL Bridge) Shinichi Arioka (AOI Electronics CO., LTD., Japan), Yusuke Naka (TAIYO INK MFG. CO., LTD., Japan), Koh Meiten (TAIYO INK MFG. CO., LTD., Japan), Fumito Ootake (ULVAC, Inc., Japan), Yasuhiro Morikawa (ULVAC, Inc., Japan), Tanapun Srichanthamit (AOI ELECTRONICS CO., LTD., Japan), Osamu Okada (Institute of Science Tokyo, Japan), and Yoichiro Kurita (Institute of Science Tokyo, Japan)	785
Panel Level Interposer by using Glass Carrier for 2.5D Advance IC Package Application	793
Fine Pitch Semi-Additive RDL-Process Development Nelson Pinho (Imec, Belgium), Lili Wang (Imec, Belgium), Murat Pak (Imec, Belgium), Amaia Zerio (Imec, Belgium), Jeonho Kim (Imec, Belgium), Punith Gowda (Imec, Belgium), Naveen Reddy (Imec, Belgium), Andy Miller (Imec, Belgium), and Eric Beyne (Imec, Belgium)	798

Wafer Backside Fine Pitch Copper Interconnects and Low-Profile Micro-Bumps Pad Process for Multiple Chip-on-Wafer Stacking Structure
Demonstration of a Hybrid Wiring Layer Assembly for Low-Cost sub-10µm Pitch Integration 812 Vineeth Harish (UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS), USA), Seungwoo Baek (UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS), USA), Kai Zheng (Applied Materials, USA), Krutikesh Sahoo (UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS), USA), Gilbert Park (Applied Materials, USA), Han-Wen Chen (Applied Materials, USA), Steven Verhaverbeke (Applied Materials, USA), and Subramanian S. Iyer (UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS), USA)
A Novel Architecture for On-Device AI in Mobile Application with Enhanced Heat Dissipation 819 Kyung Don Mun (Samsung Electronics Co., Ltd, South Korea), Jihwang Kim (Samsung Electronics Co., Ltd, South Korea), Sangjin Baek (Samsung Electronics Co., Ltd, South Korea), Jaechoon Kim (Samsung Electronics Co., Ltd, South Korea), Suk Won Jang (Samsung Electronics Co., Ltd, South Korea), Kang Joon Lee (Samsung Electronics Co., Ltd, South Korea), DongWoon Park (Samsung Electronics Co., Ltd, South Korea), and Dae-Woo Kim (Samsung Electronics Co., Ltd, South Korea)
High-Density RDL Fan-Out With L/S 2/2µm Dry Etched Micro Vias for Agile Prototyping/Low Volume Production and TAT/NRE Cost Modeling
Session 21: Meeting AI Challenges : Large Package Solution and Warpage Management for Advanced Packaging
Containment Solution for Liquid Metal-Based Second-Level Interconnect Technology

Ultra High Aspect Ratio Photo Resist for Cu Pillar Based Multi-Stack Fan-out Package with	024
Wide I/O LPDDR	. 836
Seon Ho Lee (Samsung Electronics Co., Ltd., Republic of Korea),	
Jinyoung Kim (Samsung Electronics Co., Ltd., Republic of Korea), Jeongseok Mun (Samsung Electronics Co., Ltd., Republic of Korea),	
Okseon Yoon (Samsung Electronics Co., Ltd., Republic of Korea),	
Jeongju Park (Samsung Electronics Co., Ltd., Republic of Korea),	
JunHyeong Park (Samsung Electronics Co., Ltd., Republic of Korea), and	
Jihye Shim (Samsung Electronics Co., Ltd., Republic of Korea)	
Advanced Fan-Out Panel Level Packaging via Digital Lithography Patterning Development for	
AI Devices	. 841
Ksenija Varga (EV Group, St. Florian am Inn, Austria), Roman Holly (EV	. 011
Group, St. Florian am Inn, Austria), Tobias Zenger (EV Group, St.	
Florian am Inn, Austria), Matthias Brunnbauer (EV Group, St. Florian	
am Inn, Austria), Boris Považay (EV Group, St. Florian am Inn,	
Austria), Thomas Uhrmann (EV Group, St. Florian am Inn, Austria),	
Dimitri Janssen (FUJIFILM Electronic Materials, Belgium), and Stefan	
Vanclooster (FUJIFILM Electronic Materials, Belgium)	
Effective Build-Up Substrate Design for Warpage Reduction and Reliability Enhancement in	
Advanced Semiconductor Packages	847
Daichi Okazaki (Ajinomoto Fine-Techno Co., Inc., JAPAN), Eiji Baba	
(Ajinomoto Fine-Techno Co., Inc., JAPAN), Yuto Inoue (Ajinomoto	
Fine-Techno Co., Inc., JAPAN), Daisuke Hironiwa (Ajinomoto Fine-Techno	
Co., Inc., JAPAN), Ikumi Sawa (Ajinomoto Fine-Techno Co., Inc.,	
JAPAN), YoungGun Han (Fukuoka University, JAPAN), Taka Kanayama	
(Fukuoka University, JAPAN), Atsunori Hattori (3D semiconductor	
research center, JAPAN), Kanta Nogita (3D semiconductor research	
center, JAPAN), and Ryo Miyamoto (Ajinomoto Fine-Techno Co., Inc.,	
JAPAN)	
Development of Negative Thermal Expansion Zeolite Fillers for Next-Generation Low CTE	
Encapsulation Materials	. 852
Ryo Nishida (Mitsubishi Chemical Corporation, Japan), Yutaro Tanaka	
(Mitsubishi Chemical Corporation, Japan), Shu Hikima (Mitsubishi	
Chemical Corporation, Japan), Ryohji Ohnishi (Mitsubishi Chemical	
Corporation, Japan), Kazuki Tsujikawa (Mitsubishi Chemical	
Corporation, Japan), Tetsuharu Yuge (Mitsubishi Chemical Corporation,	
Japan), and Masahiro Yokoyama (Mitsubishi Chemical Corporation, Japan)	
Development of Novel Photosensitive Polyimide with 170 °C Curing Process to Enable Low	
Warpage and Sub-2 µm Patterning for RDLs in Next Generation Interposer	. 857
Yusuke Murata (JSR Corporation, Japan), Shuhei Horikawa (JSR	
Corporation, Japan), Mitsuka Inoue (JSR Corporation, Japan), Ryoji	
Tatara (JSR Corporation, Japan), and Hirokazu Ito (JSR Corporation,	
Japan)	

Innovative Silicon Die Thinning and Edge Protection of Chip-to-Wafer Hybrid Bonded Wafer for High-Density Multi-Chip Stacking
Session 22: Heterogenous Integration Using Bridge and 3D Stacking
Hybrid Bonding with Fluidic Self Alignment: Process Optimization and Electrical Test Vehicle Fabrication
Optimization of Alignment Model and Metrology During Backside EUV Lithography Patterning for CFET Technology
Assessing Queue Time in D2W Hybrid Bonding Through Precise Bond Strength Measurements 878 Yuki Yoshihara (YOKOHAMA National University), Junya Fuse (Yokohama National University), Shimpei Aoki (Toray Engineering Co.,Ltd.), Takashi Hare (Toray Engineering Co.,Ltd.), Kentaro Mihara (Toray Engineering Co.,Ltd.), Takayuki Miyoshi (Toray Engineering Co.,Ltd.), Naoko Yamamoto (DISCO Corporation), Shunsuke Teranishi (DISCO Corporation), Takafumi Fukushima (Tohoku University), Akira Uedono (University of Tsukuba), and Fumihiro Inoue (Yokohama National University)

Thin 3D: An Innovative Approach to Ultra-Thin Wafer-Level Active Device Transfer Technology with Optimized Material and Thermal Solution for 3D IC Ting-Yu Chen (National Yang Ming Chiao Tung University, Taiwan), Shie-Ping Chang (National Yang Ming Chiao Tung University, Taiwan), Bo-Jheng Shih (National Yang Ming Chiao Tung University, Taiwan), Zih-Yang Chen (National Yang Ming Chiao Tung University, Taiwan), Yu-Lun Liu (National Yang Ming Chiao Tung University, Taiwan), Po-Jung Sung (Taiwan Semiconductor Research Institute, Taiwan), Nien-Chih Lin (Taiwan Semiconductor Research Institute, Taiwan), Chih-Chao Yang (Taiwan Semiconductor Research Institute, Taiwan), Po-Tsang Huang (National Yang Ming Chiao Tung University, Taiwan), Ming-Yang Li (Taiwan Semiconductor Manufacturing Company, Taiwa), Iuliana P. Radu (Taiwan Semiconductor Manufacturing Company, Taiwa), and Kuan-Neng Chen (National Yang Ming Chiao Tung University, Taiwan)	385
Ultra-Thin Wafer Handling Process for Advanced Packaging using Novel Temporary Bonding Film and De-Bonding Method	890
A Novel Thermal Isolation Method with Embedded 'Glass Bridge' Structures in Silicon-Based 2.5D Heterogeneous Integration Systems	395
Technology Enhancements on FOCoS-Bridge for Emerging Trends in High-Performance Computing (HPC) and Artificial Intelligence (AI)	_
Session 23: AI Enabled Innovations in Advanced Packaging Technologies	
AI-Based Decision-Tree Concept to Fabricate Active Waferscale Fabric for Heterogeneous Chiplet Integration	906

AI Trustworthiness in the Era of Advanced Packaging: Challenges and Opportunities	.912
Efficient Visual Inspection Framework of High-Bandwidth Memory Bumps with Generative and Deep Learning AI Richard Chang (Institute for Infocomm Research (I2R), A*STAR, Singapore), Jie Wang (Institute for Infocomm Research (I2R), A*STAR, Singapore), Ser Choong Chong (Institute for Microelectronics (IME), A*STAR, Singapore), Xulei Yang (Institute for Infocomm Research (I2R),	. 920
A*STAR, Singapore), and Ramanpreet Singh Pahwa (Institute for Infocomm Research (I2R), A*STAR, Singapore) Generative Model Based Multi-Layer PDN Impedance Estimation with Multi-Power Domain	. 927
Hyunjun An (Korea Advanced Institute of Science and Technology (KAIST), Republic of Korea), Haeseok Suh (Korea Advanced Institute of Science and Technology (KAIST), Republic of Korea), Keeyoung Son (Korea Advanced Institute of Science and Technology (KAIST), Republic of Korea), Haeyeon Kim (Korea Advanced Institute of Science and Technology (KAIST), Republic of Korea), Keunwoo Kim (Korea Advanced Institute of Science and Technology (KAIST), Republic of Korea), Junghyun Lee (Korea Advanced Institute of Science and Technology (KAIST), Republic of Korea), Taein Shin (Korea Advanced Institute of Science and Technology (KAIST), Republic of Korea), Seonguk Choi (Korea Advanced Institute of Science and Technology (KAIST), Republic of Korea), Taesoo Kim (Korea Advanced Institute of Science and Technology (KAIST), Republic of Korea), Junho Park (Korea Advanced Institute of Science and Technology (KAIST), Republic of Korea), Inyoung Choi (Korea Advanced Institute of Science and Technology (KAIST), Republic of Korea), and Joungho Kim (Korea Advanced Institute of Science and Technology (KAIST), Republic of Korea)	
RAICEx: A Rapid and Accurate AI-Based Framework for Crosstalk Prediction in IC Packages with a Case Study on High-Speed DDR Systems	. 933
TDR Optimization Method of 112G Serdes Interface in PKG Using Deep Reinforment Learing Hyunwoong Kim (SAMSUNG Foundry, Republic of Korea (South)), Sungwook Moon (SAMSUNG Foundry, Republic of Korea (South)), Jiyoung Park (SAMSUNG Foundry, Republic of Korea (South)), Taeyun Kim (SAMSUNG Foundry, Republic of Korea (South)), Jinho Kim (SAMSUNG Foundry, Republic of Korea (South)), Haemin Lee (SAMSUNG Foundry, Republic of Korea (South)), and Seungki Nam (SAMSUNG Foundry, Republic of Korea (South))	941
AI-Assisted Electro-Thermal Co-Design for Hybrid Bonded Packages	. 947

Session 24: Advanced Characterization and Modeling of Next Generation Packaging Materials

Characterization of Moisture Diffusion Properties of ABF and Mold Compounds in Molded Package with High Copper Density Substrate	. 953
Thermal-Mechanical Behavior of Highly (111)-Oriented Nano Twinned Electroplated Copper for Advanced Electronic Packaging	. 958
Nanoindentation Based Methodology to Characterize the Adhesion Strength of Dielectric Bond Interfaces Kris Vanstreels (imec, Belgium), Oguzhan Orkut Okudur (imec, Belgium), Yusuf Burak Ozdemir (imec, Belgium), Mario Gonzalez (imec, Belgium), and Eric Beyne (imec, Belgium)	. 965
Non-PFAS Semiconductor Packaging Material Performance and Stability in Comparison with PFAS Materials	. 972
Predictive Modeling of Thin Films Properties Using an Experimental and Simulation-Based Approach	. 980
Physics-Based Modeling with Nanoindentation on the Mechanical Reliability of TGV Substrates Under Annealing Effects Jui-Chang Chuang (EOSL, R.O.C.), Chang-Chun Lee (National Tsing Hua University, R.O.C.), Wei-Cheng Tsai (EOSL, R.O.C.), Hao-Zhou Lin (EOSL, R.O.C.), Chen-Tsai Yang (EOSL, R.O.C.), Chung-I Li (EOSL, R.O.C.), Shih-Hsien Lee (Semiconductor Advanced Packaging, R.O.C.), and Shih-Hao Kuo (Semiconductor Advanced Packaging, R.O.C.)	985

Validated Methodology for Accurate Simultaneous Measurement of Elastic Modulus and CTE of BEOL Materials for Improved Advanced Package Performance Prediction
Session 25: Advanced Substrate Technologies- Organic, Embedding and Glass
Development of Glass Core Substrates for Long-Term Reliability Under Thermal Stress
Fully Encapsulated Fine Pitch Dual Damascene Organic RDL with Low Dk Df Photosensitive Polyimide and Its Reliability
A Comparative Study on Power Delivery Network (PDN) using Several Capacitor-Embedded Substrates for Next Generation Power Supply Applications
Embedded Vertical PDN (EV-PDN) Including Voltage Regulator (VR) for Over-1kW FC-BGA Based on Over-1mm Thick-Core Organic Substrate
Glass Core Substrate versus Organic Core Substrate

Development of Glass Core Build-Up Substate with TGV
High-Aspect-Ratio, 6-µm-Diameter Through-Glass-Via Fabrication into 100-µm-Thick ENA1 by Dry Laser Micro-Drilling Process
Session 26: Process Innovation in Through-Via and Solder Interconnections
Deep Via and Trench Etching of Low CTE Glass Package Substrate using SF6, NF3 and H2O Based NLD Plasma Process
Development of Straight, Small-Diameter, High-Aspect Ratio Copper-Filled Through-Glass Vias (TGV) for High-Density 3D Interconnections
Metallization of Helium-Hermetic and Thermo-Mechanically Reliable Through Glass Vias (TGV) by Conformal Pinched Via (CPV) Approach
A Novel Approach to Ultra-Low Temperature Interconnection: Double-Sided SLID Process using SAC BGAs and Eutectic SnBiIn
Growth of Nanovoids in Electroless Cu Layer of Micro-Via After Thermal Reliability Test

Formic Acid Vapor Assisted Fluxless TCB for Advanced Packaging- a Key Enabler for Ultra-Fine Pitch and High-Density Interconnects	51
Enhancing Wafer-Level Cu-Solder Bonding: A Fluxless Approach with Cu-Selective Passivation Coating	59
Session 27: Thermal Management and Material Solutions for High Performance 2.5D and 3D Packaging	
Optimized TIM1 Solution for Large 2.5D HPC Packages using Silicone Matrix Containing Liquid Metal Materials	75
Novel Fabrication of Ultra-Long Al_2O_3 NWs and Their Integration into Al_2O_3 NWs and Their Hierarchically Structured Sheets-Epoxy Composites for Enhanced Thermal Management in Advanced Semiconductor Packaging	32
Characterization of PVD Backside Metal Adhesion for Improved Thermal Management in Heterogeneous Integration	39
Novel Low Df and Low CTE Material with High Thermal Stability for Organic Integration Board	94

Thermal Management of Nano-TSVs in Advanced BS-PDN: A Comparative Study of AlN and Oxide Dielectrics for Heat Dissipation Efficiency
Mold Underfill Process with Sheet Molding Compound for Full-Reticle Size Dies with Single-Digit Micrometer Gaps
Low Dk/Df Siloxane Hybrid Laminates for Advanced Packaging Substrate
Session 28: Reliability of Heterogeneous Integrated (HI) Packages
Session 28: Reliability of Heterogeneous Integrated (HI) Packages A Procedure for Evaluating the Chiplet-Module-System Interaction of a 2.5-D Package Under Board-Level Reliability Test Condition
A Procedure for Evaluating the Chiplet-Module-System Interaction of a 2.5-D Package Under Board-Level Reliability Test Condition

Influence of Cycling Induced Damage on the Anand Model Parameters of SAC305 Lead-Free Solder Golam Rakib Mazumder (Auburn University), Souvik Chakraborty (Auburn University), Mahbub Alam Maruf (Auburn University), Omma Sumaiya (Auburn University), Jeffrey C. Suhling (Auburn University), and Pradeep Lall (Auburn University)	1140
The Influence of Full IMC Structure on Micro-Bump EM Performance Chung-Yu Chiu (Taiwan Semiconductor Manufacturing Company, Ltd., R.O.C.), Jui-Shen Chang (Taiwan Semiconductor Manufacturing Company, Ltd., R.O.C.), Tzuan-Horng Liu (Taiwan Semiconductor Manufacturing Company, Ltd., R.O.C.), Chen-Nan Chiu (Taiwan Semiconductor Manufacturing Company, Ltd., R.O.C.), Yao-Chun Chuang (Taiwan Semiconductor Manufacturing Company, Ltd., R.O.C.), Ryan Lu (Taiwan Semiconductor Manufacturing Company, Ltd., R.O.C.), An-Jhih Su (Taiwan Semiconductor Manufacturing Company, Ltd., R.O.C.), John Yeh (Taiwan Semiconductor Manufacturing Company, Ltd., R.O.C.), and Jyun-Lin Wu (Taiwan Semiconductor Manufacturing Company, Ltd., R.O.C.)	1148
First Proof of 3D-IC Power Plane Defect Localization via Frequency Domain Spatial Heat Mapping Zhansen Shi (National University of Singapore, Singapore), Lucas Lum (National University of Singapore, Singapore), Bernice Zee (Advanced Micro Devices (Singapore) Pte Ltd, Singapore), Jiann Min Chin (Advanced Micro Devices (Singapore) Pte Ltd, Singapore), and Yeow Kheng Lim (National University of Singapore, Singapore)	1153
Advanced Thermal Management for High Power HPC, AI Nokibul Islam (STATS ChipPAC Inc, USA), Choong Kooi Chee (Marvell Technology Inc, USA), and JoonYoung Choi (STATS ChipPAC Inc, USA)	1160
Session 29: Advances in Additive Manufacturing, Wearable and Medical Technologies	
3D Printed Fanout Interposer Substrates with Curved Through-Holes for Rapid Prototyping of Advanced Packaging	1167

Fully Printed Pressure Sensor Array for Soft Robotics	173
Direct Digital Manufacturing for Laser-Drilled Vias in Multilayer Glass Printed Circuit Structures	181
Design and Fabrication of Bendable Double-Layer RDL Metallization Based on FOWLP for In-Mold Flexible Hybrid Electronics (iFHE)	187
FlexPower II: Flexible Interdigitated Battlet Li-ion Battery on FlexTrate^TM for Wearables	192
Design, Materials Selection, and Assembly Process for a CMUT-Based Handheld Ultrasound Probe Head: Overcoming Development Challenges	198
Session 30: Simulations on Advanced Package Processing - Hybrid Bonding, Chip Stacking and Wafer-to-Wafer	
Atomistic Modeling of Interfacial Cracking in Copper-to-Copper Direct Bonding	206

Crystal Plasticity-Based Modeling and Experimental Validation of the Influence of Microstructures and Grain Boundary Junction Types on the Cu-Cu Bonding Interface	1211
Lee (Sungkyunkwan University, Republic of Korea)	
Thermal Modeling of IR Laser Debond with Inorganic Thin Film Release Layers	1216
Tailoring Sintering Pressure to Optimize Nanoparticle Connectivity and Mechanical Strength in Cu-Based Interconnects	1223
Wafer Substrate Impact on Direct Wafer-to-Wafer Bonding Process Nathan Ip (Tokyo Electron America, Inc., USA), Yuhai Xiang (Tokyo Electron America, Inc., USA), Andrew Tuchman (TEL Technology Center, America, USA), Norifumi Kohama (Tokyo Electron Kyushu Ltd., Japan), Xuemei Chen (Tokyo Electron America, Inc., USA), Ilseok Son (TEL Technology Center, America, USA), and Kimio Motoda (Tokyo Electron Kyushu Ltd., Japan)	1230
Advanced Packaging Techniques: Hybrid Numerical and Experimental Analysis of Underfill Flow in Fine Pitch Multi-Chip Modules	1235

Simulation Analysis of Edge Dot-Void Formation and Edge Roll-Off Effects in Wafer-to-Wafer Bonding	242
Sunghwan Kim (Samsung Electronics, Republic of Korea), Youngsoo Kim (Samsung Electronics, Republic of Korea), Cheolmin Shin (Samsung Electronics, Republic of Korea), Geun-Myeong Kim (Samsung Electronics, Republic of Korea), Minyeong Je (Samsung Electronics, Republic of Korea), Seungchan Han (Samsung Electronics, Republic of Korea), Kyu-Ha Lee (Samsung Electronics, Republic of Korea), Hongkyun Lee (Samsung Electronics, Republic of Korea), Hanseong Shin (Samsung Electronics, Republic of Korea), Hyunyong Jeong (Samsung Electronics, Republic of Korea), Seongmin Son (Samsung Electronics, Republic of Korea), Hyunkyung Bae (Samsung Electronics, Republic of Korea), Soon-Wook Kim (Samsung Electronics, Republic of Korea), Dongchan Lim (Samsung Electronics, Republic of Korea), Hojin Lee (Samsung Electronics, Republic of Korea), Seungmin Lee (Samsung Electronics, Republic of Korea), Seungmin Lee (Samsung Electronics, Republic of Korea), Seung Hun Lee (Samsung Electronics, Republic of Korea), Kwangjin Moon (Samsung Electronics, Republic of Korea), and Dae Sin Kim (Samsung Electronics, Republic of Korea)	
Session 31: Automotive Power	
Development of a Low Temperature Sinterable Cu Paste Based on Micro Scale Flake	247
Novel Metal Based Thermal Interface Materials for Flip Chip Ball Grid Array Packages	255
Chiplet Package for Automotive and Edge Processors	259
Study of the Optimal Cu Core Size Based on Surface Evolver for Solder Bridge and HiP Free of Large PBGA Package	264

Localized Formation of Laser Non-conductive Film (NCF) on 10 µm Diameter Bumps, Applied to
20 μm Pitch Chiplet Chip-on-Wafer (CoW) Bonding
Jungho Shin (Superintelligence Creative Laboratory, ETRI, Korea), Jiho
Joo (Superintelligence Creative Laboratory, ETRI, Korea), Gwang-Mun
Choi (Superintelligence Creative Laboratory, ETRI, Korea), Chanmi Lee
(Superintelligence Creative Laboratory, ETRI, Korea), Ki-seok Jang
(Superintelligence Creative Laboratory, ETRI, Korea), Jin-hyuk Oh
(Superintelligence Creative Laboratory, ETRI, Korea), Ji-Eun Jung
(Superintelligence Creative Laboratory, ETRI, Korea), Ga-Eun Lee
(Superintelligence Creative Laboratory, ETRI, Korea), Seong-Cheol Kim
(Hanbat National Univeristy, Korea), Yong-Sung Eom (Superintelligence
Creative Laboratory, ETRI, Korea), and Kwang-Seong Choi
(Superintelligence Creative Laboratory, ETRI, Korea)
Mechanical and Electrical Evaluation of Materials for High Temperature Applications on Low
CTE AlN Ceramic Substrates
Mousa Al-Zanina (The State University of New York, USA), Erik Busse
(The State University of New York, USA), Riadh Al-Haidari (The State
University of New York, USA), Emuobosan Enakerakpo (The State
University of New York, USA), Stephen Gonya (The State University of
New York, USA), Anju Sharma (The State University of New York),
Mohammed Alhendi (The State University of New York, USA), Mark Poliks
(The State University of New York, USA), David Lin (GE Global
Research, USA), Cathleen Hoel (GE Global Research, USA), David
Shaddock (GE Global Research, USA), Linda Boyd (GE Global Research,
USA), and Sreya Paladugu (GE Global Research, USA)
Analysis and Optimization of Multi-Channel E-Mode AlGaN/GaN Trigate FinFET for Vertical
Power Delivery with Embedded Power Converters
Ayoub Sadeghi (University of Illinois Chicago, USA) and Inna
Partin-Vaisband (University of Illinois Chicago, USA)
Cassian 20 Dasian Matariala Matualaan & Chandauda fau Naut
Session 32: Design, Materials, Metrology & Standards for Next
Generation Interconnections
Dragges Development and Characteristics of Small Diameter (2 um) Cabalt Filled Through
Process Development and Characteristics of Small-Diameter (<3 µm), Cobalt-Filled Through Silicon Vias (TSVs) for High-Density 3D Chip Stacking
Silicon Vias (TSVs) for High-Density 3D Chip Stacking
USA), Thomas E. Beechem (Purdue University, USA), and Tiwei Wei
(Purdue University, USA)
Are Voids Restricted to Cu-Cu Bonding Interface? Truth Revealed by Conversion Electron
Yield-Scanning Transmission X-ray Microscopy
Murugesan Mariappan (Tohoku Univ., Japan), Shohei Yamashita (High
Energy Accelerator Research Organization (KEK), Japan), and Takafumi
Fukushima (Tohoku University, Japan)
I minorum (I one and one of months)

Ultra-Fast Cu/Polymer Hybrid Bonding with Electroless Passivation Layer for Cost-Effective	1000
Yu-Lun Liu (National Yang Ming Chiao Tung University, Taiwan), Tzu-Yu Chen (National Yang Ming Chiao Tung University, Taiwan), Kazuaki Ebisawa (Tokyo Ohka Kogyo Co., LTD, Japan), Makiko Irie (Tokyo Ohka Kogyo Co., LTD, Japan), Chun-Ta Li (National Yang Ming Chiao Tung University, Taiwan), Jia-Rui Lin (National Yang Ming Chiao Tung University, Taiwan), Yi-Hsuan Chen (National Yang Ming Chiao Tung University, Taiwan), Ya-Chien Chuang (Tokyo Ohka Kogyo Co., LTD, Japan), Hsiao-Wei Yeh (Tokyo Ohka Kogyo Co., LTD, Japan), Satoshi Fujimura (Tokyo Ohka Kogyo Co., LTD, Japan), and Kuan-Neng Chen (National Yang Ming Chiao Tung University, Taiwan)	1302
X64 UCIe Chiplet Interconnection at 32 GT/s on a Silicon Core Substrate	1308
Study of High-Density Optical Redistribution Layer Enabling Advanced Chiplet Edge Bandwidth Density on Active Optical Package Substrate	1313
A Study About Bonding Properties with Multilayer Porous Structures for Fine Pitch Interconnection	1318
Massive Orthogonal Stacking Assembly of IC (MOSAIC) Cube with Inductive Coupling for Exascale Memory Applications	1324

Session 33: Innovative Interconnects and Through Via Technology for 3D Packaging

Direct Bonding of Porous Cu Bumps Fabricated using Gas Treatment of Cu-Sn Bumps
Enabling 10 µm Die-to-Die Pad Pitch in Flexible Fan-Out with TrueAdaptTM
Novel Thick Dry Film Photoresist and Process Optimization for High-Aspect Cu Pillar Patterning
Study of 2 x 4 µm Pitch Capsule Shaped TSVs and 2 ìm Pitch TSVs in WoWoW Integration
Bottom-Up Electrodeposition of Small Diameter, High Aspect Ratio Nanotwinned Copper-Filled Through-Silicon Vias for Ultra High-Density 3D Integration
Dry Film Photo-Imageable Dielectric Enabling Glass Core Substrate TGV Filling and Build-Up 1358 Yaming Jiang (DuPont Electronics & Industrial, USA), Patrick Huang (DuPont Electronics & Industrial, R.O.C), Jason Chuang (DuPont Electronics & Industrial, R.O.C), George Yen (DuPont Electronics & Industrial, R.O.C), Zhou Lu (DuPont Electronics & Industrial, USA), Colin Hayes (DuPont Electronics & Industrial, USA), Chris Gilmore (DuPont Electronics & Industrial, USA), LiYen Lin (DuPont Electronics & Industrial, R.O.C), Jeng-Ting Li (Unimicron Hsinchu, R.O.C.), Wei-Tse Ho (Unimicron Hsinchu, R.O.C.), Chi-Hai Kuo (Unimicron Hsinchu, R.O.C.), Bruce P Lin (Unimicron Hsinchu, R.O.C.), Cheng-Ta Ko (Unimicron Hsinchu, R.O.C.), Mike Ma (Unimicron Hsinchu, R.O.C.), and Eugene Lee (DuPont Electronics & Industrial, USA)

Development of Via-First TSV and Backside Interconnect Process for Large-Scale Superconducting Quantum Annealing Circuits	363
Session 34: Reliability of Interconnects in Advanced Packaging	
Impact of Current Stressed SAC305 and Sn-Bi Interconnect Anode and Cathode Side Thermo-Mechanical Stability	.369
Improved Understanding of Electromigration Under AC Loads Impacting Microstructure and Reliability of SAC Solder Interconnects	375
Deterioration of Electromigration Reliability in Microbumps Due to Severe Side Wall Wetting	381
Prediction of Effects of Bi-Addition in SnAgCu Solders on High Strain Rate Properties	386
Low Temperature Solder Reliability Study for Photonics Packages	394

Challenges and Solutions in Measuring Copper-Polymer Interfacial Adhesion Strength in Advanced Packaging	1399
Influence of Doping on the Electromigration Performance of SAC Solder Alloys on BGA Components	1405
Session 35: High -Performance Antenna and RF Design	
3D Vertical Glass Stacking for 6G Communications - Interconnect Fabrication and Broadband Characterization	l 412
Multidisciplinary Design Optimization of High-Speed Ceramic LCCC Package Through Automate FEA Simulation	
On-Chip Shoelace Fully Integrated Inductor	424
Terahertz 300GHz Antenna in Package for 6G Applications 1 M. Sun (Agency for Science, Technology and Research (A*STAR), Republic of Singapore) and T.G. Lim (Agency for Science, Technology and Research (A*STAR), Republic of Singapore)	432

Integration of D-Band 140 GHz III-V Components Transceiver in Embedding PCB-Based
Technology
Tekfouy Lim (Fraunhofer Institute for Reliability and Microintegration
IZM, Germany), Stefan Kosmider (Fraunhofer Institute for Reliability
and Microintegration IZM, Germany), Kavin Senthil Murugesan
(Fraunhofer Institute for Reliability and Microintegration IZM,
Germany), Thi Huyen Le (Fraunhofer Institute for Reliability and
Microintegration IZM, Germany), Marius van Dijk (Fraunhofer Institute
for Reliability and Microintegration IZM, Germany), Johannes Jaeschke
(Fraunhofer Institute for Reliability and Microintegration IZM,
Germany), Ivan Ndip (Fraunhofer Institute for Reliability and
Microintegration IZM, Germany), and Ulrike Ganesh (Fraunhofer
· ·
Institute for Reliability and Microintegration IZM, Germany)
Designing Antennas and RF Components at 110-330 GHz using IPD Technology
Muhammad Ibrahim (University of Oulu, Finland), Kimmo Rasilainen
(University of Oulu, Finland), Jan Saijets (VTT Technical Research
Centre of Finland Ltd.), Pekka Rantakari (VTT Technical Research
Centre of Finland Ltd.), Aarno Pärssinen (University of Oulu,
Finland), and Marko E. Leinonen (University of Oulu, Finland)
G-Band Micromachined 4x1 & 8x1 Crossed Linear Array Antennas
Alexander Wilcher (University of Florida, USA), Shreya Sahai
(University of Florida, USA), Payman Pahlavan (University of Florida,
USA), Alex Phipps (Naval Information Warfare Center (NIWC), USA), Jia
Chieh (Naval Information Warfare Center (NIWC), USA), David Arnold
(University of Florida, USA), and Yong-Kyu Yoon (University of
Florida, USA)
Session 36: Modeling Driven Packaging and Process Advancements
Session 50. Wodering Driven I ackaging and I focess Advancements
Warpage Simulation and Experimental Validation of The X-Dimension Fan-Out
Integration-Bridge Wafer Level Packaging Process
Jian Cheng (JCET Group, China), Liping Zhu (JCET Group, China), Boping
Wu (JCET Group, China), Cheng Yang (JCET Group, China), and Haijie
Chen (JCET Group, China)
Multi-Layer Sequential Fabrication and Mechanics-Based Model of Glass-Core Packages with
Embedded Dies 1460
Alexander R. King (Georgia Institute of Technology, USA), Kaushik
Godbole (Georgia Institute of Technology, USA), Mohanalingam
Kathaperumal (Georgia Institute of Technology, USA), Kyoung-Sik Jack
Moon (Georgia Institute of Technology, USA), Muhannad Bakir (Georgia
Institute of Technology, USA), and Suresh K. Sitaraman (Georgia
Institute of Technology, USA), und Suresh K. Sturumun (Georgia Institute of Technology, USA)
momma of recumology, asres

A Novel Fracture Mechanics Technique on Studying Passivation Crack Behavior for Advanced Si Package with Aluminum Redistribution Layer (Al-RDL) Routing	8
Interface Reliability of Advanced Packaging Under Sequential Stresses of High-Temperature and Temperature-Humidity in Automotive Environments	5
Design and Manufacture of Integrated Passive Devices in Coreless Package Substrates for Power Applications	3
Simulation of Mechanical Cu Pad Expansion Mechanism and Measures to Increase Expansion 148 Takaaki Hirano (Sony Semiconductor Solutions Corporations, Japan), Taichi Yamada (Sony Semiconductor Solutions Corporations, Japan), Yuriko Yamano (Sony Semiconductor Solutions Corporations, Japan), Naoki Komai (Sony Semiconductor Solutions Corporations, Japan), Takumi Onodera (Sony Semiconductor Solutions Corporations, Japan), Yukako Ikegami (Sony Semiconductor Solutions Corporations, Japan), Shoji Kobayashi (Sony Semiconductor Solutions Corporations, Japan), Yoshiya Hagimoto (Sony Semiconductor Solutions Corporations, Japan), and Hayato Iwamoto (Sony Semiconductor Solutions Corporations, Japan)	8
Assessing Solder Joint Reliability Under Multi-Shock Loading by a Cohesive Zone Approach with Irreversible Damage Progression	3

Interactive Presentations 1

Temperature Experiments for A 3D-Printed Encapsulated Thermal MEMS Wind Sensor Under Low Pressure
Sicun Duan (Southeast University, China), Zongyuan Cao (Southeast University, China), Zhenxiang Yi (Southeast University, China), Ming Qin (Southeast University, China), and Qing-An Huang (Southeast University, China)
Deep Learning Enhanced Thermal Simulation for Efficient Semiconductor Layout Design using Thermal Twin
Bin He (Agency for Science, Technology & Research (A*STAR), Singapore), Weiyang Miao (Nanyang Technological University, Singapore), and Gongyue Tang (Agency for Science, Technology & Research (A*STAR), Singapore)
Architecting the Thermal Dissapation and Power Delivery for Large-Scale Systems and
Experimental Demonstration of the Segmented Cooling for Silicon Thermal Dielets With a Power Density of 1 W/mm2
Haoxiang Ren (UCLA Center for Heterogeneous Integration and
Performance Scaling (CHIPS)), Ben Yang (UCLA Center for Heterogeneous
Integration and Performance Scaling (CHIPS)), Naarendharan Sundaram (UCLA Center for Heterogeneous Integration and Performance Scaling
(CHIPS)), Dongkai Shangguan (Thermal Engineering Associates,Inc.),
Timothy Fisher (UCLA Center for Heterogeneous Integration and
Performance Scaling (CHIPS)), and Subramanian Iyer (UCLA Center for
Heterogeneous Integration and Performance Scaling (CHIPS))
Corrosion Analysis of the Electrode Coating in Film Capacitors for Power Electronics
Applications
Sandy Klengel (Fraunhofer IMWS, Germany), Robert Klengel (Fraunhofer
IMWS, Germany), Carola Klute (Fraunhofer IMWS, Germany), and Bolko Mühs-Portius (Fraunhofer IMWS, Germany)
Electromigration Lifetime Improvement of Ball Grid Array Solder Joints for High
Performance Computing Applications
Vishnu Shukla (University of Central Florida, USA), Andrea Molina
Moreno (University of Central Florida, USA), Omar Ahmed (Juniper
Networks, USA), Matthew Ally (University of Central Florida, USA),
Cameron Drewes (University of Central Florida, USA), Miftahul Nabila
(University of Central Florida, USA), Phoebe Cook (University of Central Florida, USA), Kaitlyn Munoz (University of Central Florida,
USA), Jeng Hau Huang (National Taiwan University, Taiwan), Nicholas
Rudawski (University of Florida, USA), Peng Su (Juniper Networks,
USA), Leif Hutchinson (Juniper Networks, USA), Valery Kugel (Juniper
Networks, USA), Bernard Glasauer (Juniper Networks, USA), and Tengfei
Jiang (University of Central Florida, USA)
Interconnect Reliability for Single-Step Sintered Die Stack
Netherlands), Sebastian Quednau (Nanowired GmbH, Germany), Sandy
Klengel (Fraunhofer IMWS, Germany), Robert Klengel (Fraunhofer IMWS,
Germany), Robin Simpson (Nexperia, United Kingdom), René Poelma (Nexperia, The Netherlands), Nick Liu (Nexperia, The Netherlands)
(Nexperia, The Netherlands), Nick Liu (Nexperia, The Netherlands), Sebastian Fritzsche (Heraeus Electronics, Germany), and Frank Krüeger
(Heraeus Electronics, Germany)

Comparison of Mechanical Response and Failure Characteristics of Selected High-Temperature Solder Alloys	6
Sean Y. Lai (Purdue University), Lijia Xie (Purdue University), David N. Halbrooks (Purdue University), Morgana Ribas (MacDermid Alpha), John Blendell (Purdue University), Carol Handwerker (Purdue University), and Ganesh Subbarayan (Purdue University)	
Rapid Estimation of Anisotropic Thermal Conductivity in RDL for 2.5D Chiplet Design	1
A Novel Methodology for Characterizing and Validating Viscoelastic and Thermal Expansion Properties of Polymer Films	7
Enhancing Reliability of Multi-Chip Modules by using the Reinforcement Mechanisms of Side-Fill Technology	1
Characterization of Mechanical behavior of Porous Conductive PDMS-CNT/Graphene based Foams under Multidirectional Strain for Flexible/Stretchable Electronics	3
Leveraging Artificial Intelligence to Enable High-Fidelity Modeling of Substrate Thermo-Mechanical Behavior	4
Artificial Intelligence-Based Warpage Prediction Model for Accelerating Thermo-Mechanical Simulation in Advanced Packaging)

Fast and Accurate Machine Learning Prediction of Back-End-Of-Line Thermal Resistances in Backside Power Delivery and Chiplet Architectures	1577
A Flexible and Scalable Thermal Test Vehicle Design for Electronics Cooling Solutions	1583
An Effective 3D Thermal Network Integrated with Deep Learning for Improved Prediction of the 3D Thermal Properties of Complex Packaging Patterns Jeong-Hyeon Park (Sungkyunkwan University, Republic of Korea), Jaechoon Kim (Samsung Electronics Co., Ltd, Republic of Korea), Sukwon Jang (Samsung Electronics Co., Ltd, Republic of Korea), Sungho Mun (Samsung Electronics Co., Ltd, Republic of Korea), and Eun-Ho Lee (Sungkyunkwan University, Republic of Korea)	1589
Thermal Analysis and Design Guideline of Massive Orthogonal Stacking Assembly of IC (MOSAIC) Cube with Bump Connection Enabling SoC-DRAM Direct Stacking	1595
Raman and X-ray Imaging Based Thermo-Mechanical Characterization of Metal-Embedded Chip Assembly	1601
GA-NN and Explainable AI for IC Packaging Warpage Optimization: A Case Study on Product Feature Yan-Cheng Lin (National Cheng Kung University, Taiwan), Tang-Yuan Chen (Advanced Semiconductor Engineering, Inc., Taiwan), Chen-Chao Wang (Advanced Semiconductor Engineering, Inc., Taiwan), Chih-Pin Hung (Advanced Semiconductor Engineering, Inc., Taiwan), I-An Shou (National Cheng Kung University, Taiwan), and Hung-Kai Wang (National Cheng Kung University, National Tsing Hua University, Taiwan)	1609
A Computational Framework to Predict the Maximum Possible Warpage Due to Package-to-Package Variations	1615

Thermal Characterization of HBMs Integrated via Hybrid Bonding Huicheng Feng (Agency for Science, Technology and Research (A*STAR), Republic of Singapore), Yong Han (Agency for Science, Technology and Research (A*STAR), Republic of Singapore), Gongyue Tang (Agency for Science, Technology and Research (A*STAR), Republic of Singapore), Ling Xie (Agency for Science, Technology and Research (A*STAR), Republic of Singapore), and Vasarla Nagendra Sekhar (Agency for Science, Technology and Research (A*STAR), Republic of Singapore)	1621
An Efficient Data Augmentation and Semantic Segmentation Framework for 3D Defect Detection of HBMs	1628
Yang Yu (A*STAR, Singapore), Jie Wang (A*STAR, Singapore), Richard Chang (A*STAR, Singapore), Ser Choong Chong (A*STAR, Singapore), Ramanpreet Singh Pahwa (A*STAR, Singapore), and Xulei Yang (A*STAR, Singapore)	1020
Warpage Control Mechanism Study of Stiffener on AI Chip IC Packaging	N/A
Digital Design of Inter-Die Gap Fill Dielectric Film Processing for C2W Hybrid Bonding using Finite Element Modelling	1644
Mitigation of Wafer-to-Wafer Bonding Distortions Through Accelerated Simulations and Measurements Oguzhan Orkut Okudur (imec, Belgium), Serena Iacovo (imec, Belgium), Shuo Kang (imec, Belgium), Deewakar Sharma (imec, Belgium), Mario Gonzalez (imec, Belgium), and Eric Beyne (imec, Belgium)	1650
Interactive Presentations 2	
Flexible Glass Electrical Characterization using Aerosol Jet Printing Ethan Kepros (Michigan State University, USA), Bhargav Avireni (Michigan State University, USA), Sambit Kumar Ghosh (Michigan State University, USA), and Premjeet Chahal (Michigan State University, USA)	1656

Bio-Packaging Development of a Wearable Fluidic Monitoring System for Improved Blood Glucose Management in Critically Ill Diabetic Patients	
Rui Qi Lim (Agency for Science, Technology and Research (A*STAR), Singapore), James Yap Ven Wee (Agency for Science, Technology and Research (A*STAR), Singapore), and Ming-Yuan Cheng (Agency for Science, Technology and Research (A*STAR), Singapore)	
Parasitic Extraction and Signal Integrity Analysis of Memristor-Based Crossbar Arrays for Neuromorphic Computing	
Broadband Optical Engine System Integration by Wafer Level Process in HPC/AI Era	
Cost-Effective Package Design for a Chiplet Interfaces on Organic Substrates using Low Cost Design Rules	
Signal and Power Integrity Optimization using Novel Bridge Die and Copper Post Interconnect Design in 2.xD Packaging for Wide I/O Applications	
Systematic Crosstalk Reduction Methods towards PCIe 7.0 PAM4 Transmission on Lopro FPIO Connectors	

A Dual Mode Brillouin/Low-Frequency Raman Spectroscopy Microscope for Local Mechanical Property Imaging for Semiconductor Packaging Materials	1694
Packaging and Integration of Multifunctional Brain Computer Interface Ziqi Jia (University of Florida, USA), Ariel David Cerpa (University of Florida, USA), Gloria J. Kim (University of Florida, USA), and Yong-Kyu Yoon (University of Florida, USA)	1702
A K-Band Circularly Polarized Antenna for Short-Range Communication Applications	1706
Design Enablement Methodology for 3D Stacked RF Systems Raju Mani (Technology and Research (A*STAR), Republic of Singapore), Dutta Rahul (Technology and Research (A*STAR), Republic of Singapore), Tengiz Svimonishvili (Technology and Research (A*STAR), Republic of Singapore), Mihai D. Rotaru (Technology and Research (A*STAR), Republic of Singapore), and Vignesh Shanmugam Bhaskar (Technology and Research (A*STAR), Republic of Singapore)	1710
Leveraging Advanced Packaging for IP Protection in Heterogeneous AI Hardware	1716
A Compact Dual Band (28/39 GHz) 1x4 Antenna Array Design with Frequency Selective Surface-Base (FSS) for 5G AiP Applications	1723
Large-Scale Spaceborne Deployable Active Phased-Array Antenna Design Using Rigid-Flex Boards for LEO Satellite Constellation	1728

A 6G Terahertz 256-Element Dual-Polarized MIMO Antenna Array with Low-Profile and Broadband	1735
Xin Zhang (Chinese Academy of Sciences, China), Yuxiang Zheng (Chinese Academy of Sciences, China), Fengze Hou (Chinese Academy of Sciences, China), and Qidong Wang (Chinese Academy of Sciences, China)	
Time-Efficient Eye-Opening Estimation Method for High-Bandwidth Memory Interface Design with Equalizers	1740
Joonhyun Kim (Samsung Electronics, Co. Ltd, South Korea), Sungwook Moon (Samsung Electronics, Co. Ltd, South Korea), and Yongho Lee (Samsung Electronics, Co. Ltd, South Korea)	
Machine Learning-Optimized Metasurface Matching Layer for Enhanced Deep Fat Sensing using PDMS and Copper Tape	1745
Prediction of Cross Section Images and Optimization of Processes with Neural Network	1751
AI-Driven Automatic Routing for UCIe Bridge with Heterogeneous Configurations in Advanced System-in-Package	1757
Additive Manufacturing of Passive Electronic Components using Aerosol Jet Printing and Reliability Tests for Spaceborne Applications	1765
Novel Wireless PVDF-PEDOT:PSS/LIG Based Wearable Multimodal Sensing Platform	1773

Quasi-Coaxial Through-Hole Integrated Additively Manufactured Antenna-in-Package Lid	770
Substrates1 Nahyeon Kim (Ulsan National Institute of Science and Technology	L779
(UNIST), South Korea), Haksoon Jung (Ulsan National Institute of	
Science and Technology (UNIST), Republic of Korea), Yurim Choi (Ulsan	
National Institute of Science and Technology (UNIST), Republic of	
Korea), Hyeongjun Kim (Ulsan National Institute of Science and	
Technology (UNIST), Republic of Korea), Seongju Kim (Ulsan National	
Institute of Science and Technology (UNIST), Republic of Korea),	
Yongwoo Lee (Ulsan National Institute of Science and Technology	
(UNIST), Republic of Korea), Yunsik Park (Korea Electronics Technology	
Institute (KETI), Republic of Korea), Seungyeon Koh (University of	
Seoul, Republic of Korea), Hyeok Kim (University of Seoul, Republic of Korea), and Jimin Kwon (Ulsan National Institute of Science and	
Technology (UNIST), Republic of Korea)	
1 1	1784
Anthony P. Kotula (National Institute of Standards and Technology,	
USA), Ran Tao (National Institute of Standards and Technology, USA),	
Jianwei Tu (National Institute of Standards and Technology, USA), Young Jong Lee (National Institute of Standards and Technology, USA),	
and Gale A. Holmes (National Institute of Standards and Technology,	
USA)	
Shintaro Goto (Tohoku University, Japan), Shogo Koseki (Tohoku University, Japan), Kai Takeuchi (Tohoku University, Japan), and Eiji	l 7 91
Higurashi (Tohoku University, Japan)	
Capping Layers for Enhanced Crystallinity of Single-Crystal Germanium on Insulator in	
	1795
Van Mina Dan (Mational Vana Mina Chigo Tana Hairangita Tairna)	
Yu-Ming Pan (National Yang Ming Chiao Tung University, Taiwan),	
Ching-Lin Chen (National Yang Ming Chiao Tung University, Taiwan),	
Ching-Lin Chen (National Yang Ming Chiao Tung University, Taiwan), Hao-Tung Chung (National Yang Ming Chiao Tung University, Taiwan),	
Ching-Lin Chen (National Yang Ming Chiao Tung University, Taiwan), Hao-Tung Chung (National Yang Ming Chiao Tung University, Taiwan), Chiao-Yen Wang (National Yang Ming Chiao Tung University, Taiwan),	
Ching-Lin Chen (National Yang Ming Chiao Tung University, Taiwan), Hao-Tung Chung (National Yang Ming Chiao Tung University, Taiwan), Chiao-Yen Wang (National Yang Ming Chiao Tung University, Taiwan), Nien-Chih Lin (Taiwan Semiconductor Research Institute, Taiwan),	
Ching-Lin Chen (National Yang Ming Chiao Tung University, Taiwan), Hao-Tung Chung (National Yang Ming Chiao Tung University, Taiwan), Chiao-Yen Wang (National Yang Ming Chiao Tung University, Taiwan), Nien-Chih Lin (Taiwan Semiconductor Research Institute, Taiwan), Chih-Chao Yang (Taiwan Semiconductor Research Institute, Taiwan),	
Ching-Lin Chen (National Yang Ming Chiao Tung University, Taiwan), Hao-Tung Chung (National Yang Ming Chiao Tung University, Taiwan), Chiao-Yen Wang (National Yang Ming Chiao Tung University, Taiwan), Nien-Chih Lin (Taiwan Semiconductor Research Institute, Taiwan), Chih-Chao Yang (Taiwan Semiconductor Research Institute, Taiwan), Chang-Hong Shen (Taiwan Semiconductor Research Institute, Taiwan), and	
Ching-Lin Chen (National Yang Ming Chiao Tung University, Taiwan), Hao-Tung Chung (National Yang Ming Chiao Tung University, Taiwan), Chiao-Yen Wang (National Yang Ming Chiao Tung University, Taiwan), Nien-Chih Lin (Taiwan Semiconductor Research Institute, Taiwan), Chih-Chao Yang (Taiwan Semiconductor Research Institute, Taiwan), Chang-Hong Shen (Taiwan Semiconductor Research Institute, Taiwan), and Kuan-Neng Chen (National Yang Ming Chiao Tung University, Taiwan)	1800
Ching-Lin Chen (National Yang Ming Chiao Tung University, Taiwan), Hao-Tung Chung (National Yang Ming Chiao Tung University, Taiwan), Chiao-Yen Wang (National Yang Ming Chiao Tung University, Taiwan), Nien-Chih Lin (Taiwan Semiconductor Research Institute, Taiwan), Chih-Chao Yang (Taiwan Semiconductor Research Institute, Taiwan), Chang-Hong Shen (Taiwan Semiconductor Research Institute, Taiwan), and Kuan-Neng Chen (National Yang Ming Chiao Tung University, Taiwan) Novel Optical Chiplet Structure Based on MCeP®	1800
Ching-Lin Chen (National Yang Ming Chiao Tung University, Taiwan), Hao-Tung Chung (National Yang Ming Chiao Tung University, Taiwan), Chiao-Yen Wang (National Yang Ming Chiao Tung University, Taiwan), Nien-Chih Lin (Taiwan Semiconductor Research Institute, Taiwan), Chih-Chao Yang (Taiwan Semiconductor Research Institute, Taiwan), Chang-Hong Shen (Taiwan Semiconductor Research Institute, Taiwan), and Kuan-Neng Chen (National Yang Ming Chiao Tung University, Taiwan) Novel Optical Chiplet Structure Based on MCeP®	1800
Ching-Lin Chen (National Yang Ming Chiao Tung University, Taiwan), Hao-Tung Chung (National Yang Ming Chiao Tung University, Taiwan), Chiao-Yen Wang (National Yang Ming Chiao Tung University, Taiwan), Nien-Chih Lin (Taiwan Semiconductor Research Institute, Taiwan), Chih-Chao Yang (Taiwan Semiconductor Research Institute, Taiwan), Chang-Hong Shen (Taiwan Semiconductor Research Institute, Taiwan), and Kuan-Neng Chen (National Yang Ming Chiao Tung University, Taiwan) Novel Optical Chiplet Structure Based on MCeP®	1800
Ching-Lin Chen (National Yang Ming Chiao Tung University, Taiwan), Hao-Tung Chung (National Yang Ming Chiao Tung University, Taiwan), Chiao-Yen Wang (National Yang Ming Chiao Tung University, Taiwan), Nien-Chih Lin (Taiwan Semiconductor Research Institute, Taiwan), Chih-Chao Yang (Taiwan Semiconductor Research Institute, Taiwan), Chang-Hong Shen (Taiwan Semiconductor Research Institute, Taiwan), and Kuan-Neng Chen (National Yang Ming Chiao Tung University, Taiwan) Novel Optical Chiplet Structure Based on MCeP®	1800

Die-to-Die Bonding Development Employing Atomic Layer Deposition to Enable Heterogeneous Integration of Optoelectronic Integrated Circuits
Interactive Presentations 3
An Innovative Flux-Less Solder Ball Attachment Technology (FLAT) for Advanced BGA Assembly 1811 Dongjin Kim (Korea Institute of Industrial Technology, South Korea), Seonghui Han (Korea Institute of Industrial Technology, South Korea), Sang Eun Han (Korea Institute of Industrial Technology, South Korea), Dong-Gyu Choi (Korea Institute of Industrial Technology, South Korea), Sehoon Yoo (Korea Institute of Industrial Technology, South Korea), Eunchae Kim (Prinsol Co., Ltd, South Korea), and Kwansik Chung (Prinsol Co., Ltd, South Korea)
Technology for Forming Micro Vias Smaller Than 20 µm With Low Surface Roughness on Build-Up Films Using UV Nanosecond Laser Drilling and Plasma Desmearing
Fabrication of D-band (140 GHz) Broadband Antenna using Quartz Glass on Silicon Hybrid Bonded Wafer with Cavity
The Role of Preparation and Bonding Parameters in Improving Hybrid Bonding Quality

High Precision Large Reticle Thermo-Compression Bonding for Advanced Packaging for AI Era . Shripad Gokhale (Intel Corporation, USA), Kartik Srinivasan (Intel Corporation, USA), Shan Zhong (Intel Corporation, USA), and Anurag Tripathi (Intel Corporation, USA)	1832
Electrical Performance of CMP Process for Hybrid Bonding Application with Conventional / nt-Cu and Low Temperature of Si_xN_y / Si_xO_y Dielectrics	1837
IR Laser Debonding for Silicon Based Temporary Carrier Systems Enabling 2.5D and 3D Chiplet Integration Processes	1843
Hydrophobic Barrier for Controlled Epoxy Keep-Out-Zone in Flip Chip Assembly	1848
Accelerating Root Cause Identification of Subtle Bonding Failures using Microwave Induced Plasma Charles Odegard (Texas Instruments, Inc., USA), Daniel Scott (Texas Instruments, Inc., USA), Olivia Bonin (Texas Instruments, Inc., USA), Yashan Peng (JIACO Instruments B.V., The Netherlands), Jiaqi Tang (JIACO Instruments B.V., The Netherlands), Mark McKinnon (JIACO Instruments B.V., The Netherlands), and Kees Beenakker (Delft University of Technology, The Netherlands)	1854
Wet-Chemical Cu Cleaning for Fine-Pitch Hybrid Bonding Kohei Nakayama (YOKOHAMA National University, Japan), Kenta Hayama (Yokohama National University, Japan), Fabiana Tanaka (Yokohama National University, Japan), Sven Dewilde (imec, Belgium), Steven Deckers (imec, Belgium), Nancy Heylen (imec, Belgium), Yoichi Tanaka (Kurita Water Industries Ltd., Japan), Yusuke Okazaki (Kurita Water Industries Ltd., Japan), Nobuko Gan (Kurita Water Industries Ltd., Japan), Hideaki Iino (Kurita Water Industries Ltd., Japan), Fumihiro Inoue (Yokohama National University, Japan), and Harold Philipsen (imec, Belgium)	1859

Die-Attach Materials	1864
Babatunde Falola (Binghamton University, USA), Riadh Al-Haidari (Binghamton University, USA), Olya Noruz Shamsian (Binghamton University, USA), Udara Somarathna (Binghamton University, USA), Bryan Cabrera (Binghamton University, USA), Mousa AL-Zanina (Binghamton University, USA), Mohammed Alhendi (Binghamton University, USA), Mark Poliks (Binghamton University, USA), Gurvinder Singh Khinda (GE HealthCare, USA), Nancy Stoffel (GE Research, USA), Tzu-Jen Kao (GE HealthCare, USA), and Rafael Tudela (Tapecon Inc., USA)	
Riadh Al-Haidari (Binghamton University), Babatunde Falola (Binghamton University), Zhi Dou (Binghamton University), Mark Schadt (Binghamton University), Mohammed Alhendi (Binghamton University), Mark Poliks (Binghamton University), Ekaterina Dvoretskaya (SunRay Scientific,Inc.), and Andrew Stemmermann (SunRay Scientific,Inc.)	1872
A Mild Surface Activation Under Redox Gases using Vacuum Ultraviolet Irradiation for Interconnection of Semiconductor Packaging	1879
Demonstration of a Fully Integrated, High Bandwidth, Active Flexible Connector for Large Area Computational Systems Randall Irwin (UCLA Center for Heterogeneous Integration and Performance Scaling, USA), Joanna Fang (UCLA Center for Heterogeneous Integration and Performance Scaling, USA), and Subramanian S. Iyer (UCLA Center for Heterogeneous Integration and Performance Scaling, USA)	1884
A High Throughput Low-Temperature Copper-Copper Thermal Compression Bonding Scheme us Tin Overlayer Tanmay S. Konnur (UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS), USA), Krutikesh Sahoo (UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS), USA), Randall Irwin (UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS), USA), Vineeth Harish (UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS), USA), Jui-Han Liu (UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS), USA), and Subramanian S. Iyer (UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS), USA)	_
Advanced Face-To-Back CoW 2.0-µm Pitch Cu-Cu Hybrid Bonding Process for Three Layer-Stacked 3D Heterogenous Integration. Akihiro Urata (Sony Semiconductor Solutions Corporation), Takahiro Kamei (Sony Semiconductor Solutions Corporation), Itsuki Imanishi (Sony Semiconductor Solutions Corporation), Masanori Chiyozono (Sony Semiconductor Solutions Corporation), Toru Osako (Sony Semiconductor Solutions Corporation), Kan Shimizu (Sony Semiconductor Solutions Corporation), Yoshihisa Kagawa (Sony), and Hayato Iwamoto (Sony Semiconductor Solutions Corporation)	1895

Process Technology Enablers for Aggressive Scaling of Hybrid Bonding Temperature and Pitch. Kai Ma (Applied Materials, Inc., USA), Lei Xue (Applied Materials, Inc., USA), Eric Bergman (Applied Materials, Inc., USA), Nikolaos Bekiaris (Applied Materials, Inc., USA), Taketo Sekine (Applied Materials, Inc., USA), Ching-Hsiang Hsu (Applied Materials, Inc., USA), Santosh Rath (Applied Materials, Inc., USA), Taotao Ding (St.Florian am Inn, Austria), Barbara Weis (St.Florian am Inn, Austria), Gernot Probst (St.Florian am Inn, Austria), Thomas Uhrmann (St.Florian am Inn, Austria), and Markus Wimplinger (St.Florian am Inn, Austria)	1901
High-Quality Cu μ-Joints by High-Throughput Contactless Hot-Isostatic-Pressure (HIP) Annealing for Chip-to-Wafer and Wafer-to-Wafer Hybrid Bonding	1908
Fabrication of Panel-Level Redistribution Interposer with 1.5/1.5 µm Multilayer Fine Wiring and Solutions to Issues of Miniaturization Masashi Minami (Resonac Corporation, Japan), Sachiko Matsushita (Resonac Corporation, Japan), and Sadaaki Katoh (Resonac Corporation, Japan)	1915
Polyimide Fine Via and Trench Formation Based on Plasma Etching Technology for RDL Interposer	1920
Development and Characterization of Electrodeposited Tin-Indium Alloy Microbumps for Low Temperature Assembly	1924
Effect of Dimension on Thermal Expansion of Cu Pads in SiO2 Vias for 3D IC Fine-Pitch Hybrid Bonding Pin-Lin Chen (National Yang Ming Chiao Tung University (NYCU), Taiwan) and Chih Chen (National Yang Ming Chiao Tung University (NYCU), Taiwan)	1929
Impact of Temporary Substrates and Adhesives on Die-to-Wafer Overlay	1934
Patterning of Sub 1 µm CD TSV and Bond Pad for Fine-pitch 2.5D/3D Hybrid Bonding Applications	1939

Process Development, Challenges, and Strategies for Void-Free Multi-Chip Stacking in
Hybrid Bonding Applications
Ser Choong Chong (Institute of Microelectronics (IME), Agency for
Science, Technology and Research (A*STAR), Republic of Singapore),
Ling Xie (Institute of Microelectronics (IME), Agency for Science,
Technology and Research ($A*STAR$), Republic of Singapore), Vasarla
Nagendra Sekhar (Institute of Microelectronics (IME), Agency for
Science, Technology and Research ($A*STAR$), Republic of Singapore),
Mishra Dileep Kumar (Institute of Microelectronics (IME), Agency for
Science, Technology and Research ($A*STAR$), Republic of Singapore),
B.S.S. Chandra Rao (Institute of Microelectronics (IME), Agency for
Science, Technology and Research (A*STAR), Republic of Singapore), and
Vempati Srinivasa Rao (Institute of Microelectronics (IME), Agency for
Science, Technology and Research ($A*STAR$), Republic of Singapore)
Ozone-Ethylene Radical Activation of SiCN/Cu without Water Rinsing for Hybrid Bonding 1948 Bungo Tanaka (Tohoku University, Japan), Murugesan Mariappan (Tohoku University Sendai, Japan), Soichiro Motoda (MEIDEN NANOPROCESS INNOVATIONS, INC., Japan), Tetsuya Nishiguchi (MEIDEN NANOPROCESS INNOVATIONS, INC., Japan), Yuma Okadome (MEIDEN NANOPROCESS INNOVATIONS, INC., Japan), Tetsu Tanaka (Tohoku University, Japan), and Takafumi Fukushima (Tohoku University, Japan)
Environmentally Friendly Cu Post Technology Based on Laser-Assisted Bonding with Compression (LABC) and Fume-Free Laser Solder Paste for Advanced 3D Interconnections
Through GaN Via for 3D Heterogeneous Strata Integration

Microbump Interconnections Using Vertical Wire Technology for the Power Connections between SoC and Substrate in the Bridge Die-Based Packaging Platform	1964
Novel Fault Isolation Methodology Applied on Nano-Scale Defect in Fine Line RDL for Advanced Fan-Out Package	1970
Interactive Presentations 4	
Improving the Uniformity of Cu Deposition in Fan-Out Panel Level Package with FEM Simulation Model	1975
Lithography-Free Anisotropic Magnetoresistance Sensor-Based Rotational Speed Measurement System on PEEK with Integrated Electronics Tim Nils Bierwirth (Leibniz University Hannover, Germany), Sebastian Bengsch (Ensinger GmbH, Germany), Eike Christian Fischer (Freelancer, Germany), Michael Werner (Ensinger GmbH, Germany), and Marc Christopher Wurz (Leibniz University Hannover, Germany)	1981
Effect of Plasma Etching and Color Difference of the Molding Compound Surface on Adhesion in Electromagnetic Shielding	1986
Integrated Passive Devices in the Silicon Interconnect Fabric Haoxiang Ren (UCLA Center for Heterogeneous Integration and Performance Scaling (UCLA CHIPS), CA), Zoe Chen (UCLA Center for Heterogeneous Integration and Performance Scaling (UCLA CHIPS), CA), Jui-Han Liu (UCLA Center for Heterogeneous Integration and Performance Scaling (UCLA CHIPS), CA), Cheng-Ting Yang (UCLA Center for Heterogeneous Integration and Performance Scaling (UCLA CHIPS), CA), Ben Yang (UCLA Center for Heterogeneous Integration and Performance Scaling (UCLA CHIPS), CA), Boris Vaisband (UCLA Center for Heterogeneous Integration and Performance Scaling (UCLA CHIPS), CA; University of California, CA), and Subramanian S. Iyer (UCLA Center for Heterogeneous Integration and Performance Scaling (UCLA CHIPS), CA)	1994

Parametric Analysis of Thermo-Mechanical Behavior for HBM in System-In-Package
Configurations 1999
Hyunggyun Noh (Samsung Electronics, South Korea), Wonhong Choi
(Samsung Electronics, South Korea), Woongkee Kim (Samsung Electronics,
South Korea), Gunhee Bae (Samsung Electronics, South Korea), Yumi Sim
(Samsung Electronics, South Korea), Seungyeon Kim (Samsung
Electronics, South Korea), Yuchul Hwang (Samsung Electronics, South
Korea), and Yunsung Lee (Samsung Foundry)
A Highly Reliable Filling Method for Package-on-Package Utilizing Epoxy Flux2004
Kisu Joo (Samsung Electronics Co. Ltd., Korea), Yongju Lee (Samsung
Electronics Co. Ltd., Korea), Minki Ahn (Samsung Electronics Co. Ltd.,
Korea), Kyojin Hwang (Samsung Electronics Co. Ltd., Korea), Daehyun
Kim (Samsung Electronics Co. Ltd., Korea), Junghwa Kim (Samsung
Electronics Co. Ltd., Korea), and Heeseok Lee (Samsung Electronics Co.
Ltd., Korea)
Comprehensive Analysis of the Impact of Various Surface Modification Techniques on
Difficult-to-Adhesion Resin
Akihiro Shimizu (Ushio Inc., Japan) and Shinichi Endo (Ushio Inc.,
Japan)
A Novel Disaggregated Approach of Assembling Integrated Heat Spreader for Advanced
Packages
Arifur Chowdhury (Intel Corporation, USA), Jaclyn Avallone (Intel
Corporation, USA), Bamidele D. Falola (Intel Corporation, USA), Taylor
Gaines (Intel Corporation, USA), Haowen Liu (Intel Corporation, USA),
Peng Li (Intel Corporation, USA), Sergio A Chan Arguedas (Intel
Corporation, USA), and Aravindha R Antoniswamy (Intel Corporation,
USA)
Characterization of FOWLP Process using Temporary Bonding Materials on Carrier with Very
Low Die Shift 2022
Tiffany Tang (imec, Belgium), Alice Guerrero (Brewer Science,
Belgium), Dieter Cuypers (imec, Belgium), Maarten Macours (imec,
Belgium), Aldrin Vaquilar (imec, Belgium), Pieter Bex (imec, Belgium),
Koen Kennes (imec, Belgium), Alain Phommahaxay (imec, Belgium), Gerald
Beyer (imec, Belgium), and Eric Beyne (imec, Belgium)
Wafer-to-Wafer Bonding With Saddle-Shaped Wafers
Shuo Kang (imec), Serena Iacovo (imec), Koen D (imec), Oguzhan Orkut
Okudur (imec), Anton Alexeev (EV Group), Thomas Plach (EV Group),
Taotao Ding (EV Group), and Markus Wimplinger (EV Group)
, , , , , , , , , , , , , , , , , , , ,
Novel Packaging Platform Based on Bridge Dies with Top and Bottom I/O Connections on
Standard Substrates
Micron Inc., Republic of Korea), Yong Gyu Jang (HANA Micron Inc.,
Republic of Korea), Yongnam Koh (HANA Micron Inc., Republic of Korea),
Jin-Wook Jang (HANA Micron Inc., Korea), and Jayden Donghyun Kim (HANA
Micron Inc., Korea)
TIME OF THE ACTION

Advanced Resin Material Enabling Room-Temperature Bonding for WOW and COW 3DI Applications	. 2039
Bond Wave Analysis of SiCN for Fine Pitch Hybrid Bonding Ryosuke Sato (YOKOHAMA National University, Japan), Atsushi Nagata (Tokyo Electron Kyushu Limited, Japan), Hayato Kitagawa (YOKOHAMA National University, Japan), Yoshihiro Kondo (Tokyo Electron Kyushu Limited, Japan), Kenichi Saito (Tokyo Electron Limited, Japan), Junghwan Park (SK hynix Inc, Korea), Chiwoo Ahn (SK hynix Inc, Korea), Yeoun-Soo Kim (SK hynix Inc, Korea), Jiho Kang (SK hynix Inc, Korea), and Fumihiro Inoue (YOKOHAMA National University, Japan)	. 2046
Characterization of Interfacial Fracture Strength in Hybrid Bonded Wafers: A Novel Approach for High-Resolution Spatial Profiling	. 2054
Laminate Materials with Excellent Co-Planarity and Dimensional Stability for Advanced 2.xD Package	. 2059
Rapid Dendritic Amplification of Amino Groups on BN Surfaces for Enhanced Thermal Conductivity in Polymer Composites	. 2065
VCS (Vertical Copper Post Stack) for on-Device AI Memory Solution	. 2069
Experimental Demonstration of High-Power Thermal Test Vehicle using Two-Phase Cooling for AI Datacenters, 5G RAN, and Edge Compute Nodes	. 2074

Addressing Key Process Challenges in Developing High Aspect Ratio TSVs up to 15 with 1 µm Critical Dimension
Development of High Thermal Conductance Wafer Bonding Interface with PVD Aluminum Nitride 2086 Andrew Tuchman (TEL Techonology Center, America, LLC, USA), Ayuta Suzuki (TEL Techonology Center, America, LLC, USA), Joshua Greklek (TEL Techonology Center, America, LLC, USA), Joshua Peck (TEL Techonology Center, America, LLC, USA), Rinus Lee (TEL Techonology Center, America, LLC, USA), and Ilseok Son (TEL Techonology Center, America, LLC, USA)
Electrolytic Copper Plating Process for Glass Substrate
The Formation of Microvia with a Diameter of 3.5 µm and an Aspect Ratio of 3 in Ajinomoto Build-up Film® (ABF) using KrF Excimer Laser Ablation
Efficient Utilization of Different Kinds of Superelements for Thermo-Mechanical Reliability FE-Analysis of Chiplets
Mechanical Strength and Pad Cratering Risk Determination of High-Speed PCBs via Physical Testing and Numerical Simulation

Student Interactive Presentations

Characterization of the Mechanical and Thermal Properties of SAC+Bi Phases in Hybrid SAC/LTS Solder Joints	2117
Pick-and-Release: A Novel Contactless Bonding Method for Die Attachment 2 Ahmed Abdelwahab (Delft University of Technology, Netherlands), Henk van Zeijl (Delft University of Technology, Netherlands), Remco van Hoorn (ITEC, Netherlands), Hans Kuipers (ITEC, Netherlands), and Massimo Mastrangeli (Delft University of Technology, Netherlands)	2125
Assessment of Electromagnetic Board Level Shielding using Continuous Carbon Fiber	2133
3D Coupled Line Inductors with Through-Glass Vias for Compact Passive Circuit Integration in Glass Packages	2140
Design, Fabrication and Characterization of a 3D-Printed Radix^TM-Based Patch Antenna for 5G mmWave Applications	2145
Enhancing Runtime Security in Heterogeneous System-in-Package Through a Chiplet-Based Root-of-Trust	2150

Physics-Informed Neural Networks for SAM Image Enhancement with a Novel Physics-Constrained Metric for Advanced Semiconductor Packaging Inspection	2158
Thermo-Seal: A Multi-Layered InfraRed Watermarking Scheme for On-Field IC Provenance Verification Using Thermal Signatures M Shafkat M Khan (University of Florida, USA), Tyla E Hart (University of Florida, USA), Himanandhan Reddy Kottur (University of Florida, USA), Liton Kumar Biswas (University of Florida, USA), Nitin Varshney (University of Florida, USA), Stephan R. Larmann (InfraTec Infrared LLC), and Navid Asadizanjani (University of Florida, USA)	2166
Facile Fabrication for Flexible Pressure Sensor using FDM-Type 3D Printing Technology Junyoung Park (Hanyang University, South Korea) and Hongyun So (Hanyang University, South Korea)	2174
Electrospray Deposited Silver Films for Electromagnetic Interference (EMI) Protection on Insulating Targets Emma E. Pawliczak (State University of New York at Binghamton, USA) and Paul R. Chiarot (State University of New York at Binghamton, USA)	2180
Scalable Metamaterial Antenna Arrays with Reduced Mutual Coupling for SWaP-Constrained Applications	2187
Heterogeneous Integration of Memristor Emulator for Low Power Computing Zohreh Salehi (University of Illinois, USA), Hanzhi Ma (Zhejiang University, China), Yi Zhou (University of Illinois, USA), Tahsin Shameem (University of Illinois, USA), and Jose E. Schutt-Aine (University of Illinois, USA)	2192
UCIe-A Mimic Channel Design and Verification for Early On-Chip System Validation	2199

Organic and Hybrid Nanoscale Films for Low Loss Direct Glass-Copper Metallization	2206
Optimization of Reflow Profile for Solder Thermal Interface Materials with an Inline Vacuum Oven Piyush Kulkarni (Binghamton University, USA), Ali Davoodabadi (Universal Instruments Corporation, USA), and Scott Schiffres (Binghamton University, USA)	2211
Characterization of Dielectric Materials Beyond Room Temperature using the Lab-Developed Temperature Split Cavity (TSC) Method	2218
Ultra-Thin Chiplet Embedding in Glass-Core Package Redistribution Layers	2224
High-Frequency Multi-Chip RF Module Enabled by Fused-Silica Stitch-Chip Technology: RF and Interconnect Characterization	
Universal Micropatterning Technique for High Density Die Packaging	2237
Void Formation Elimination in Ultra-Thin Au-Sn Solid-Liquid Interdiffusion Bonding using Rapid Cooling Process for Advanced Packaging and MEMS Applications	2243
3D Heterogeneous Integration of Packaged Dies for Flexible FOWLP Micro-Display using Low? Temperature Solder Bonding on FlexTrate^TM	2248

Enhancing Reliability of 30 μm-Pitch Interconnections by Optimizing Material Properties of Laser Non-Conductive Paste (LNCP) for Room Temperature Laser-Assisted Bonding with
Compression (LABC)
Gaeun Lee (Electronics and Telecommunications Research Institute,
Korea), Jiho Joo (Electronics and Telecommunications Research
Institute, Korea), Ki-Seok Jang (Electronics and Telecommunications
Research Institute, Korea), Yong-Sung Eom (Electronics and
Telecommunications Research Institute, Korea), Gwang-Mun Choi
(Electronics and Telecommunications Research Institute, Korea), Jungho
Shin (Electronics and Telecommunications Research Institute, Korea),
Chanmi Lee (Electronics and Telecommunications Research Institute,
Korea), Jin-Hyuk Oh (Electronics and Telecommunications Research
Institute, Korea), Jieun Jung (Electronics and Telecommunications
Research Institute, Korea), Seong-Cheol Kim (Electronics and
Telecommunications Research Institute, Korea), Seung-Yoon Lee (Hanbat
National University, Korea), and Kwang-Seong Choi (Electronics and
Telecommunications Research Institute, Korea)
An Innovative TSV based Integrated Voltage Regulator
Rui Huang (Northeastern University), Haowen Li (Northeastern
University), M. Sun (Northeastern University), N.X. Sun (Northeastern
University), Xiaoling Shi (Winchester Technologies, LLC), Hwaider Lin
(Winchester Technologies, LLC), Hui Lu (Winchester Technologies, LLC),
Mohan Sanghadasa (US Army DEVCOM Aviation & Missile Center Redstone),
Chenyang Zhu (Clemson University), and Xin Zhao (Clemson University)
Kinetic Evolution and Phase Transformation of Ni/In and Cu/In Intermetallics
Tassawar Hussain (KU Leuven), Jaber Derakhshandeh (imec), Tom Cochet
(imec), Ehsan Shafahian (imec), Prathamesh Dhakras (imec), Aksel
Goehnermeier (Carl Zeiss Microscopy GmbH), Eric Beyne (imec), and
Ingrid De Wolf (imec)
· ·
High Aspect Ratio Spiral Inductor with Progressive Turn Widths for Embedded Power Converters
Rami Rasheedi (University of Illinois Chicago, USA) and Inna
Partin-Vaisband (University of Illinois Chicago, USA)
Efficient Scalable Thermoelectric Modeling of High-Frequency Cylindrical Interconnects for
Heterogeneous Package Arrays 2278
Mohamed Gharib (University of Illinois Chicago, USA) and Inna
Partin-Vaisband (University of Illinois Chicago, USA)
Hybrid Voltage Regulators for High Performance Computing: Analytical Models and Design
Methodology
Salma Abdelzaher (University of Illinois Chicago, USA), Mohamed Gharib
(University of Illinois Chicago, USA), and Inna Partin-Vaisband
(University of Illinois Chicago, USA)
Imaging Assisted Dual Sided Light Coupling Technique for Propagation Loss Estimation of
Waveguide Interconnects
Abhinandan Hazarika (University College Cork, Ireland), Brendan
Roycroft (University College Cork, Ireland), Muhammet Genc (Tyndall
National Institute, Ireland), Brian Corbett (University College Cork,
Ireland), and Zhi Li (University College Cork, Ireland)

Chao-Yang Chiang (National Tsing Hua University, Taiwan), Po-Hsun He (National Tsing Hua University, Taiwan), Yu-Hsiang Chang (Advanced Semiconductor Engineering, Inc., Taiwan), Hung-Hsien Huang (Advanced Semiconductor Engineering, Inc., Taiwan), Chen-Chao Wang (Advanced Semiconductor Engineering, Inc., Taiwan), Chih-Pin Hung (Advanced Semiconductor Engineering, Inc., Taiwan), and Chien-Neng Liao (National Tsing Hua University, Taiwan)	Direct-on-Chip Two-Phase Microjet Cooling with Surface-Enhanced Electrodeposited Microporous Structures Keyu Wang (Purdue University, IN), Ketankumar Jayantkumar Yogi (Purdue University, USA), Gopinath Sahu (Purdue University, USA), Aaron Du (Purdue University, USA), and Tiwei Wei (Purdue University, IN)	2300
Yun-Hsuan Chen (National Yang Ming Chiao Tung University (NYCU), Taitvan), Guan-Zhe You (National Tsing Hua University (NTHU), Taitvan), Pin-Syuan He (National Yang Ming Chiao Tung University (NYCU), Taitvan), Yi-Chen Chung (National Yang Ming Chiao Tung University (NYCU), Taitvan), Rou-Jun Lee (National Yang Ming Chiao Tung University (NYCU), Taitvan), Rou-Jun Lee (National Yang Ming Chiao Tung University (NYCU), Taitvan), Chien-Yu Liu (National Yang Ming Chiao Tung University (NYCU), Taitvan), Chang-Chun Lee (National Tsing Hua University (NYCU), Taitvan), and Chih Chen (National Yang Ming Chiao Tung University (NYCU), Taitvan) High-Power Vapor Chambers with Hierarchical Dendritic Wick Structures for High-Performance Computing Systems N/A Chao-Yang Chiang (National Tsing Hua University, Taitvan), Po-Hsun He (National Tsing Hua University, Taitvan), Yu-Hsiang Chang (Advanced Semiconductor Engineering, Inc., Taitvan), Hung-Hsien Huang (Advanced Semiconductor Engineering, Inc., Taitvan), Chih-Pin Hung (Advanced Semiconductor Engineering, Inc., Taitvan), Chih-Pin Hung (Advanced Semiconductor Engineering, Inc., Taitvan), and Chien-Neng Liao (National Tsing Hua University, Taitvan) Measurement of Thermal, Humidity, Solder and Aging Effects of Mechanical Stress and Silicon Circuit Electrical Performance in Quad Flat Packages 2325 Carl Riehm (Technical University of Munich, Germany), Szabolcs Molnar (Technical University of Munich, Germany), Vartika Verma (Technical University of Munich, Germany), and Ralf Brederlow (Technical University of Munich, Munich, Germany), and Ralf Brederlow (Technical University of Munich,	mmWave/RF Packaging Applications	
Computing Systems N/A Chao-Yang Chiang (National Tsing Hua University, Taiwan), Po-Hsun He (National Tsing Hua University, Taiwan), Yu-Hsiang Chang (Advanced Semiconductor Engineering, Inc., Taiwan), Hung-Hsien Huang (Advanced Semiconductor Engineering, Inc., Taiwan), Chen-Chao Wang (Advanced Semiconductor Engineering, Inc., Taiwan), Chih-Pin Hung (Advanced Semiconductor Engineering, Inc., Taiwan), and Chien-Neng Liao (National Tsing Hua University, Taiwan) Measurement of Thermal, Humidity, Solder and Aging Effects of Mechanical Stress and Silicon Circuit Electrical Performance in Quad Flat Packages 2325 Carl Riehm (Technical University of Munich, Germany), Tobias Chlan (Technical University of Munich, Germany), Szabolcs Molnar (Technical University of Munich, Germany), Vartika Verma (Technical University of Munich, Germany), and Ralf Brederlow (Technical University of Munich,	2313 Yun-Hsuan Chen (National Yang Ming Chiao Tung University (NYCU), Taiwan), Guan-Zhe You (National Tsing Hua University (NTHU), Taiwan), Pin-Syuan He (National Yang Ming Chiao Tung University (NYCU), Taiwan), Yi-Chen Chung (National Yang Ming Chiao Tung University (NYCU), Taiwan), Rou-Jun Lee (National Yang Ming Chiao Tung University (NYCU), Taiwan), Chien-Yu Liu (National Yang Ming Chiao Tung University (NYCU), Taiwan), Chang-Chun Lee (National Tsing Hua University (NTHU), Taiwan), and Chih Chen (National Yang Ming Chiao	gy
Silicon Circuit Electrical Performance in Quad Flat Packages	Computing Systems	
	Measurement of Thermal, Humidity, Solder and Aging Effects of Mechanical Stress and Silicon Circuit Electrical Performance in Quad Flat Packages	2325

Author Index