

# **2025 IEEE Nordic Circuits and Systems Conference (NorCAS 2025)**

**Riga, Latvia  
28-29 October 2025**



**IEEE Catalog Number: CFP25828-POD  
ISBN: 979-8-3315-1502-7**

**Copyright © 2025 by the Institute of Electrical and Electronics Engineers, Inc.  
All Rights Reserved**

*Copyright and Reprint Permissions:* Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

***\*\*\* This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP25828-POD
ISBN (Print-On-Demand):	979-8-3315-1502-7
ISBN (Online):	979-8-3315-1501-0

**Additional Copies of This Publication Are Available From:**

Curran Associates, Inc  
57 Morehouse Lane  
Red Hook, NY 12571 USA  
Phone: (845) 758-0400  
Fax: (845) 758-2633  
E-mail: [curran@proceedings.com](mailto:curran@proceedings.com)  
Web: [www.proceedings.com](http://www.proceedings.com)

CURRAN ASSOCIATES INC.  
**proceedings**  
.com

## TABLE OF CONTENTS

Hardware Accelerated Synthetic X-Ray Medical Image Generation Using HBM-Based FPGAs .....	1
<i>Sam Aanhane, Per Knops, Rob De Jong, Casper Cromjongh, Zaid Al-Ars</i>	
Efficient Prompt Design for Resource-Constrained Deployment of Local LLMs .....	8
<i>Aisvarya Adeseye, Jouni Isoaho, Seppo Virtanen, Mohammad Tahir</i>	
A Power-Efficient Analog Integrated Neural Network for Multiple Sclerosis Disease Detection .....	15
<i>Vassilis Alimisis, Konstantinos Cheliotis, Vasileios Moustakas, Anna Mylona, Andreas Papathanasiou, Paul P. Sotiriadis</i>	
HyPPA: PPA-Aware Hierarchical RTL Generation and Evaluation of RISC-V Cores Using Hyperparameter Tuning .....	22
<i>Mohamed Badawy, Jiulong Wang, Vijaydeep Yadav, Nguyen Anh Vu Doan, Paritosh Kumar Sinha, Wolfgang Ecker</i>	
Towards Achieving Vertical Reuse in SoC-Level Verification .....	29
<i>Petr Bardonek, Alessandra Dolmeta, Marcela Zachariášová, Guido Masera</i>	
Time-Resolved Single-Photon Counting IC for Raman Imaging .....	36
<i>Leeladhar Bodu, Tuomo Talala, Jan Nissinen, Ilkka Nissinen</i>	
ChiselTrace: Typed Behavioral Debugging in Chisel Through Signal Dependency Tracing .....	43
<i>Jarl Brand, Casper Cromjongh, H. Peter Hofstee, Zaid Al-Ars</i>	
A Novel Layout-Circuit Co-Design Framework for Radiation Hardening in Nanoscale Technology .....	50
<i>Aobo Cui, Eleonora Vacca, Luca Sterpone, Sarah Azimi</i>	
A 4-W Ka-Band High-Efficiency 0.15 $\mu\text{m}$ GaAs Stacked Power Amplifier Design .....	57
<i>Mehmet Batuhan Dinç, Mustafa Berke Yelten</i>	
All About Nothing: Towards Zero-Cost Hardware Accelerated RISC-V Interrupt Handling in Rust .....	61
<i>Pawel Dzialo, Per Lindgren</i>	
Thoth: Rust-Driven Firmware and HDL Co-Design for Trusted IoT/UAV Systems .....	67
<i>Mohamed El-Hadedy, Wen-Mei Hwu</i>	
FPGA Acceleration of Convolutional Neural Networks at the Edge: A Comparative Study on High-Level Synthesis Frameworks .....	74
<i>João Rodrigo Faria, Fábio D. L. Coutinho, Arnaldo S. R. Oliveira</i>	
A Robust 90-NW Power-On Reset Circuit with Brown-Out Detection for RF Energy-Harvesting .....	80
<i>Patrick Fath, Harald Pretl</i>	
A 0.9 V StrongARM Latch Comparator with 16 Ps Delay and 7.5 fJ/op in 16 Nm FinFET CMOS Technology .....	85
<i>Rafael Ferreira, Boyapati Subrahmanyam, Bandi Chenchu Punna Rao, Miguel Coelho, Rafael Martins, Alexandra Matos, Pedro Toledo, Luis B. Oliveira, José Soares Augusto, João P. Oliveira</i>	
Accurate Analysis of Switching Transients in the High-Frequency, Integrated Dual-Path Step-Down DC-DC Converter .....	92
<i>Domenico Frassetto, Stefano Cabizza, Asif Karim, Giorgio Spiazzi, Andrea Bevilacqua, Andrea Neviani</i>	

4T Bitcell for Digital Compute-In-Memory .....	99
<i>Florian Freye, Christian Lanius, Nils Mutert, Tobias Gemmeke</i>	
KRS Unleashed: Towards a Robotics FPGA Development Environment for Rapid Prototyping .....	106
<i>Paul Gottschaldt, Diana Goehringer</i>	
Improving AI Accelerator Performance Through Co-Designing Neural Networks and Systolic HW .....	113
<i>Annina Gutermann, Alexey Serdyuk, Foivos Paraskevas, Hella Toto Kiesa, Fabian Lesniak, Jakob Schwarz, Michael Hartmann, Tanja Harbaum, Juergen Becker</i>	
A (145, 128) DEC-TED BCH Decoder with Composite Field and Redundant Arithmetic .....	120
<i>Hossein Hashemi Shadmehri, Christian Lanius, Tobias Gemmeke</i>	
Integrated Electroforming of Memristor Cells in Crossbar Arrays.....	127
<i>Ricardo Heinen, Jonas Zoche, Ralf Wunderlich, Stefan Heinen</i>	
A Robust, Fully Integrated 30.5-33.2 GHz and 34.3-36.8 GHz Frequency Synthesizer in SiGe-BiCMOS for Space Applications.....	133
<i>Frank Herzel, Seyyid Dilek, Jakub Jablonski, Falk Korndörfer, Corrado Carta, Gunter Fischer</i>	
Delay-Switching Oscillator and Switching-Mode Power Amplifier in 65 Nm CMOS for Isolation Crossing SWIPT .....	140
<i>Lukas Hüssen, Muh-Dey Wei, Renato Negra</i>	
A 22nm Coarse-Grained Reconfigurable Array with Novel Features for Machine Learning and Digital Signal Processing .....	145
<i>Waqar Hussain, Alexandra Geciova, Ralf Hekmann, Henry Hoffmann, Zohaib Hassan, Jari Nurmi</i>	
A 50 Gbps Reference-Less NRZ Full-Rate Bang-Bang CDR with Automatic Frequency Acquisition in 130nm SiGe:C BiCMOS Technology .....	152
<i>Mohammed Iftekhhar, Babak Sadiye, Wolfgang Mueller, J. Christoph Scheytt</i>	
The PAE Cell: A Novel Multiple Outputs Logic Cell and Technology Mapping for eFPGA .....	159
<i>Ryo Iwasaki, Kenshu Seto, Masahiro Iida</i>	
Matrix-Vectorized Canonical Signed Digit Quantized Neural Networks for Efficient Forward Pass Simulation .....	166
<i>Maria Khan, Jari Nurmi</i>	
Lightweight Multicast Interconnect for Time-Predictable Data Streams in MPSoCs .....	171
<i>Maximilian Kirschner, Henrik Scheidt, Jürgen Becker</i>	
Design and Experimental Verification of a 0.14-0.55V 1.9-24.2pW 22nm 3-bit Binary Search Supply-to-Digital Converter Using One-Hot Hard-Wired Topology and Supply-Dependent-Activation Buffers for Supply Sensing IoT Systems .....	178
<i>Hiroaki Kitaike, Hironori Tagawa, Kento Okamura, Wu You, Kei Awano, Jin Nakamura, Masaya Kaneko, Yuta Kimura, Hiroaki Nakamura, Shufan Xu, Kunyang Liu, Hirofumi Shinohara, Kiichi Niitsu</i>	
Optimizing Embedded Software Platforms Development: A Multi-Stage MDA-Driven Approach to Firmware Generation for Multiple Programming Languages .....	184
<i>Raphael Kunz, Lijun Chen, Stephanie Ecker, Yash Ranjan, Paritosh Kumar Sinha, Wolfgang Ecker</i>	

Model-Driven Generation of Executable Models for Hardware Specification Validation .....	190
<i>Robert Kunzelmann, Raymund Tonyka, Vinod Bangalore Ganesh, Raphael Kunz, Stephanie Ecker, Wolfgang Ecker</i>	
System Level Acceleration of Banded Smith Waterman on FPGA.....	197
<i>Christian Lanius, Ibrahim Burak Yorulmaz, Tobias Gemmeke</i>	
Systematic Design of a PVT-Robust CMOS Time-Based-Controlled DC-DC Converter Using Open-Source Tools .....	204
<i>Jorge Marin, Vicente Osorio, Andrés Martínez, Daniel Arévalos, Krzysztof Herman, Juan Pablo Martínez Brito, Christian A. Rojas</i>	
Grading Defects: Evaluating Approximate Circuits for Error-Tolerant Systems .....	210
<i>Gianluca Martino, Alberto Garcia-Ortiz, Lutz Schammer, Goerschwin Fey</i>	
300 mV-VD D, nw-Power, ST-DIGOTA Using I/O Devices in FinFET Technology.....	217
<i>Alexandra Matos, Ricardo Machado, Pedro Toledo, Miguel Coelho, Rafael Ferreira, Rafael Martins, Boyapati Subrahmanyam, João P. Oliveira, Luis B. Oliveira, José Soares Augusto</i>	
Automatic Verification of Analog and Mixed-Signal Neural Network Accelerators and Matrix Multipliers .....	223
<i>Roland Müller, Bijoy Kundu, Jan Maximilian Vieregge, Yogesh Patil, Ralf Brederlow</i>	
Rust for Safety and Security Critical Systems.....	230
<i>Malte Munch, Marcus Lindner, Johan Eriksson, Pawel Dzialo, Per Lindgren</i>	
ATAS-HM: Adaptive Task Allocation for Real-Time Tasks on Heterogeneous Multicore Systems .....	237
<i>Arthur Nathaniel Mwang'Onda, Diana Goehringer</i>	
Performance Evaluation of MAGIC-ReRAM Arithmetic Circuits for Low-Latency In-Memory Computing.....	244
<i>Saeideh Nabipour, Fatemeh Shirinzadeh, Kamalika Datta, Abhoy Kole, Saeideh Shirinzadeh, Rolf Drechsler</i>	
Exploiting Multi-VT FDSOI Technology for Improved Area and Energy Trade-Offs for Ultra-Low Voltage Schmitt Triggers .....	251
<i>Louisa Charlotte Nägle, Snorre Aunet, Ulrich Rückert</i>	
Towards Predictable Ultra-Low Latency End-Nodes with Hardware-Accelerated Abstract Timers.....	258
<i>Antti Nurmi, Henri Lunnikivi, Per Lindgren, Timo D. Hämäläinen</i>	
An Adaptive and Secure Resource Management Architecture for Virtualized FPGAs .....	264
<i>Zuwen Ou, Lu Jiang, Lester Kalms, Diana Göhringer</i>	
An Ultra-Low Power Bandpass Filter Bank with Input and Output Common-Mode Feedback in FD-SOI .....	271
<i>Damian Panter, Gabriel Lías Villar, Erkan Nevzat Isa, Amelie Hagelauer</i>	
Thermal-EXAMINER: IP Extraction from MAGIC Logic-in-Memory Using Thermal Side-Channel Attacks.....	277
<i>L. Pfeifer, A. Weiler, J. S. Haas, R. Leupers, J. M. Joseph</i>	
A Low-Power and High-Precision Winner-Take-All Circuit for Low-Voltage Applications .....	284
<i>Fahimeh Rahimi, Mehdi Saberi, Alexandre Schmid</i>	
Near-Threshold Voltage Massive MIMO Computing .....	289
<i>Mikael Rinkinen, Mehdi Safarpour, Shahriar Shahabuddin, Olli Silvén, Lauri Koskinen</i>	

Fault-Tolerant Character Recognition in Neuromorphic Systems Using RRAM Crossbar Arrays .....	296
<i>Fatemeh Shirinzadeh, Abhoy Kole, Kamalika Datta, Saeideh Shirinzadeh, Rolf Drechsler</i>	
Small Packets, Big Challenges: Enhancing Reliability in High-Speed, Low-Latency Inter-FPGA Communication .....	303
<i>Vida Sobhani, Jialan Zheng, Tobias Gemmeke</i>	
Implementation of Drive Signal in DC-DC Converters for Chaos Synchronization.....	310
<i>Daniils Surmacs, Sergejs Tjukovs, Romans Kusunins, Kristaps Gailis, Dmitrijs Pikulins</i>	
Novel Verification IP (VIP) for AXI4 Interconnects Employing Universal Verification Methodology (UVM).....	314
<i>Petri Sydänmaa, Jaisal Ashraf, Syed Mohsin Abbas</i>	
Automatic Reference Clock Duty Cycle Calibration System for Dual Edge Sampling RF Circuits.....	320
<i>Miikka Tenhunen, Veeti Lahtinen, Marko Kosunen</i>	
A Hierarchical Approach to Health Management in Heterogeneous Embedded Systems.....	325
<i>Anton Tsertov, Konstantin Shibin, Sergei Devadze, Artur Jutman</i>	
Implementation Study of a Noise Cancellation Filter for a 0–3 MASH Delta-Sigma-ADC .....	332
<i>Jonathan Ungethüm, Nicolas Graber, Simon Wilhelmstätter, John G. Kauffman, Maurits Ortmanns</i>	
GenIE: Reuse-Oriented Generation of Domain-Specific Instruction Extensions.....	338
<i>Philipp Van Kempen, Andreas Hager-Chukas, Daniel Mueller-Gritschneider, Ulf Schlichtmann</i>	
Simopt-Power: Leveraging Simulation Metadata for Low-Power Design Synthesis.....	345
<i>Eashan Wadhwa, Shanker Shreejith</i>	
Evaluating Rapid Makespan Predictions for Heterogeneous Systems with Programmable Logic.....	351
<i>Martin Wilhelm, Franz Freitag, Max Tzschoppe, Thilo Pionteck</i>	
A 1.4-V 260-pW 1-mm <sup>2</sup> 65-nm CMOS Temperature/pH Sensing IC Featuring Voltage-Stacking Timer and Wireless Transmitter for Stomach-Acid-Charged Tablet-Type Digital Pills with Long- Term In-Body Monitoring .....	358
<i>You Wu, Kei Awano, Ikuro Yamane, Hiroaki Kitaike, Masaya Kaneko, Hisataka Maruyama, Hiroshi Miyaguchi, Shinya Yoshida, Takumi Kobayashi, Daisuke Anzai, Takeshi Fujiyabu, Natsuko Inagaki, Kenji Takeda, Toshiro Yamanaka, Taichi Ito, Hiroki Kawashima, Mitsuhiro Fujishiro, Fumihito Arai, Koji Ohnishi, Kiichi Niitsu</i>	
A 28-GHz Monostatic OFDM-based ISAC System on RFSoc with Real-time Processing .....	365
<i>Yizheng Wu, Arif Rahmadian Arifianto, Vishnu Unnikrishnan, Anteneh A. Gebremariam, Liang Liu</i>	
A Foreground Calibration Scheme for Comparator Offsets in Loop-Unrolled SAR ADCs.....	372
<i>Shaobai Xing, Pietro Andreani, Wenbo Li</i>	
Exploration of Short Floating-Point Numbers for Hardware-Friendly Digital Predistortion .....	378
<i>Ziyi Yu, Mubanda Talemwa, Per Larsson-Edefors</i>	
Memristor Differential Pair Ternary Weight Neural (TWN) Network Architecture.....	383
<i>Yi Zhu, Dinesh Pamunuwa, Roshan Weerasekera</i>	
A 8.9 $\mu$ W 12.3-ENOB SAR ADC with <1 LSB DNL/INL for Electrochemical Impedance Spectroscopy in 12nm CMOS .....	389
<i>Christian Ziegler, Alexander Meyer, Fa Foster Dai, Liubov Bakhchova, Vadim Issakov</i>	

## Author Index