

2025 10th International Conference on Integrated Circuits and Microsystems (ICICM 2025)

**Hefei, China
17-19 October 2025**

Pages 1–495

IEEE Catalog Number: CFP25H23-POD
ISBN: 979-8-3315-8850-2



Copyright © 2025, IEEE

All Rights Reserved

Copyright and Reprint Permissions:

Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

*** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.

IEEE Catalog Number:	CFP25H23-POD
ISBN (Print-On-Demand):	979-8-3315-8850-2
ISBN (Online):	979-8-3315-8849-6

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA

Phone:	(845) 758-0400
Fax:	(845) 758-2633
E-mail:	curran@proceedings.com
Web:	www.proceedings.com

TABLE OF CONTENTS

A Compensation-Capacitor-Based Perturbation Injection Calibration Method for SAR ADCs	1
<i>Hongjian Ren, Ke Hu, Wenya Luo, Chao Cao, Haijun Guo</i>	
Design and Simulation of High-Frequency FBAR Based on Multiphysics and MBVD Circuit Modeling	7
<i>Rui Zhao, Jiangbo Wei, Yang Xiao, Liaoliao Zhang, Haijuan Li, Jiaqi Liu, Chao Wang</i>	
A 10GS/s 8b Time-Interleaved ADC with Aperture Error Calibration and LMS-Based Nonlinearity Correction	12
<i>Chuan Qin, Chuan Liu, Runqiao Wang, Lecheng Li, Maliang Liu, Yintang Yang</i>	
VCIL: An Open-Source Pipeline-Tight HIL Framework for Cycle-Accurate RISC-V Coprocessor Verification	19
<i>Xian Lin, Xin Zheng, Zhixin Fan, Huaian Gao, Shuting Cai, Xiaoming Xiong</i>	
An Electrode Impedance Evaluation IC with Biphasic Output Current for Biomedical Devices	25
<i>Fang Xie, Yu Ang Ru, Zhuo Chen, Xu Liu</i>	
A Fast Transient and High PSRR LDO with 62 ns Settling Time	31
<i>Ruijie Wang, Zhiguo Yu, Xiaofeng Gu</i>	
Automatic Generation Method of Test Vectors for FPGA Interconnect Resources Based on Self-adaptive Ford-Fulkerson Algorithm	37
<i>Liang Zhou, Wei Zhou, Mingzhe Li, Kun Guo, Ding Zhang, Yan Huang</i>	
A Multi-Phase Clock Generator with Customized Duty Cycles for Pipeline-SAR ADCs	43
<i>He Zhi, Hongtao Yue, Yuwei Zong, Zhongxu Zhang, Jianhui Wu, Xin Li</i>	
Hardware Design and Side-Channel Security Analysis on the Key Computational Block for YOLOv11	49
<i>Runquan Shao, Liji Wu, Jing Hu, Le Wu, Xiangmin Zhang</i>	
Secondary-Side Controlled Flyback Converter with Buck-Bypass for Multi-Port Application	54
<i>Zhen Wang, Yi Liu</i>	
Research on the Method of Switching Adjustment to Reduce the Temperature Drift of the Bandgap Reference	60
<i>Bin Wen, Zhongjie Guo, Hongpeng Dai, Xiaoqing Qiang</i>	
Design and Implementation of a Secure Boot RISC-V Processor for IoT Devices	65
<i>Zeyu Li, Liji Wu, Jing Hu, Han Sun, Xiangmin Zhang, Haijie Wang</i>	
A 1GS/s 13-bit Single-Channel Hybrid Pipelined SAR ADC with Domino SAR Logic	71
<i>Chuan Liu, Chuan Qin, Lecheng Li, Zhihao Hou, Yuqi Fan, Maliang Liu</i>	
A 1.7-to-3.0 GHz 201.95 dBc/Hz FOMT VCO With a Current-Reuse Active Inductor	76
<i>Xinyi Zhang, Wanqing Wu, Guoxun Dai, Jiangnan Li, Haigang Feng</i>	
A 24-28GHz GaN SPDT MMIC with High Isolation and Low Insertion Loss	81
<i>Peiyao Liu, Pengfei Jiang, Kui Dang, Rujun Sun, Yue Hao, Jincheng Zhang</i>	
Design and FPGA Implementation of a NTT Hardware Accelerator for PQC ML-DSA	86
<i>Shuhang Zhu, Liji Wu, Lei Li, Yifan Yang, Xiangmin Zhang</i>	

The Effective Resistance Calculation Method Based on Matrix Partitioning Takahashi Algorithm	92
<i>Meng Li, Yu Chen, Jingrui Chen, Yaokai Zhang, Jinyu Zhang, Xiaolue Lai</i>	
Hardware Design for Decomposition Module with Variable-Order Masking against Side-Channel Attack for PQC ML-DSA	99
<i>Xuejian Wang, Liji Wu, Lei Li, Yifan Yang, Xiangmin Zhang</i>	
Design and Implementation of a High-Reliability MIPI Interface Error Detection and Correction System for CMOS Image Sensors	105
<i>Qiang Zhao, Jianwei Feng, Bin Qiang, Zhigang Li, Xin Li, Chunyu Peng, Xiulong Wu</i>	
Temperature Sensing Module Design for Silicon MEMS Clocks	110
<i>Shaotian Fan, Lu Tang, Yuxing Gu</i>	
An End-to-End Compact Shape-Aware Macro Placer Using Reinforcement Learning	115
<i>Hailiang Li, Xiao Wang, Xu Yang, Miaohui Hao, Yan Huo, Beiping Yan</i>	
A 2.4 GHz Wide-Tuning-Range Low-Phase-Noise Differential Digitally Controlled Ring Oscillator for CMOS Image Sensor Applications	122
<i>Zhigang Li, Hongjia Xu, Yao Nian, Jingyi Wang, Xin Li, Qiang Zhao, Xiulong Wu</i>	
Smart Wireless Insole with Self-Powered Triboelectric Pressure Sensors for Gait Detection	127
<i>Yuhan Wang, Yue Yao, Enze Li, Sifan Liang, Lei Li</i>	
Voltage-Time Hybrid Domain ADC with PVT Tracking for High-Frame-Rate CMOS Image Sensor	132
<i>Xin Li, Ziheng Wang, Bin Qiang, Chunyu Peng, Qiang Zhao, Xiulong Wu</i>	
A Very-Large-Dynamic-Range Charge-Sensitive Front End for One-Terminal Capacitive Sensors in 65-nm CMOS	138
<i>Haitao Fan, Wenxiang Li, Jiafeng Yang</i>	
A fast transient-response LDO-CP with novel high voltage compensation structure in CMOS image sensors	143
<i>Qiang Zhao, Zhendong Niu, Zhigang Li, Xiuying Wang, Chunyu Peng, Xiulong Wu</i>	
A 13-bit 1.5-GS/s Dual-Residue Pipelined ADC with Time-Domain Interpolation and Parallel Quantization	148
<i>Zecheng Zhou, Depan Li, Longsheng Wang, Ting Li, Dongbing Fu, Dengquan Li</i>	
A Novel Self-adaptive Dead-time Control Circuit Design for GaN Gate Drive Circuit	153
<i>Shupeng Yan, Shengqi Yu, Yi Huang, Junjie Yi, Pengyu Wang</i>	
A Novel Hybrid Switching Scheme for SAR ADC with High Efficiency and High Linearity	158
<i>Yushi Chen, Ying Li, Fang Liang, Zewen Wang, Zuoru Dong, Xiaodong Wang</i>	
A Unified Swin Transformer Framework for Inverse Lithography and Lithography Simulation	163
<i>Jiajun Tan, Ling Liang, Ming Zhu</i>	
Design of 6-to-8-bit High-Speed Time-Interleaved SAR ADC	168
<i>Zhenyang Zhang, Fangxu Lv, Zhengbin Pang, Jiaqing Xu, Qiang Wang, Meng Li</i>	
RLMBFF: Multi-bit Flip-Flops Merging using Deep Reinforcement Learning	173
<i>Zeqi Chen, Zhaori Bi, Changhao Yan, Ming Zhu, Xiulong Wu, Xuan Zeng</i>	

HybridSYN: An Efficient Logic Synthesis Methodology	180
<i>Ke Wang, Yue Wu, Xiaoyan Yang</i>	
A 20-GHz Low-Jitter Fractional-N CP-PLL With 2.5-GHz FBAR Reference	186
<i>Jiandu Wang, Jiwei Huang, Yi Sun</i>	
A 14-Bit SAR ADC with Area-Efficiency Hybrid Three-Segment CDAC	191
<i>Chengchen Song, Jia Yu, Chao Cao, Hongjian Ren, Yuchan Duan, Haijun Guo</i>	
A Fully Reversible Feynman Gate with Magic Block for Quantum-dot Cellular Automata Circuits	198
<i>Jiayi Zhang, Feifei Deng, Xianghui Li, Yuezhong Xiong, Yunong Zhao, Xiaohui Guo</i>	
A Wide-Temperature-Range Low-Drift Bandgap Reference with Process-Corner-Adaptive Logic Current Compensation	204
<i>Xuesong Chen, Yu Jin, Ning Fu, Weifeng Li, Duli Yu</i>	
A Pixel-to-Column Digital Readout Circuit with InPixel CDS for Ga ₂ O ₃ UV Photodetectors	209
<i>Jiekun Zhang, Guangfen Wei, Jingwu Gong, Yu Zhou, Xiaodong Zhang, Helun Song</i>	
A DDR Controller Circuit Gate-level Post-simulation Method in SoC Design	215
<i>Yande Jiang, Jingbo Ma, Guangda Zhang, Huiquan Wang, Bingxi Pei, Na Chen, Jian Fang</i>	
A High-Precision Current Detection Circuit for Battery Management System Chip in Electric Vehicle	221
<i>Zhiwei Li, Liji Wu, Dan Xie, Kunming Mao, Haifeng Chen, Zhilin Zhong</i>	
A Robust Startup Circuit for Current-Mode Bandgap Reference	226
<i>Qi Wang, Hao Li, Chunlei Pang</i>	
A Low-Power High-Accuracy Phase Frequency Detector and Charge Pump Design for CPPLL in 28 nm CMOS Technology	232
<i>Zhigang Li, Hao Lei, Zhihao Liu, Lingrui Yan, Qiang Zhao, Shan Gao, Xiulong Wu</i>	
A 60-V 96.7%-Efficiency 175kHz Integrated Dimmable LED Driver with Mean-Peak Current Control and Frequency Jittering Scheme	237
<i>Jiamian Mao, Zhongguang Xu, Xiangyin Chen</i>	
A 100-Gb/s PAM4 Receiver Analog Front-End	243
<i>Haoran Huang, Yue Xu, Jing Huang, Gengzhen Qi</i>	
A -86 dBm/15.6 μ W Wake-Up Receiver for Internet of Vehicles Applications	247
<i>Rui Chen, Yan Li, Liming Si, Xinchao Zhong, Chiu-Wing Sham, Hang Yu</i>	
A 28 – 32 Gb/s Wireline Receiver with A Genetic- Algorithm-Based Adaptive CTLE in 28 nm CMOS	252
<i>Yingjie Zhang, Fangxu Lv, Liangyong Yuan, Xiaoyue Hu, Ruixiao Kuai, Xianchao Zeng</i>	
A Wideband Blocker-Tolerant Receiver with High Linearity and Low 0 dBm-BNF in 65-nm CMOS	257
<i>Kaiyun Deng, Yingqi Liu, Qingrui Jiang, Kailin Liu, Shaohui Pan, Haigang Feng</i>	
A Model of a C-band Mixer Circuit	262
<i>Xuezhen Zhao, Jun Liu, Jing Wang, Guodong Su</i>	
Parametric Modeling of Transmission Structure of RF Microsystem Based on CNN-LSTM-SelfAttention	267
<i>Li Qin, De Xi Liu, Cui Jing, Lei Shi, Ya Wei Liu, Ting Xue</i>	

A Radio-Frequency Orthogonal Switched-Capacitor Transmitter	272
<i>Yingyi Chen, Mianting Hu, Sijia Zhao, Ruiyi He, Gengzhen Qi</i>	
Daisy Chain Transmitter Circuit Design with AntiElectromagnetic Interference for BMS Chip in EV	276
<i>Chen Lin, Liji Wu, Jing Hu, Zonghuan Wu, Xiangmin Zhang</i>	
A Low-Power Flip signal Pulse Width Self-Adaptive Circuit for Piezoelectric Energy Harvesting	282
<i>Hongtao Yue, Shuo Zhang, Haoyu Xue, He Zhi, Jianhui Wu, Xin Li</i>	
A Sub-nanosecond Delay and 200V/ns CMTI Level Shifter for GaN HEMTs Gate Driver	288
<i>Shengqi Yu, Pengyu Wang, Junjie Yi, Shupeng Yan, Yi Huang</i>	
A Wide Tuning Range Dual-Mode, Magnetical-Coupled VCO with Capacitive-Coupled Noise-Circulating Technique Achieving FoM of 188dBc/Hz	294
<i>Qishuang Liu, Chenxiang Cai, Yunchu Li</i>	
A Fractional-N All-Digital PLL with 166fs _{rms} Jitter and 238 dB FoM Based on a Distributed Switched-Capacitor Arrays DCO	299
<i>Zhihong Xu, Yuhui Li, Pei Qin, Changsong Lin, Jinhua Guo, Xiaorui Liu, Taotao Xu, Quan Xue</i>	
A CMOS Current-Reused Wideband Low-Power Dynamic Current Mode Logic Frequency Divider	305
<i>Jingchen Liu, Youming Zhang, Xusheng Tang, Zhennan Wei, Shenghao Meng</i>	
A VHF memristor emulator for crossbar synaptic simulation	309
<i>Guangzhen Dai, Bingchen Liu, Sihao Yang, Wei Li, Daohua Wu, Yuefeng He</i>	
A Novel SiC LDMOS with Electron Accumulation Layer Featuring Ultra-low Specific On-resistance and Improved Breakdown Voltage	317
<i>Moufu Kong, Lin Tong, Qizhi Feng, Jiaru Jia, Zhaoyu Ai, Hongfei Deng, Yangyang Ma, Peifei Wu</i>	
Hardware Implementation and Side-Channel Security Analysis for High-Precision AI Tansformer Encoder	322
<i>Wentao Wang, Liji Wu, Jing Hu, Le Wu, Xiangmin Zhang</i>	
High-Performance Data Prefetching Accelerator for Real-Time Object Detection	328
<i>Yanzhou Tang, Xiangyu Zhou, Zeyi Lin, Ming Cheng, Naifeng Jing, Jianfei Jiang, Weiguang Sheng Qin Wang</i>	
Design of High-reliability and High-dynamic Analog Front-end for DC Carrier Chip	333
<i>Quan Sun, Gang Chen, Changyou Men, Shuang Wu</i>	
A Steady-State Temperature Solving Method for Multi-Chip Modules Components Based on an Improved U-Net	338
<i>Fulong Yang, Feng Wu, Teng Zhang, Jinjin Zhou, Qing Yang</i>	
Open-LUT: Interactive g _m /ID Lookup Tables for MOSFET Sizing in Open-Source PDKs	344
<i>Sihawi A. Khalid, Susie E. Maestre, Karla M. Madrid-Khalid</i>	
A 9.37-Tb/s/mm 5-bit-6-bit Crosstalk Cancellation Transceiver with ICBS Codes for High-Density Die-to-Die Interfaces	354
<i>Ruotian Yin, Jinwen Li, Fangxu Lv, Geng Zhang, Ruixiao Kuai, Bohui Bai</i>	
Design and Implementation of an Integrated Testing System for Spintronic Chips	360
<i>Wenyan Liu, Zihan Gao, Zhifu Guo, Zefan Wu, Xiangrong Pu, Xu Liu, Zhang Zhang</i>	

Design of a Reusable UVM Verification Framework for Pixel Readout Chips	366
<i>Yu Zhao, Zexuan Zhao, Yuanhong Jiao, Xiaomin Wei, Heng Yang, Long Liu, Yongcai Hu</i>	
Design of High Gain and High Power Amplifier chip Based on RF Choke Segmented Multiplexing Interstage Matching Technology	372
<i>Zhenbing Li, Weijun Li, Haoyang Sun, Jiaxin Liu, Jialong Fu, Yaocheng Shang</i>	
Research on SoC Chip System Modeling for Noise Suppression and Self-organizing Communication Integration for Distributed Photovoltaics	378
<i>Quan Sun, Gang Chen, Changyou Men, Shuang Wu</i>	
Topology Evaluation-Based Layer Assignment Method for Free-assignment Routing in InFO Packages	384
<i>Zhan-Yang Zhu, Ning Xu, Hao-Ying Wu, Chenglin Lu</i>	
A Radiation Tolerant CMOS Voltage Reference Circuit for High Energy Physics Experiments	391
<i>Wei Ming Yang, Jia Wang, Xiayu Wang, Ran Zheng, Xiaomin Wei, Yongcai Hu</i>	
Dynamic Reward Weighting Based Deep Q-Learning for Routing in Advanced Packaging	397
<i>Shubin Chen, Qinghai Liu, Xiaowei Wu, Jun Xu, Xiaolin Xu</i>	
A 7-Bit 1.8 ps Two-Step Time-to-Digital Converter in 28 nm CMOS Technology	403
<i>Zhigang Li, Yao Nian, Hongjia Xu, Wei Liu, Xin Li, Qiang Zhao, Xiulong Wu</i>	
Ka-Band Broadband LNA in 65-nm CMOS Using Pre-stage Current-reuse Technique and Large-size Transistor	408
<i>Zihan Yang, Hao Wang, Ye Liu, Tongde Huang, Wen Wu</i>	
A 0.4 to 8GHz Broadband High-linearity I/Q Active Mixer in 130nm BiCMOS Technology	413
<i>Qipeng Li, Zhenghao He, Chun Zhu, Yifan Huang, Qin Li</i>	
A Compact Active Phase Shifter for 110-150 GHz Phased Arrays in 130 nm BiCMOS	418
<i>Shuguang Liu, Jinhao Zhou, Yuyang Liu, Hu Lian, Yaxin Zhang, Ziqiang Yang</i>	
Interface Quality Improvement in Planar SiC MOSFETs Using Supercritical Fluid Nitriding	422
<i>Xiaoqing Bao, Lei Li, Lei Lu, Kuan-Chang Chang</i>	
Design of a Bandgap Voltage Reference for an 8-bit SAR-ADC for Powerline Monitoring using SKY130 PDK	427
<i>Krisna M. Cañonero, Jovelyn S. Bernales, Abdulwarith G. Macapundag, Sihawi A. Khalid, Susie E. Maestre</i>	
A 2.9mV _{pp} Ripple 60mA Digital Low-Dropout Regulator in 28nm CMOS	433
<i>Wenxin Zhang, Yuhang Zhang, Yang Shen, Xiaojin Li, Bingyi Ye, Yabin Sun</i>	
MOSFET Modeling of 0.18 μm CMOS Technology Based on BSIM4 Model for Cryogenic Devices	439
<i>Dong Chen, Zuoru Dong, Yushi Chen, Xingyu Cui, Fang Liang, Xiaodong Wang</i>	
Process Integration Optimization for RF SOI Process with Arcing Issue	445
<i>Zhangli Liu, Fei Meng, Ruofan Dai</i>	
An Optimized ROM based Direct Digital Synthesizer Based on 65nm CMOS Technology	449
<i>Yuan Yuan, Qingsheng Hu, Xu Wu, Li Anming Li</i>	
Integrated Circuit Design of CMOS Deadtime Controller for 48 V GaN DC-DC Converter	454
<i>Haoyu Chen, Miao Cui</i>	

An Ultra-Low Power Digital Assisted Self-Tracking Zero-Current Detector for DC-DC Converters	459
<i>Chuting Yang, Xing Li</i>	
A High-Linearity Digital-to-Time Converter Design for Fractional-N Sub-sampling PLL	464
<i>Jiangnan Li, Wangqing Wu, Ke Cao, Xinyi Zhang, Haigang Feng</i>	
A 24–27-GHz 3-Stage Driving Amplifier with 18–25dB Variable Gain in 180-nm CMOS for Beamforming ICs	469
<i>Zhenghuan Wei, Kaibo Zhang, Lijuan Wang, Sanming Hu</i>	
A 16-b 8-MS/s Pipelined SAR ADC With Robust Ring Amplifier and On-Chip Bit-Weight Calibration	474
<i>Shaojuan Chen, Xiaoyi Li, Xuanhao Zhang, Xingshuai Zou, Zhenbing Li, Jiaxin Liu</i>	
An IVUS AFE with LNA and a CT $\Delta\Sigma$ modulator with 80MHz BW and 12 bit ENOB	480
<i>Jie Peng, Yunchu Li</i>	
A Neuron-and-Synapse Unit Circuit with Information Propagation Function for Spiking Neural Networks	486
<i>Yide Zhang, Zixuan Ling, Zicheng Yin, Xu Liu</i>	
CMOS PWM Controller Design for GaN-Based 48V1 V DC-DC Buck Converter	491
<i>Guanyu Wu, Miao Cui</i>	
HEA ₂ -MAC: A Hybrid Exponent-Aware Approximate MAC for Efficient CNN Processing	496
<i>Weixuan Wang, Zihan Zou, Xin Cao, Xuefeng Cai, Hao Cai, Bo Liu</i>	
A Low-Power Continuous-Time Quadrature Bandpass $\Sigma\Delta$ ADC with a novel ELD Compensation Method in Quantizer	502
<i>Haowen Ba, Jun Ye, Hanli Liu, Feijun Zheng</i>	
Low Power $\Sigma\Delta$ Modulator Applied to CIS Column Parallel Readout Circuit	507
<i>Dengju Sun, Zhongjie Guo, Ruiming Xu, Jinqian Zhou</i>	
Design and Analysis of AC/DC Converter for GaNBased Server Power Supply System	512
<i>Fen Guo, Tuo Li, Changhong Wang, Kang Su, Jiankai Xu, Xin Xi, Kejian Zhu, Xinxin Yuan</i>	
A Low-noise PGA With High-gain Chopper Offset-stabilized Amplifier Combining Ping-Pong Auto-zero For TMR Analog Front-End	517
<i>Hui Wang, Guifa Yan, Mingqi Pan, Bo Wang, Jianhui Wu, Xin Li</i>	
An Adaptive dynamic R-tree indexing algorithm for HDI PCB layout	523
<i>Zhang Yang, Liang Xiaoyu, Ning Xu</i>	
A Novel Region-Wise Automatic Routing Algorithm for Analog Circuit	529
<i>Hao Xie, Wenxue Chen, Wei Zhang, Bijian Lan, Jing Wan</i>	
A 0.6-3 GHz Active Double-Balanced Mixer Circuit Design	535
<i>Jing Wang, Jun Liu, Xuezhen Zhao, Guodong Su</i>	
Replicated Partitioning for Hypergraphs with Multiple Constraints	540
<i>Kexin Zhang, Shunyang Bi, Jing Tang, Hailong You, Qiwan Chen</i>	
A cryogenic readout integrated circuit for blocked-impurity-band (BIB) far-infrared focal plane array detectors	546
<i>Yushi Chen, Xin Ge, Hongbo Ma, Zewen Wang, Zuoru Dong, Xiaodong Wang</i>	

1T1C-Enhanced TFT-Integrated Gate Driver Circuit Design for Reliable In-cell Touch Sensing Displays	551
<i>Congwei Liao, Yong Wang, Chao Teng, Yi Shen, Yudong Liu, Shengdong Zhang</i>	
Neural Network-Based Method for Magnetic Field Inversion of Energized Conductors in Printed Circuit Boards	556
<i>Qi Li, Yiling Liang, Zhen Liu, Lulu Tian</i>	
A double layer placement algorithm for IC-based modules of printed circuit board	561
<i>Hangyuan Li, Yu Chen, Zhaoyang Yang, Haotian Pang, Ning Xu</i>	
High-Performance Hydrogenated Oxide-Semiconductor Schottky Barrier Diodes with ALD HfO ₂ Interface	568
<i>Yucheng Cao, Chenyang Huang, Yuyang Cai, Kuan-Chang Chang, Lei Li, Congwei Liao, Yufeng Jin, Lei Lu</i>	
An Ultra-Low-Power True Random Number Generator Based on Volatile RRAM	573
<i>Qi Luo, Zhen Wang, Xueming Fan, Pengtao Li, Guobin Zhang, Yishu Zhang</i>	
Performance Evaluation of an Advanced-Node CMOS Sensor for Partial Detection	578
<i>Yue Su, Mingjie Feng, Zhiyu Xiang, Cheng Zeng, Congcong Wang, Hui Zhang</i>	
Low-power LDO with Fast Transient Response Based on FVF Structure	583
<i>Wenya Luo, Longfei Xu, Hongjian Ren, Chao Cao, Haijun Guo</i>	
Low-Power MCU Architecture Optimization and Energy Efficiency Enhancement in Intelligent Pressure Sensor SoCs	589
<i>Yaoming Lv, Hong Yang, Feng Zou, Yuhua Cheng</i>	
A Low-Phase-Noise and Low-Power Class-C VCO with Robust Start-up for FMCW Radars	594
<i>Zhigang Li, Zhihao Liu, Hao Lei, Hang Yang, Qiang Zhao, Shan Gao, Xiulong Wu</i>	
A 0.47 nJ/Conversion CMOS Temperature Sensor with 0.00786 mm ² Core in 65nm CMOS	599
<i>Hangfei Song, Yichi Zhang, Aili Wang</i>	
An Ultra-low Power 2× / 4× Reconfigurable Charge Pump for RF Energy Harvesting System	605
<i>Xuanchen Mei, Xin Liu, Junhui Ou, Yanqi Zheng, Mo Huang, Xiuyin Zhang</i>	
Cross-Process Bayesian Multi-Objective Collaborative Optimization For Process Migration	610
<i>Zixi Guo, Ruiyu Lyu, Zhaori Bi, Changhao Yan, Ming Zhu, Xiulong Wu, Xuan Zeng</i>	
Multi-Branch Autoencoder Networks for Efficient Inverse Design of Wideband Frequency-Selective Surfaces	616
<i>Wei Jiang, Haoran Huang, Guangxin Liao, Shenli Zheng, Jiacheng Guo, Yuan Du</i>	
GraphRL-Core: Intelligent Logic Synthesis Optimization via Graph Transformer and Deep Reinforcement Learning	622
<i>Sujie Zhu, Guande Dong, Haoyang He, Chong Xia, Jianwang Zhai</i>	
A Hilbert Transform-Based Timing Skew Estimation Method for Dual-Channel TIADCs	628
<i>Xin Li, Ying Pan, Mengdi Miao, Yu Liu, Chenghu Dai, Zhiting Lin</i>	
A Fast Auto-Frequency Calibration Technique with High Reference Frequency for PLL	633
<i>Yan Feng, Yongjie Ye, Guoxiao Cheng, Liu Wang, Wei Kang</i>	

Post-Routing Compression Algorithm for Area-Efficient Layout design of Analog Integrated Circuit	638
<i>Xiaoyue Wu, Yubo Zhang, Wei Zhang, Bijian Lan, Jing Wan</i>	
A Fractional-N Reference-Sampling PLL With a Gain-Boost Fractional Phase Detector for Phase Noise Reduction	643
<i>Xiaolian Xi, Lecheng Cai, Yihao Liu, Fan Liu, Yanlong Zhang</i>	
A 59.6GHz Broadband 3-stage Cascode LNA with Peak Detector for Bandwidth Self-healing	648
<i>Xinsheng Cheng, Jiacheng Guo, Juntao Liu, JingJing Lv, Yuan Du</i>	
Addressing Signal Integrity Challenges in DDR5 SDRAM: A High-Precision ZQ Calibration Circuit with Fast Calibration Time	653
<i>Kexin Feng, ZhiQiang Zhang</i>	
A Pipeline-Based Common Framework for Parallel Mixed Signal Simulation	660
<i>Longchen Sun, Guangrong Li, Zhenguo Zhao, Xin Huang, Xuan Zeng, Fan Yang, Zhao Ri Bi</i>	
A Rectifier Circuit with Adjustable Temperature Coefficient for Precise Amplitude Control of MEMS Resonator	665
<i>Guanxiao Zhang, Yang Zhao, Qin Shi, Guoming Xia, Anping Qiu, Meijia Xu</i>	
A Low-Complexity Bandwidth Enhancement Design Method for mm-Wave Doherty Amplifier	670
<i>Yujie Sheng, Fei You, Maojun Pan, Songbai He</i>	
A 10-bit 3-GS/s Single-Channel Pipelined ADC with Parallel Time-Domain Quantization Based on Dynamic Residue Amplifier	675
<i>Depan Li, Xin Zhao, Dengquan Li, Zhangming Zhu</i>	
Design of High Speed and Energy-Efficient ADC Based on Dynamic Bandwidth Ring Amplifier	681
<i>Xin Yang, Qingyuan Liu, Xiaobo Chen, Dan Sun, Bin Zheng, Tieliang Zhang, Long Yang</i>	
A 12-b 1-GS/s Pipelined-SAR ADC With a Hybrid Parallel Timing Scheme and PVT-Robust Ring-Amp	686
<i>Junhui Guo, Yunchu Li</i>	
An X-band Compact High-Efficiency MMIC Power Amplifier in 0.25- μ m GaN Technology	692
<i>Ye Liu, Anshi Zhu, Zihan Yang, Tongde Huang, Wen Wu</i>	
Design of a Two-Stage Fully Differential Operational Amplifier for High-Resolution Sigma Delta ADCs	697
<i>Zhan Shi, Zenghao Zhu, Yan Zhao, Franco Maloberti</i>	
Design of Power Amplifier for Short Message Application of BDS-III Communication Terminal	702
<i>Zhenbing Li, Weijun Li, Haoyang Sun, Jiaxin Li u, Jialong Fu, Yaocheng Shang</i>	
Design of a High-Bandwidth Low-Noise Amplifier	708
<i>Hongmei Chen, Ruiting Shen, Yuexin Tan, Zheyu Li</i>	
A Compact Wideband E-band Low Noise Amplifier with 3.3-4.5 dB Noise Figure using 45-nm RFSOI	716
<i>Yinhan Lin, Haoshen Zhu, Taotao Xu, Zhuming Li, Guohai Quan, Pei Qin, Quan Xue</i>	
A Wideband Input Buffer Based on AC-Coupled Flipped Source Follower Using Auxiliary Operational Amplifiers for 8-GS/s ADCs	721
<i>Yuhang Zhang, Jian Chen, Weiying Hu, Xianguo Kou, Changdong Guo, Haizhi Song</i>	

A 2.4-2.6 GHz CMOS High Linearity Power Amplifier with MGTR and Harmonic Trap Techniques	726
<i>Runxun Zhang, Gengzhen Qi</i>	
A Ka Band High Back-off PAE Power Amplifier with Adaptive Bias Circuits in 65 nm CMOS	731
<i>Ran Zhang, Xiaodong Zhao, Hangbiao Li</i>	
A DAC Design using 5-V High-voltage Process for Driving Large Electrode Loads of Neural Stimulators	737
<i>Xu Liu, YuAng Ru, Zhuo Chen, Fang Xie, Zhijie Chen, Peiyuan Wan</i>	
MEMS-Enabled Computational Spectrometer Based on Cascaded Waveguide Couplers	743
<i>Hanxing Wang, Yan Liu, Nan Wang, Yiming Ma</i>	
Control Strategy and Parameter Identification Method for Photovoltaic Inverter Electromechanical Transient Model Based on Improved Fish Eagle Optimization Algorithm	748
<i>Zecheng Li, Yaojia Huo, Kai Hou, Xiao Zhang, Hao Liu, Jinpeng Hao</i>	
Design of a Cross-Platform Simulation and Verification System for Complex Onboard Control Computers	753
<i>Zheng Yang, Shenglong Li, Chaofan Zhou</i>	
Fast Frequency Stabilization Technique for Buck Converter Based on Adaptive PLL	759
<i>Kerun Li, Mei Jiang, Jianing Guo, Yuxuan Guo</i>	
A Wide-Range PFD and Low-Mismatch Source-Switched CP for MEMS Clock Systems	764
<i>Changfu Wei, Lu Tang, Ziyao Xiong</i>	
High-Reliability Integration Design Method for Micro Systems SiP in Complex Spatial Environments	770
<i>Shang Jiang, Wenchang Li, Zucheng Gu, Tianyi Zhang</i>	
Design and Implementation of an FPGA-Based Test System for Depth of Interaction Measurement	780
<i>XiaoTian Lv, Ce Zhang, Ran Zheng, XiaoMin Wei, FeiFei Xue, RuiGuang Zhao, YongCai Hu</i>	
Design and Nonlinear Analysis of a Multi-Stepped MEMS Resonator with 1:3 Internal Resonance	785
<i>Peilong Li, Yu Jin</i>	
A 10.8-12.5-GHz Charge Pump PLL With 68.4-fs _{rms} Jitter and -252-dB FOMJ Based on a Time-Amplifying Phase-Frequency Detector	791
<i>Yuzhong Li, Zunfa Cheng, Jiwei Huang</i>	
A Stochastic Computing-Based Computing-in-Memory Macro with Bit-Split Stochastic Number Generation	796
<i>Zhiting Lin, Dandan Chen, Siyan Li, Shuang Liu, Yu Liu, Xiulong Wu</i>	
An Analytical Compact Model for Multi-time Programmable Memory Cells	801
<i>Tiantian Gan, Xiaojin Li, Tengyang Liu, Yabin Sun, Yanling Shi, Jianpeng Chu</i>	
A Hybrid Computing-in-Memory Architecture for Energy-Efficient Edge AI Inference	805
<i>Fangchao Lou, Dandan Chen, Jian Cao, Xing Zhang, Bo Zhang</i>	
A Reliable 512-kb HZO-based 2T2C FeRAM Array with Capacitor under Bitline	810
<i>Jing Wang, Xiangyin Chen, Zhongguang Xu</i>	
Reconfigurable SRAM Computing-In-Memory Macro Based on Local Computing Cell	814
<i>Chenghu Dai, Chaoyi Wang, Zeyi Liu, Qiang Zhao, Chunyu Peng</i>	

A 10T1C SRAM-Based Computing-in-Memory Unit Supporting Logic and MAC Computing for Energy- Efficient Edge AI Chips	819
<i>Zhiting Lin, Chenglong Duan, Miao Long, Juntao Ge, Fugui Jiang, Yang Yang, Xiulong Wu</i>	
OpenPIM: An Open-Source Programmable Processing-In-Memory Accelerator Design & Pipeline Simulation Framework	824
<i>Ruibao Wang, Wenshuo Yue, Daijing Shi, Yuchao Yang, Bonan Yan</i>	
CASA-CIM: A 28nm 131.54 TOPS/W SRAM-Based CIM Macro with Cap-Adder Weighting and Shift-After-Addition Data Streaming for Efficient MAC Operations	830
<i>Runru Yu, Chenyang Zhao, Honghu Yang, Zhiting Lin, Xiulong Wu, Keji Zhou, Jianguo Yang</i>	
Adaptive VREF variation Compensation Scheme for High-Speed DRAM interface & Its Offset Calibration Scheme	835
<i>Chris Eom, Kenji Wen, Mia Xu, Taco Zhang, Derek Yang, Bosco Lai</i>	
Stochastic Computation Based Quantization Strategy for SRAM Computing-in-Memory Macro	839
<i>Xin Li, Yifan Wu, Lintao Chen, Chenghu Dai, Xiulong Wu, Zhiting Lin</i>	
Design of a Multi-Dimensional and Multi-Precision Tensor Computation Unit Based on FPGA	844
<i>Yupeng Fang</i>	
A Low-Ripple Charge Pump with Adaptive Load Compensation for Flash-Based CIM	852
<i>Xuyuan Gu, Xiaofeng Gu, Zhiguo Yu</i>	
Interface-Engineered TiO ₂ /SiO ₂ Stacks Enable Ultralow-Power Phase-Change Memory with Nanosecond-Speed	858
<i>Ruizhe Zhao, Jun Zhou, Jun Chen, Hao Tong, Xiangshui Miao</i>	
Hafnium-Based Ferroelectric Diode with Interlayer Enhancement for In-Memory Logic Application	863
<i>Shuo Han, Chuanzhi Liu, Qimiao Zeng, Yefan Zhang, Wei Wang, Rongrong Cao</i>	
Reconfigurable Memory Device based on Defect Engineering of 2D Ferroelectric CuInP ₂ S ₆	868
<i>Yunpeng Xia, Yu Li, Tianqi Li, Qinfei Long, Zihui Hong, Yunhe Hou, Tiande Mo</i>	
ANDQ-NAT: Adaptive Non-linearity Dynamic Quantization Non-Ideality Aware Training Framework for Computing-In-Memory Macros	873
<i>Yu Liu, Jianxing Zhou, Hao Li, Yang Lou, Xiulong Wu, Zhiting Lin</i>	
A Fast-Transient-Response Hybrid Architecture LDO for NFC Reader SoC	879
<i>Xindong Mi, JinBiao Zhong, YuXuan Huang, JianGuo Hu</i>	
Design of an ATD Circuit for Asynchronous SRAM	885
<i>Jialin Liu, Rongkang Ren, Xin Li, Jiancheng Li, Qichao Zha</i>	
An Ultra-Wideband Compact Power Divider for Phased Array Radar Systems	890
<i>Wanfu Liu, Jianhui Wu</i>	
A Timing Interleaving RX Scheme with direct Multiplexing Sampler based on dual reference for DDR interface	895
<i>Mia Xu, Chris Eom, Kenji Wen, Tinna Ding, Bosco Lai</i>	
Graph-Based Representation of Verilog HDL: Python-Based Control and Data Flow Graph Generation	899
<i>Yipeng Wang, Zhiqiang He, Lingwei Yan, Gang Chen</i>	

A Node Merging Algorithm Using Fault-Detection for XOR-Majority Network	904
<i>Shijia Fan, Feifei Deng</i>	
FMSRdiff: Efficient latent diffusion framework combining consistency model and flow matching for super-resolution	910
<i>QunKai Peng, GuoFeng Cai, YiHua Xu, Kuan-Chang Chang, Lei Li, GuiBo Luo</i>	
An FBAR Driven Fractional-N Ring PLL Using Harmonic-Mixer-Based Dual Feedback and Split-Feedback Frequency Division	918
<i>Qinglong Tian, Jiwei Huang, Hongqu Lin</i>	
A Fault Tolerant Routing Method for 3D Network on Chip without Redundant TSV or Router-Avoidance	923
<i>Zeyi Lin, Duo Yu, Yanzhou Tang, Naifeng Jing, Jianfei Jiang, Weiguang Sheng, Lifu Cheng, Qin Wang</i>	
The Mechanical Properties of Wrinkled MnPS ₃ Structures	929
<i>Tongxu Huang, Jiaxian Sun, Zihao Wu, Yiting Wei, Wenjun Chen</i>	
Supercritical Fluid-Engineered p-GaN Thin Films with Improved Electrical and Optical Properties	933
<i>Yao-Li Chuang, Lei Li, Lei Lu, Kuan-Chang Chang</i>	
Design for Hardware Acceleration of Signature Verification in PQC Stateless Hash-Based Digital Signature Algorithm	937
<i>Haoran Liu, Liji Wu, Lei Li, Yifan Yang, Xiangmin Zhang</i>	
A 88 -dB SNDR 156-KHz-BW Noise-Shaping SAR ADC with 3rd-CIFF Structure and Dynamic Integrator	943
<i>Yulin Feng, Mei Jiang, Xinhui He, Zhengru Li</i>	
Mo ₂ C-MoS ₂ Mixed-Dimensional Bulk Heterostructure-Based Memristor for Artificial Synapses	948
<i>Libin Liang, Ziyao Lu, Zhenhua Guo, Chunyi Qiu, Zhuoling Zhou, Changjiu Teng</i>	
Artificial Neural Network-Based Compact Model for Carbon Nanotube Field-Effect Transistors	953
<i>Zhi Zhang, Honggang Liu</i>	
Electronic Properties of Violet Phosphorus Devices	958
<i>Chunyi Qiu, Ziyao Lu, Yiting Wei, Jiaxian Sun, Shilong Zhao</i>	
A SiC Power Module Package Based on the Dual-side Cooling with Highly Thermally Conductive Graphite-Molybdenum Spacer	962
<i>Yucheng Xu, Jiafei Yao, Yuxuan Dai, Ziwei Hu, Fan Yang, Kemeng Yang, Binbin Xu, Zhikuang Cai, Yufeng Guo</i>	
Work Function Variation Effect Prediction on Heterojunction Tunnel FET Using Multi-Layer Perceptron-Based Neural Network Model	967
<i>Haotong Han, Yunhe Guan, Tongqing Yan, Weihai Sun, Xiangtai Liu, Haifeng Chen</i>	
Enhancing Carrier Mobility in a-IZO/a-IGZO Thin-Film Transistors through Band Structure Engineering of Heterojunction Channels	972
<i>Huan Yang, Shengdong Zhang, Yong Wang, Chao Teng, Yi Shen, Yudong Liu</i>	
Effect of Temperature on ESD Characteristics in 30 nm Partially Depleted SOI MOSFET	977
<i>Liye Yu, Jingrui Wang, Zhongxu Chen, Yixin Zheng, Ziyang Dai, Mingzhi Wan</i>	

A Package-on-Package Module with Integrated FPGA Minimum System for 48-Channel Synchronous Sampling 16-bit ADC	984
<i>Han Li, Jiangbo Wei, Yuan Miao, Weize An, Xudong Wu, Huan Yu, Chao Wang</i>	