Let a Neural Network Be Your Invariant

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Abstract

Safety verification ensures that a system avoids undesired behaviour. Liveness complements safety, ensuring that the system also achieves its desired objectives. A complete specification of functional correctness must combine both safety and liveness. Proving with mathematical certainty that a system satisfies a safety property demands presenting an appropriate inductive invariant of the system, whereas proving liveness requires showing a measure of progress witnessed by a ranking function. Neural model checking has recently introduced a data-driven approach to the formal verification of reactive systems, albeit focusing on ranking functions and thus addressing liveness properties only. In this paper, we extend and generalise neural model checking to additionally encompass inductive invariants and thus safety properties as well. Given a system and a linear temporal logic specification of safety and liveness, our approach alternates a learning and a checking component towards the construction of a provably sound neural certificate. Our new method introduces a neural certificate architecture that jointly represents inductive invariants as proofs of safety, and ranking functions as proofs of liveness. Moreover, our new architecture is amenable to training using constraint solvers, accelerating prior neural model checking work otherwise based on gradient descent. We experimentally demonstrate that our method is orders of magnitude faster than the state-of-the-art model checkers on pure liveness and combined safety and liveness verification tasks written in SystemVerilog, while enabling the verification of richer properties than was previously possible for neural model checking.

1 Introduction

Model checking addresses the question of whether a reactive system $\mathcal{M}$ meets a specification of intended behaviour Φ [42]. Reactive systems are systems that continually respond to inputs and operate over infinite executions. Exemplars include hardware designs implementing processing units, communication and arbitration protocols, as well as digital controllers for automotive, aerospace, or medical applications, where safety is paramount. Safety properties require that *nothing bad ever happens*. A safety violation is a finite execution the last state of which falsifies Φ and the damage is irredeemable [77]. Safety properties are dual to liveness properties, which require that *something good eventually happens*. A liveness violation is evidenced by an infinite execution that falsifies Φ, as any finite violating prefix could in principle still be extended to a compliant execution [77]. Every linear-time specification is the composition of a safety and a liveness property [8], and linear temporal logic (LTL) provides an expressive language for specifying linear-time properties of reactive systems.

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SystemVerilog Assertions (SVA) bring linear-time logic into commercial hardware design flows [56], and electronic design automation vendors have spent decades optimising symbolic model checkers for them. Testing and simulation alone cannot fully guarantee that a system meets its specifications, and explicitly enumerating every possible behaviour is impractical, except for the most trivial hardware designs. Symbolic model checking has made it feasible to handle large state spaces. Two symbolic paradigms dominate. Algorithms based on binary decision diagrams (BDDs) provide sound and complete procedures for LTL model checking, yet BDDs often explode in size when faced with arithmetic data paths ubiquitous in modern hardware design [26, 52]. Bounded model checking (BMC) algorithms enjoy the much more scalable combinatorial and arithmetic reasoning of SAT solvers, but only explore the state space up to a finite depth, sacrificing completeness over unbounded execution [17]. Incremental algorithms for the construction of exploration frontiers (IC3) bridge that gap in unbounded safety verification [20], but fall short on liveness.

Neural model checking is an automated approach that leverages *neural certificates* to verify reactive systems against LTL specifications, but prior work has exclusively focused on liveness properties [63]. This prior cognate work learns ranking functions represented as neural networks—which serve as proof of liveness—from random executions and then checks their validity using symbolic reasoning, thereby providing formal guarantees. However, specifications that characterise pure safety or combinations of safety and liveness additionally demand the construction of inductive invariants—which serve as proofs of safety. Prior work does not construct such invariants, leaving safety out of reach.

In this paper, we demonstrate that neural networks are an effective representation for inductive invariants as well. Our novel method leverages neural certificates to simultaneously represent ranking functions and inductive invariants. Given a hardware design $\mathcal{M}$ and a non-deterministic Büchi automaton $\mathcal{A}_{\neg\Phi}$ that recognises the violations to an LTL formula Φ, we train a neural certificate on sample transitions of the synchronous composition $\mathcal{M} \parallel \mathcal{A}_{\neg\Phi}$. This network (i) classifies each state as inside or outside the invariant and (ii) ranks the states, within the invariant, to strictly decrease whenever an accepting state is encountered. We then pose a one-step BMC query to check if the neural certificate is true over the entire state space. On affirmation, this proves every accepting state is either (i) unreachable or (ii) visited at most finitely many times. This implies that no reachable behaviour of $\mathcal{M}$ satisfies $\neg\Phi$, thereby proving that every reachable behaviour of $\mathcal{M}$ satisfies Φ.

We implemented our method using a new neural ranking function architecture that enables training using constraint solvers, in contrast to prior work that exclusively relies on gradient descent for training [63]. Our new architecture yields more compact representations and it is much more efficient and numerically stable than prior work. We extended the prior benchmark with standard safety and combined liveness and safety verification problems, and have compared our method with the state-of-the-art hardware model checkers. Measuring against the per-task fastest on pure-liveness, our method is faster on $66\,\%$ of tasks, $10\times$ faster on $46\,\%$, $10^3\times$ on $11\,\%$, and $10^4\times$ on $4\,\%$. On pure safety tasks, while not outperforming, we match the best symbolic tools: $80\,\%$ of instances complete for all approaches in under $1\,$s. The picture changes dramatically for properties that demand *both* an inductive invariant and a ranking function: our method is faster than the leading model checkers on $61\,\%$ of tasks, running $10^2\times$ on $43\,\%$, $10^4\times$ on $27\,\%$, and $10^5\times$ on $6\,\%$.

Our contribution is threefold. First, by simultaneously representing inductive invariants and ranking functions using neural networks, we extend and generalise neural model checking to verify arbitrary LTL properties encompassing both safety and liveness. Second, by introducing a neural architecture amenable to training using constraint solvers, we achieve both superior runtime efficiency and numerical stability. Third, by evaluating our method across a 634-task benchmark suite, we demonstrate that our method outperforms the state of the art in automated formal verification.

2 Model Checking Safety and Liveness

We consider specifications Φ in LTL over a set of atomic propositions Π. LTL extends propositional logic with temporal operators: $\mathsf{X}\,\Phi$ meaning Φ holds at the next step, $\mathsf{F}\,\Phi$ meaning Φ eventually holds, $\mathsf{G}\,\Phi$ meaning Φ always holds, $\Phi_1 \,\mathsf{U}\, \Phi_2$ meaning Φ_1 holds at all times until Φ_2 necessarily holds at some future step, and $\Phi_1 \,\mathsf{W}\, \Phi_2$ meaning Φ_1 holds at all time before Φ_2 possibly occurs [102]. LTL naturally expresses safety, liveness, and their combinations for reactive systems. For $\Pi = \{\mathtt{a}, \mathtt{b}\}$, the formula $\mathsf{G}\ \mathtt{a}$ is a safety property: a single finite prefix whose last state violates $\mathtt{a}$ refutes it. By contrast, $\mathsf{F}\ \mathtt{b}$ is a liveness property: no finite execution suffices to disprove it, since $\mathtt{b}$ may still occur later. The formula $\mathtt{a}\,\mathsf{U}\,\mathtt{b}$ combines both: its safety component forbids any prefix containing $\neg\mathtt{a}\wedge\neg\mathtt{b}$ before the first $\mathtt{b}$, while its liveness component requires that $\mathtt{b}$ eventually occurs. Equivalently, $\mathtt{a}\,\mathsf{U}\,\mathtt{b} \;=\; \mathtt{a}\,\mathsf{W}\,\mathtt{b} \;\wedge\; \mathsf{F}\ \mathtt{b}$, where $\mathtt{a}\,\mathsf{W}\,\mathtt{b}$ is pure safety and $\mathsf{F}\ \mathtt{b}$ is pure liveness.

We model a reactive system $\mathcal{M}$ over a finite variable set $X_{\mathcal{M}}$ as a state transition system by an initial condition $\mathrm{Init}_{\mathcal{M}}$ and a sequential update relation $\mathrm{Update}_{\mathcal{M}}$. The variables are split into inputs $\mathrm{inp}\,X_{\mathcal{M}}$ and state-holding registers $\mathrm{reg}\,X_{\mathcal{M}}$. $\mathrm{Init}_{\mathcal{M}}$ is a first-order predicate over $\mathrm{reg}\,X_{\mathcal{M}}$ and $\mathrm{Update}_{\mathcal{M}}$ is a first-order predicate over $X_{\mathcal{M}} \cup \mathrm{reg}\,X'_{\mathcal{M}}$, where the set of primed variables denotes the next-cycle values. A reactive system $\mathcal{M}$ induces a transition system with state space S of valuations of $X_{\mathcal{M}}$, initial states $S_0 \subseteq S$ with $\boldsymbol{s} \in S_0 \iff \mathrm{Init}_{\mathcal{M}}(\mathrm{reg}\,\boldsymbol{s})$, and transition relation $\rightarrow_{\mathcal{M}} \subseteq S \times S$ with $\boldsymbol{s} \rightarrow_{\mathcal{M}} \boldsymbol{s}' \iff \mathrm{Update}_{\mathcal{M}}(\boldsymbol{s}, \mathrm{reg}\,\boldsymbol{s}')$. The executions of $\mathcal{M}$ are the infinite sequences $(\boldsymbol{s}_0, \boldsymbol{s}_1, \boldsymbol{s}_2 \ldots)$ where $\boldsymbol{s}_0 \in S_0$ and $\boldsymbol{s}_i \rightarrow_{\mathcal{M}} \boldsymbol{s}_{i+1}$ for all $i \in \mathbb{N}$.

We cast our model checking question as a language inclusion question. Given a system $\mathcal{M}$, we define as $\mathrm{obs}\,X_{\mathcal{M}} \subseteq X_{\mathcal{M}}$ its set of observables, and in turn define the language $L_{\mathcal{M}}$ of $\mathcal{M}$ as the set of sequences $(\mathrm{obs}\,\boldsymbol{s}_0, \mathrm{obs}\,\boldsymbol{s}_1 \ldots)$—which we call the traces of $\mathcal{M}$—induced by the executions $(\boldsymbol{s}_0, \boldsymbol{s}_1 \ldots)$ of $\mathcal{M}$. Given an LTL formula Φ over atomic propositions Π and the alphabet $\Sigma = 2^{\Pi}$ of valuations of Π, we define the language $L_{\Phi} \subseteq \Sigma^{\omega}$ of Φ as the set of all possible traces $(\sigma_0, \sigma_1 \ldots) \in \Sigma^{\omega}$ satisfying Φ. Provided that $\Pi = \mathrm{obs}\,X_{\mathcal{M}}$ (which we require to be Boolean), the model checking question asks whether $L_{\mathcal{M}} \subseteq L_{\Phi}$, i.e., all traces of $\mathcal{M}$ satisfy Φ. This is equivalent to the language emptiness question $L_{\mathcal{M}} \cap L_{\neg\Phi} = \emptyset$, i.e., no trace of $\mathcal{M}$ violates Φ [11, 42].

As is standard in automata-theoretic verification, we reduce the language emptiness question to an equivalent *fair emptiness* question. A non-deterministic Büchi automaton $\mathcal{A}$ consists of a finite set of states Q, an initial state $q_0 \in Q$, input alphabet Σ, transition relation $\delta \subseteq Q \times \Sigma \times Q$, and a set of fair states $F \subseteq Q$ [8, 39, 125]. This can be viewed as a reactive system with a single variable $X_{\mathcal{A}} = \{\mathtt{q}\}$ over Q, where $\mathrm{Init}_{\mathcal{A}}(q) \iff q = q_0$ and $\mathrm{Update}_{\mathcal{A}}(\sigma, q, q') \iff (q, \sigma, q') \in \delta$. We define the fair language $L^{\mathrm{f}}_{\mathcal{A}}$ of $\mathcal{A}$ as the set of traces of $\mathcal{A}$ whose respective executions visit F infinitely often. We rely on the fact that every LTL formula Φ admits a non-deterministic Büchi automaton $\mathcal{A}_{\Phi}$ for which $L^{\mathrm{f}}_{\mathcal{A}_{\Phi}} = L_{\Phi}$. Our reduction to fair emptiness thus constructs an automaton $\mathcal{A}_{\neg\Phi}$ and forms the synchronous product $\mathcal{M} \parallel \mathcal{A}_{\neg\Phi}$ between $\mathcal{M}$ and $A_{\neg\Phi}$ with the fair states defined as $S \times F$. We refer the reader to the literature for a full formal definition of the synchronous product [9, 11, 42]; the key property to note is that $L^{\mathrm{f}}_{\mathcal{M}\parallel\mathcal{A}_{\neg\Phi}} = L_{\mathcal{M}} \cap L^{\mathrm{f}}_{\mathcal{A}_{\Phi}}$. Hence, our language emptiness question and, in turn, our model checking question amount to deciding the fair emptiness question $L^{\mathrm{f}}_{\mathcal{M}\parallel\mathcal{A}_{\neg\Phi}} = \emptyset$.

We answer the fair emptiness question by presenting a certificate consisting of two components: (i) an inductive invariant defined as a set $I \subseteq \mathrm{reg}\,S \times Q$ that captures (or over-approximates) the reachable states of $\mathcal{M} \parallel \mathcal{A}_{\neg\Phi}$, and (ii) a ranking function $V : I \to \mathbb{W}$ over a well-founded relation $(\mathbb{W}, \prec)$ that assigns ranks to all states within the invariant that prove that all reachable executions visit fair states at most finitely many times. Concretely, for all $\boldsymbol{s}, \boldsymbol{s}' \in S$ and $q, q' \in Q$,

$$
\begin{aligned}
&\boldsymbol{s} \in S_0 && \Longrightarrow (\mathrm{reg}\,\boldsymbol{s}, q_0) \in I, && (1)\\
&(\boldsymbol{s}, q) \rightarrow_{\mathcal{M}\parallel\mathcal{A}_{\neg\Phi}} (\boldsymbol{s}', q') \;\wedge\; (\mathrm{reg}\,\boldsymbol{s}, q) \in I && \Longrightarrow (\mathrm{reg}\,\boldsymbol{s}', q') \in I, && (2)\\
&(\boldsymbol{s}, q) \rightarrow_{\mathcal{M}\parallel\mathcal{A}_{\neg\Phi}} (\boldsymbol{s}', q') \;\wedge\; (\mathrm{reg}\,\boldsymbol{s}, q) \in I && \Longrightarrow V(\mathrm{reg}\,\boldsymbol{s}, q) \succeq V(\mathrm{reg}\,\boldsymbol{s}', q'), && (3)\\
&(\boldsymbol{s}, q) \rightarrow_{\mathcal{M}\parallel\mathcal{A}_{\neg\Phi}} (\boldsymbol{s}', q') \;\wedge\; (\mathrm{reg}\,\boldsymbol{s}, q) \in I \;\wedge\; q \in F && \Longrightarrow V(\mathrm{reg}\,\boldsymbol{s}, q) \succ V(\mathrm{reg}\,\boldsymbol{s}', q'). && (4)
\end{aligned}
$$

Clauses (1) and (2) state that initial states lie in I and that I is closed under transitions, so I forms an over-approximation of the set of reachable states. Clauses (3) and (4) require that, along every transition whose source is in I, the rank V never increases, and it decreases strictly whenever the source state is fair ($q \in F$). Because $(\mathbb{W}, \prec)$ is well founded, only finitely many strict decreases are possible; hence, fair states must be visited at most finitely many times. This implies that all executions are unfair, i.e., $L^{\mathrm{f}}_{\mathcal{M}\parallel\mathcal{A}_{\neg\Phi}} = \emptyset$, which is equivalent to saying all traces of $\mathcal{M}$ satisfy Φ [125].

Figure 1 illustrates our workflow on an example. Figure 1a gives a SystemVerilog module $\mathcal{M}$ that satisfies the LTL property $\Phi = \mathtt{a}\ \mathsf{U}\ \mathtt{b}$. Figure 1b gives a Büchi automaton $\mathcal{A}_{\neg\Phi}$ recognising $\neg\Phi$. Figure 1c depicts the state space of the synchronous product $\mathcal{M} \parallel \mathcal{A}_{\neg\Phi}$: product states are arranged on a two-dimensional grid, each state corresponding to the pair of a state s_i of $\mathcal{M}$ (where i is the value of the register $\mathtt{c}$) and a state q_0, q_1, or q_2 of $\mathcal{A}_{\neg\Phi}$. The sole initial state is (s_0, q_0), and the dotted region indicates the inductive invariant I. Each state in I indicates in its upper-right corner the respective rank, taken from $\mathbb{N}$. Along each transition in I, the rank strictly decreases when leaving a fair state and never increases otherwise, ensuring that the sole fair cycle within I terminates. Notably,

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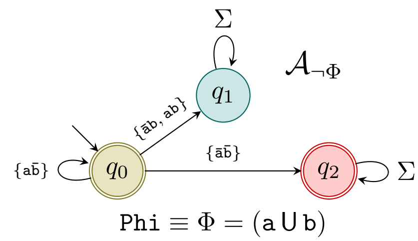
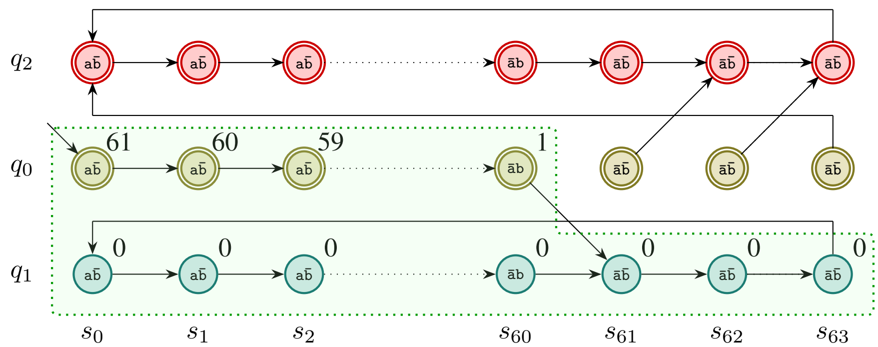
```
module MODEL (input clk, output reg a, b);
  reg [5:0] c = 0;
  assign a = (c < 60);
  assign b = (c == 60);
  always @(posedge clk) begin
      c <= c + 1;
  end
  Phi: assert property
    (@(posedge clk) a s_until b);
endmodule
```

(a)



(b)



(c)

Figure 1: Model checking safety and liveness on an illustrative example

the system has a non-terminating fair cycle (e.g., the cycle on q_2), but this is unreachable and excluded by I. In general, invariants may include unreachable states, provided none can lead to a fair cycle.

3 Neural Partially-Ranking Functions

We reduce the fair emptiness problem to a machine learning task by (i) modelling the invariant I as a *classifier* over-approximating the reachable states, and (ii) modelling the ranking function V as a *regressor*. In this section, we present our learn-check workflow which, upon termination of our procedure, formally ensures that these two components jointly satisfy conditions (1)–(4). Crucially, we introduce the *neural partially-ranking function*, which combines the definition of inductive invariant and ranking function into a single neural network.

We define a neural partially-ranking function over discrete parameter space Θ as the function

$$\bar{V} : \mathrm{reg}\, S \times \Theta \to \mathbb{Z} \tag{5}$$

Our objective is to learn an upper bound $\kappa \in \mathbb{Z}$ and a set of parameters $\{\theta_q \in \Theta\}_{q \in Q}$, such that for all $s, s' \in S$ and $q, q' \in Q$, the following two conditions hold:

$$s \in S_0 \quad\Longrightarrow\quad \kappa \geq \bar{V}(\mathrm{reg}\, s; \theta_{q_0}), \tag{6}$$

$$(s,q) \to_{\mathcal{M} \| \mathcal{A}_{\neg\phi}} (s', q') \wedge \kappa \geq \bar{V}(\mathrm{reg}\, s; \theta_q) \quad\Longrightarrow\quad \bar{V}(\mathrm{reg}\, s; \theta_q) \;\geq\; \bar{V}(\mathrm{reg}\, s'; \theta_{q'}) + \mathbf{1}_F(q). \tag{7}$$

where $\mathbf{1}_F(q) = 1$ if $q \in F$ else 0. The trainable network parameters are in Θ and are distinct for each automaton state $q \in Q$, while κ is global. The *initiation condition* of Eq. (6) ensures that all initial states receive a rank bounded above by κ. The *ranking condition* of Eq. (7) ensures that states bounded above by κ are inductively assigned a rank. Ultimately, a solution $\boldsymbol{\kappa}$ and $\{\boldsymbol{\theta}_q\}_{q \in Q}$ induces an invariant I and ranking function V satisfying the clauses (1)–(4), respectively defined as follows:

$$I = \left\{(\mathrm{reg}\, s, q) \,:\, \boldsymbol{\kappa} \geq \bar{V}(\mathrm{reg}\, s; \boldsymbol{\theta}_q)\right\}, \qquad V(\mathrm{reg}\, s, q) \;=\; \bar{V}(\mathrm{reg}\, s; \boldsymbol{\theta}_q) \text{ if } (\mathrm{reg}\, s, q) \in I. \tag{8}$$

Since the hardware state space S and Q are finite, the image $\bar{\mathbb{W}} = \{\bar{V}(\mathrm{reg}\, s; \boldsymbol{\theta}_q) \colon s \in S, q \in Q\}$ of $\bar{V}$ for a constant parameter $\{\boldsymbol{\theta}_q\}_{q \in Q}$ is finite as well, having a least element under the strict inequality $<$ over the integers. This makes $(\bar{\mathbb{W}}, <)$ well founded, having no infinite descending chain.

We train $\bar{V}$ in a counterexample-guided inductive synthesis loop as illustrated in Figure 2a [1, 117]. Our procedure incrementally constructs two datasets D_{init} and D_{trans} to train $\bar{V}$ to respectively satisfy

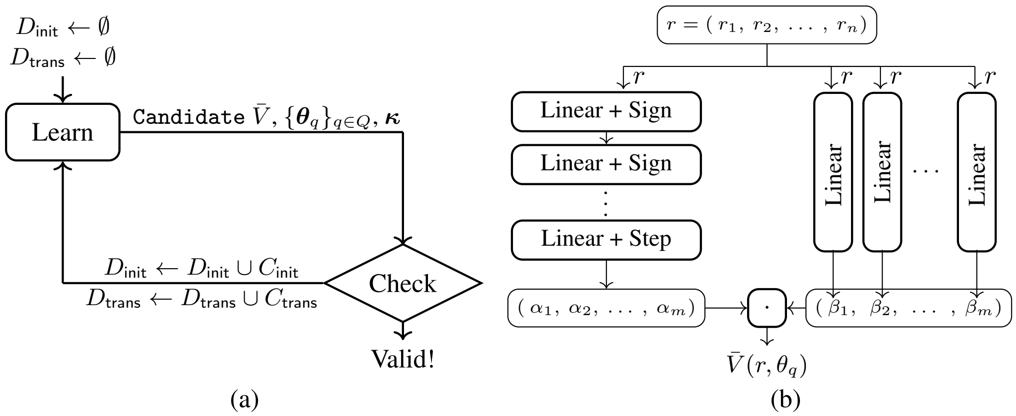


Figure 2: Our learn-check workflow (a) and our architecture for neural partially-ranking functions (b)

conditions (6) and (7). The dataset D_{init} contains sample initial register values $\operatorname{reg} \boldsymbol{s}$ of $\mathcal{M}$ where $\boldsymbol{s} \in S_0$, and the dataset D_{trans} contains sample transitions of $\mathcal{M} \parallel \mathcal{A}_{\neg\phi}$ in the form of quadruples $(\operatorname{reg} \boldsymbol{s}, \boldsymbol{q}, \operatorname{reg} \boldsymbol{s}', \boldsymbol{q}')$ where $(\boldsymbol{s}, \boldsymbol{q}) \rightarrow_{\mathcal{M}\parallel\mathcal{A}_{\neg\phi}} (\boldsymbol{s}', \boldsymbol{q}')$. Initially, we assume that D_{init} and D_{trans} are empty. Our learning component computes a set of parameters $\{\boldsymbol{\theta}_q\}_{q\in Q}$ to hold over the set of samples D_{init} and D_{trans}. Our checking component formally verifies whether conditions (6) and (7) hold over the entire state space. If the checker confirms the conditions, then the procedure halts successfully. In the converse case, it provides sets of counterexamples C_{init} and C_{trans}, which are respectively added to D_{init} and D_{trans}, and learning and checking are repeated in a loop.

Learning Our learning phase computes a set of parameters for which our initiation and ranking conditions are valid across all samples in the dataset. More precisely, enforcing our initiation condition amounts to satisfying the following constraint:

$$\operatorname{LearnInit}(\theta, \kappa) = \bigwedge_{\boldsymbol{r} \in D_{\mathsf{init}}} \big(\kappa \geq \bar{V}\big(\boldsymbol{r}; \theta_{q_0}\big)\big) \tag{9}$$

Similarly, satisfying our ranking condition amounts to satisfying the following constraint:

$$\operatorname{LearnRank}(\theta, \kappa) = \bigwedge_{(\boldsymbol{r},\boldsymbol{q},\boldsymbol{r}',\boldsymbol{q}') \in D_{\mathsf{trans}}} \big(\kappa \geq \bar{V}(\boldsymbol{r}; \theta_{\boldsymbol{q}}) \implies \bar{V}(\boldsymbol{r}; \theta_{\boldsymbol{q}}) \geq \bar{V}(\boldsymbol{r}'; \theta_{\boldsymbol{q}'}) + \mathbf{1}_F(\boldsymbol{q})\big) \tag{10}$$

Overall, our learning phase is tasked to solve the following question which, as we show in Section 4, we cast to a constraint satisfaction problem:

$$\exists \theta, \kappa \colon \operatorname{LearnInit}(\theta, \kappa) \wedge \operatorname{LearnRank}(\theta, \kappa) \tag{11}$$

If a valid set of parameters exists, then this is passed on to the checking phase. If a valid set of parameters does not exist, this indicates a larger network is needed or no solution exists at all. In this case, our strategy is to progressively add a hidden layer or widen it and retry until a preset limit.

Checking Our checking phase determines the presence or the absence of counterexamples to our initiation and ranking conditions for the candidate parameters $\boldsymbol{\kappa}, \{\boldsymbol{\theta}_q\}_{q\in Q}$. More precisely, a counterexample for the initiation condition must satisfy the following constraint:

$$\operatorname{CheckInit}(s) = \operatorname{Init}_{\mathcal{M}\parallel\mathcal{A}_{\neg\Phi}}(s, q_0) \wedge \boldsymbol{\kappa} < \bar{V}(\operatorname{reg} s; \boldsymbol{\theta}_{q_0}) \tag{12}$$

Similarly, a counterexample for the ranking condition must satisfy the following constraint:

$$\begin{aligned} \operatorname{CheckRank}(s, q, r', q') = {} & \operatorname{Update}_{\mathcal{M}\parallel\mathcal{A}_{\neg\Phi}}(s, q, r', q') \wedge \\ & \boldsymbol{\kappa} \geq \bar{V}(\operatorname{reg} s; \boldsymbol{\theta}_q) \wedge \bar{V}(\operatorname{reg} s; \boldsymbol{\theta}_q) < \bar{V}(r'; \boldsymbol{\theta}_{q'}) + \mathbf{1}_F(q) \end{aligned} \tag{13}$$

Overall, our checking phase asks whether the following statement holds:

$$\exists s \colon \operatorname{CheckInit}(s) \quad \vee \quad \exists s, q, r', q' \colon \operatorname{CheckRank}(s, q, r', q') \tag{14}$$

We check the initialisation and ranking conditions independently. If both queries are unsatisfiable, then we conclude that $\bar{V}$ is a valid neural partially-ranking function. If either or both are satisfiable,

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then the respective assignments constitute counterexamples. To produce multiple counterexamples C_{init} or C_{trans} in each iteration, we check (13) over explicitly enumerated automaton pairs (q, q') independently. This accelerates convergence, and gives equal emphasis to each transition of $\mathcal{A}_{\neg\Phi}$.

Our counterexample-guided inductive synthesis procedure captures task-specific edge cases that yield succinct datasets. This is in contrast to prior work that benefits from random initialisation of the datasets before the first iteration [63]. Moreover, as we show in Section 4, we further optimise our procedure by proposing a specialised architecture that is amenable not only to checking but also to learning using efficient and numerically stable constraint satisfaction solvers.

4 Learning Neural Partially-Ranking Functions Using MILP Solvers

We present a specialised architecture for neural partially-ranking functions amenable to training using constraint satisfaction solvers. Our architecture is illustrated in Figure 2b. Given a vector of word-level register values $r = (r_1, \dots, r_n)$ with $n = |\operatorname{reg} X_{\mathcal{M}}|$, our architecture feeds r into two branches. The left component $\alpha^{(r,q)}$ consists of L fully connected layers $(W_1^{(q)}, b_1^{(q)}, \dots, W_L^{(q)}, b_L^{(q)})$ with $N_1, \dots, N_L$ neurons, respectively, sign activation functions on the hidden layers, and step function on the output layer featuring $m = N_L$ neurons. The right component consists of m linear functions with n inputs each: $\beta^{(r,q)} = A^{(q)} r + c^{(q)}$. The left component α acts as a *mask* that selects or excludes the linear functions of the right component β; in other words, $\bar{V}(r, \theta_q) = \alpha^{(r,q)} \cdot \beta^{(r,q)}$.

Every application of arguments $(\boldsymbol{r}, \theta_{\boldsymbol{q}})$ to $\bar{V}$ in Eqs. (9)–(11) requires encoding. We build upon the result for which feed-forward neural networks with sign activation functions are amenable to training with mixed-integer linear programming (MILP) solvers [67, 121]. Henceforth, we use i, j to index individual elements of linear components, specifically i for the inputs elements and j for output elements, and we use l to index layers of the network. A single hyperparameter $P \in \mathbb{N}_{>0}$ bounds the magnitude of all decision variables in the encoding. Decision variables shared across multiple occurrences of $\boldsymbol{r}$ and associated to a common $\boldsymbol{q}$ are denoted as $w_{i\ell j}^{(\boldsymbol{q})}, b_{\ell j}^{(\boldsymbol{q})}, a_{ij}^{(\boldsymbol{q})}, c_j^{(\boldsymbol{q})} \in [-P, P]$ to respectively refer to the elements of $W_l^{(\boldsymbol{q})}$, $b_l^{(\boldsymbol{q})}$, $A^{(\boldsymbol{q})}$ and $c^{(\boldsymbol{q})}$; the threshold $\kappa \in [-P, P]$ is also a common decision variable in the learning phase. Decision variables associated to specific occurrences of $\boldsymbol{r}$ and $\boldsymbol{q}$ are $u_{\ell j}^{(\boldsymbol{r},\boldsymbol{q})} \in \{0, 1\}$ to indicate the activation status of the corresponding neurons, $z_{i\ell j}^{(\boldsymbol{r},\boldsymbol{q})}$ to represent neuron-weight products where $z_{i1j}^{(\boldsymbol{r},\boldsymbol{q})} \in [-PM_{\boldsymbol{r}}, PM_{\boldsymbol{r}}]$ with $M_{\boldsymbol{r}} = \max(|\boldsymbol{r}_1|, \dots, |\boldsymbol{r}_n|)$ and $z_{i\ell j}^{(\boldsymbol{r},\boldsymbol{q})} \in [-P, P]$ with $l \geq 2$, and finally $v_j^{(\boldsymbol{r},\boldsymbol{q})} \in [-PM_{\boldsymbol{r}}, PM_{\boldsymbol{r}}]$ to represent the overall output of the network. First, we encode the relationship between z, $\boldsymbol{r}$ and w at layer 1 as

$$z_{i1j}^{(\boldsymbol{r},\boldsymbol{q})} = \boldsymbol{r}_i w_{i1j}^{(\boldsymbol{q})} \tag{15}$$

Then, for $l = 1, \dots, L$, we encode the relationship between u, z and b at layer l (where $\epsilon > 0$) as

$$\left(u_{\ell j}^{(\boldsymbol{r},\boldsymbol{q})} = 1 \Rightarrow b_{\ell j} + \textstyle\sum_{i \in N_{\ell-1}} z_{i\ell j}^{(\boldsymbol{r},\boldsymbol{q})} \geq \epsilon\right) \wedge \left(u_{\ell j}^{(\boldsymbol{r},\boldsymbol{q})} = 0 \Rightarrow b_{\ell j} + \textstyle\sum_{i \in N_{\ell-1}} z_{i\ell j}^{(\boldsymbol{r},\boldsymbol{q})} \leq -\epsilon\right) \tag{16}$$

For $l = 2, \dots, L$, we encode the relationship between u at layer $l-1$ and z and w at layer l as

$$\begin{aligned}
&(z_{i\ell j}^{(\boldsymbol{r},\boldsymbol{q})} - w_{i\ell j}^{(\boldsymbol{q})} + 2P\, u_{(\ell-1)i}^{(\boldsymbol{r},\boldsymbol{q})} \leq 2P) \wedge (z_{i\ell j}^{(\boldsymbol{r},\boldsymbol{q})} + w_{i\ell j}^{(\boldsymbol{q})} - 2P\, u_{(\ell-1)i}^{(\boldsymbol{r},\boldsymbol{q})} \leq 0) \wedge \\
&(z_{i\ell j}^{(\boldsymbol{r},\boldsymbol{q})} - w_{i\ell j}^{(\boldsymbol{q})} - 2P\, u_{(\ell-1)i}^{(\boldsymbol{r},\boldsymbol{q})} \geq -2P) \wedge (z_{i\ell j}^{(\boldsymbol{r},\boldsymbol{q})} + w_{i\ell j}^{(\boldsymbol{q})} + 2P\, u_{(\ell-1)i}^{(\boldsymbol{r},\boldsymbol{q})} \geq 0)
\end{aligned} \tag{17}$$

which represents $z_{i\ell j}^{(\boldsymbol{r},\boldsymbol{q})} = w_{i\ell j}$ if $u_{(\ell-1)j}^{(\boldsymbol{r},\boldsymbol{q})} = 1$, and $z_{i\ell j}^{(\boldsymbol{r},\boldsymbol{q})} = -w_{i\ell j}$ otherwise. Finally, we encode the relationship between v, a, c and u at layer L as

$$\left(u_{Lj}^{(\boldsymbol{r},\boldsymbol{q})} = 1 \Rightarrow v_j^{(\boldsymbol{r},\boldsymbol{q})} = c_j^{(\boldsymbol{q})} + \textstyle\sum_{i \in n} \boldsymbol{r}_i a_{ij}^{(\boldsymbol{q})}\right) \wedge \left(u_{Lj}^{(\boldsymbol{r},\boldsymbol{q})} = 0 \Rightarrow v_j^{(\boldsymbol{r},\boldsymbol{q})} = 0\right) \tag{18}$$

As a result, each occurrence of $\bar{V}(\boldsymbol{r}, \theta_{\boldsymbol{q}})$ in Eqs. (9)–(11) corresponds to the linear term $\sum_{i \in m} v_i^{(\boldsymbol{r},\boldsymbol{q})}$.

Notably, a naïve encoding that represents $z_{i\ell j}^{(\boldsymbol{r},\boldsymbol{q})}$ as a product between a neuron variable and $w_{i\ell j}^{(\boldsymbol{q})}$ would induce bilinear constraints; our encoding avoids this and produces an equivalent encoding with linear constraints only. This enables using efficient MILP (and SMT) solvers in the learning phase.

Essentially, our architecture represents a piecewise function with 2^m configurations, given by $\alpha \in \{0, 1\}^m$, each of which induces a specific summation of linear functions, given by $\beta \in \mathbb{Z}^m$, in the spirit of piecewise-linear ranking functions [76, 123, 124]. In our implementation, we restrict all decision variables to the *integer* type, which results in neural networks that are naturally quantised.

Table 1: Tasks completed per tool, per design; in bold the max per design, per spec-type

	LS	LCD	Tmcp	i2cS	7-Seg	PWM	VGA	UARTt	Delay	Gray	Blink	Total
Pure Safety												
Tasks	16	28	17	20	15	12	20	10	32	11	25	206
`Our`	**16**	**28**	**17**	4	**15**	**12**	**20**	**10**	**32**	**11**	**25**	190
`ABC`	**16**	**28**	**17**	**20**	**15**	**12**	**20**	**10**	**32**	**11**	**25**	206
`nuXmv`	**16**	**28**	**17**	**20**	**15**	**12**	**20**	**10**	**32**	**11**	**25**	206
`rIC3`	**16**	**28**	**17**	**20**	**15**	2	**20**	**10**	**32**	**11**	**25**	196
Pure Liveness												
Tasks	16	14	17	20	30	12	10	10	32	33	25	219
`Our`	0	**14**	**17**	**20**	**30**	**12**	**10**	**10**	**32**	**33**	**14**	192
`ABC`	3	5	9	4	10	3	5	**10**	8	16	5	78
`nuXmv`	12	13	**17**	16	28	7	4	**10**	**32**	**33**	8	180
`rIC3`	7	7	13	7	17	4	6	**10**	14	19	6	110
`NMC'24`	**15**	3	10	**20**	**30**	10	9	**10**	**32**	**33**	0	172
Safety + Liveness												
Tasks	32	14	17	20	15	12	10	10	32	22	25	209
`Our`	**32**	**14**	**17**	3	9	**12**	**10**	**10**	**32**	**22**	11	172
`ABC`	7	12	11	**20**	5	3	**10**	7	6	11	4	96
`nuXmv`	11	12	14	16	**15**	6	**10**	**10**	26	14	**20**	154
`rIC3`	12	**14**	14	**20**	8	4	**10**	9	18	14	6	129

5 Experimental Evaluation

Implementation We implemented a prototype using a modular `Python` 3.12 pipeline [2]. Given an LTL formula Φ, we obtained $\mathcal{A}_{\neg\Phi}$ with `Spot` 2.11.6 [51], converted SystemVerilog to bit-vector SMT using `EBMC` 5.6 [91], performed validity queries and computed counterexamples using `Bitwuzla` 0.7.0 [96], and trained a neural partially-ranking function using the MILP solver `Gurobi` 12.0.1 [65]. Our method relies on a single global hyperparameter configuration, besides the integer bound P (see Section 4). We chose P from a finite set of configurations $\{1, 5, 10, \lfloor M/10 \rfloor, \lfloor M/2 \rfloor, M, M{+}1, 2M\}$, where M is the largest value any register can take in the hardware design; this renders the bounds for z_{i1j} and v_j quadratic in M except when $P = 1$, 5, or 10. We configured the architecture to start with a linear model (per $q \in \mathcal{A}_{\neg\phi}$) and add one hidden layer with a single neuron (left branch of Figure 2a) upon the first failure of the learning phase, subsequently increasing its width by one neuron upon subsequent failures, up to 5 attempts.

Experimental Setup Building on the ten parameterised SystemVerilog designs and 194 pure-liveness tasks of prior work [63], we add an eleventh design and, for all eleven, contribute additional pure-safety and combined safety–liveness specifications on each task, yielding a 634-task suite that retains the original diversity (Appendix A). We compared against (i) the gradient-based neural model checking approach, labelled `NMC'24` (liveness only) [63], and (ii) the winners of recent HWMCC editions [107]: `nuXmv` 2.1.0 [28], `rIC3` 1.5.1 [119], and `ABC/Super-Prove` [24]. For `nuXmv` we translated each design with its assertions to SMV using `EBMC`; then, we converted SMV to AIG for `ABC` and `rIC3` with `AIGER` [18], yielding a fully automated flow. All experiments ran on an AWS m6a.4xlarge instance (16 vCPUs, 64 GB RAM, Ubuntu 24.04). Each task had a $5\,\mathrm{h}$ timeout per tool; in aggregate, the experiments consumed $9083\,\mathrm{h}$ ($\approx 378\,\mathrm{d}$) of compute time.

Overall Efficacy Table 1 presents all solved instances by property class. For *pure-safety*—historically emphasised in HWMCC [16, 107]—symbolic tools clear $\geq 95\,\%$ of tasks, and we remain close to decades-mature tools at $92\,\%$. For *pure-liveness*, performance spreads: `nuXmv` $82\,\%$, `ABC` $36\,\%$, `rIC3` $50\,\%$, `NMC'24` $79\,\%$, while we complete $88\,\%$. On *safety–plus-liveness* properties, the gap widens, `nuXmv` solves $74\,\%$, `ABC` $46\,\%$, `rIC3` $61\,\%$, and our approach reaches $82\,\%$.

Comparison on Pure Safety We generally perform on par with leading symbolic checkers with decades of optimisation, as Figure 3a indicates, while being faster than `NuXmv` on $17\,\%$, `rIC3` on

[2]`https://github.com/aiverification/neuralmc`

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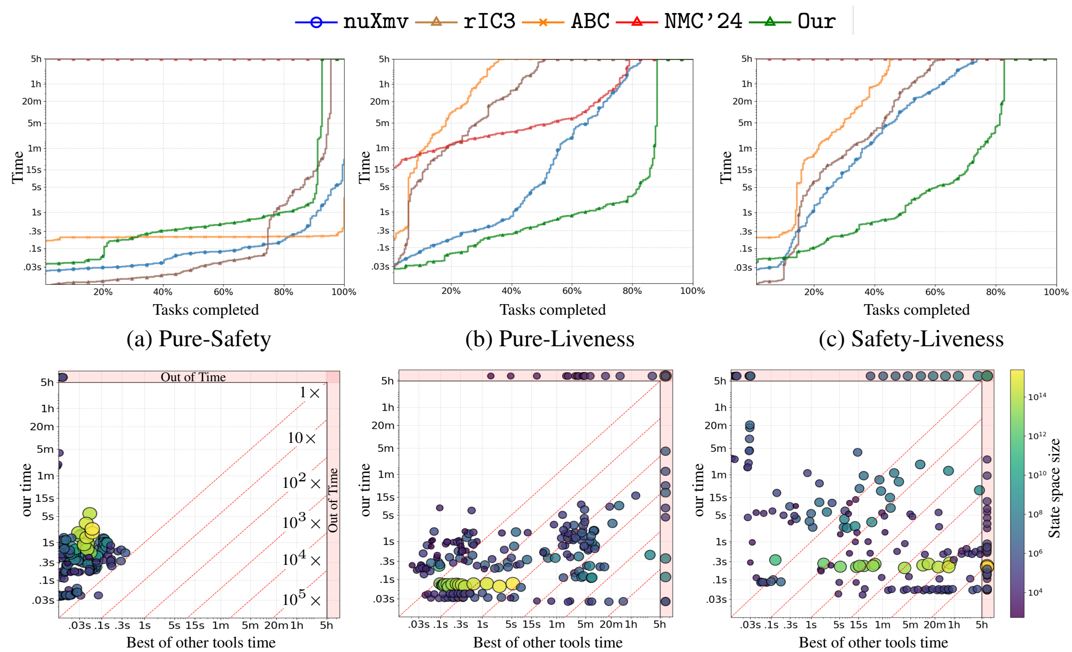


(a) Pure-Safety (b) Pure-Liveness (c) Safety-Liveness

(d) Pure-Safety (e) Pure-Liveness (f) Safety-Liveness

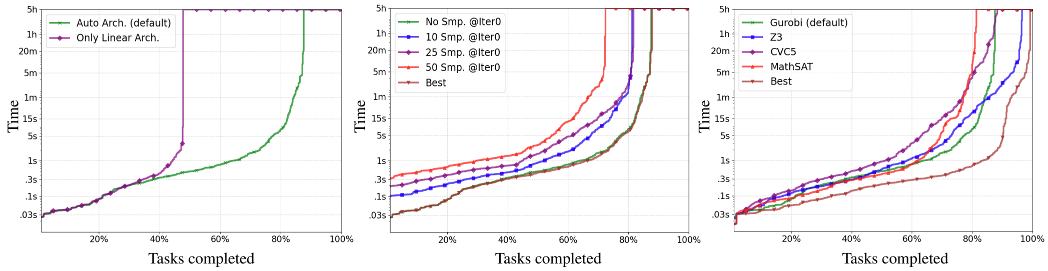
Figure 3: Runtime comparison with the state of the art (all times are in *log scale*)

$25\,\%$, and ABC on $32\,\%$ of safety tasks. Figure 3d plots each individual task by time, with the per-task fastest symbolic solver on the x-axis and our method on the y-axis; point size and brightness reflect state-space size. While symbolic tools often lead on individual instances, in $80\,\%$ of tasks both finish within $1\,$s, indicating that a our method can meaningfully match a portfolio of symbolic safety checkers, besides being the first neural model checking framework to support general safety.

Comparison on Pure Liveness Figure 3b indicates that our method is consistently faster than the others. Within $1\,$s we solve $24\,\%$ more tasks than `nuXmv`, $59\,\%$ more tasks than `rIC3`, $59\,\%$ more than `ABC`, and $64\,\%$ more than `NMC'24`; at $1\,\mathrm{min}$ the margins widen to $31\,\%$, $68\,\%$, $76\,\%$, $71\,\%$, and they still measure $12\,\%$, $45\,\%$, $59\,\%$, $13\,\%$ after $1\,$h. The percentage of tasks completed in $5\,$h per task by `nuXmv`, `NMC'24`, `rIC3`, and `ABC` are completed in under $7\,$s, $3\,$s, $0.6\,$s, $0.3\,$s by our method. Figure 3d shows the per-task runtime gains against the fastest competing method per task: our method is faster on $66\,\%$ of tasks, at least $10\times$ faster on $46\,\%$, $10^2\times$ faster on $29\,\%$, $10^3\times$ faster on $11\,\%$, $10^4\times$ faster on $4\,\%$, and $10^5\times$ faster on $1\,\%$ with respect to the whole state of the art. On a specific comparison with `NMC'24` we obtain speedups of at least $10\times$ on $88\,\%$, $10^2\times$ on $79\,\%$, $10^3\times$ on $45\,\%$, $10^4\times$ on $18\,\%$, and $10^5\times$ on $5\,\%$. Finally overall, $5\,\%$ of tasks timeout for all tools except ours.

Comparison on Combined Safety and Liveness Figure 3c indicates that the performance gap between our method and the alternatives further widens on safety-liveness tasks. Within $1\,$s our approach completes $31\,\%$ more tasks than `nuXmv`, $34\,\%$ more than `rIC3` and $36\,\%$ more than `ABC`; after $1\,\mathrm{min}$ the gaps grow to $38\,\%$, $43\,\%$, $54\,\%$, and persist at $20\,\%$, $31\,\%$, $41\,\%$ after $1\,$h. Benchmarks that exhaust `nuXmv`, `ABC` or `rIC3` in $5\,$h finish in $56\,$s, $6\,$s, $0.8\,$s per task with our approach. Figure 3f shows that we are faster on $61\,\%$, $10\times$ faster on $52\,\%$, $10^2\times$ faster on $43\,\%$, $10^3\times$ faster on $36\,\%$, $10^4\times$ faster on $27\,\%$, and $10^5\times$faster on $6\,\%$ of the tasks; all tools, besides ours, hit the $5\,$h timeout on $18\,\%$ of the task suite, bringing arbitrary LTL verification to runtime parity with pure-safety.

Neural Certificates Expressivity In Figure 4a, `Auto` is our default configuration that starts with linear for each state q of $\mathcal{A}_{\neg\Phi}$ and escalates to neural models only if linear is infeasible; `Only Linear` is the ablation that *exits* immediately when the linear model fails. The linear model completes $48\,\%$ of tasks within $9\,$s per task and makes no progress thereafter; by contrast, our default finishes $87\,\%$ overall. Since the default always tries the linear model first, it never trails the ablation; when linear



(a) Linear Architecture Ablation (b) Uniformly Random Samples (c) Other Learning Engines

Figure 4: Runtime analysis of our approach (all times are in *log scale*)

fails, automatic widening provides the expressivity needed to solve a lot more instances, showing that purely affine certificates are insufficient while our neural-certificate architecture succeeds.

Comparison with Random Dataset Generation Our iterative procedure presented in Figure 2a starts with empty datasets D_{init} and D_{trans} and populates them purely via a counterexample-guided procedure, which identifies edge-cases one by one towards the synthesis of neural partially-ranking functions. This is in contrast with the cognate neural model checking approach based on gradient descent, which benefits from random test generation to initially populate the datasets and rarely relies on the generation of data by means of counterexamples [63, Section 5]. Figure 4b evaluates our MILP-based approach under multiple random initialisation sizes with 0 (our default), 10, 25, and 50 randomly generated samples, respectively. As our experiment indicates, our default approach is nearly indistinguishable from the *Best* curve (which indicates the fastest configuration per instance). This indicates that our MILP-based approach does not benefit from unguided random data generation.

Comparison with SMT Learning Engines Our new architecture makes learning amenable to MILP solving and, more generally, to decision procedures for linear theories implemented in SMT solvers. Figure 4c compares alternative engines for our learn phase, where we replace the MILP solver `Gurobi` with the SMT solvers `CVC5` 1.1.2 [14], `MathSAT` 5.6.10 [36], and `Z3` 4.13.0 [49] via `PySMT` [59]. Within the $5\,\mathrm{h}$ timeout, `MathSAT` completed $81\,\%$ of tasks, `Gurobi` completed $87\,\%$, `CVC5` completed $88\,\%$, and `Z3` completed $96\,\%$ of tasks. `Gurobi` and `Z3` offer the best compromise between speed and efficacy, with `Z3` demonstrating superior coverage and `Gurobi` shorter runtimes: `Gurobi` was on average $7\times$ faster than `Z3` on successfully solved instances. However, `Gurobi` failed to return a result in $13\,\%$ of cases because of memory segmentation faults, model infeasibility for our hyper-parameters, numerical mismatches after evaluation of the result with `NumPy`; only 2 tasks were timeouts. The *Best* curve selects the fastest engine per instance—obviously outperforming every other solver, providing a baseline for a potential portfolio implementation. We remark that all experiments besides this comparison (Figure 4c) use only `Gurobi` as its learning engine.

Strengths and Limitations Our approach is much more straightforward in terms of parameter tuning then the prior neural model checking approach [63], owing to the theoretical completeness and the superior numerical stability of MILP and SMT algorithms over stochastic gradient descent. However, this strongly relies on sign-activated feed-forward neural networks; the generalisation to further architectures is an open problem for future investigation. Our method is amenable to training over parameters of integer type, which naturally results in quantised neural partially-raking functions. On the other hand, our approach is limited to hardware and reactive systems without arrays or strings of parametric length, procedure calls or dynamic data structures, which are topics for future work.

Threats to Validity Our empirical evaluation has demonstrated the superior performance of our approach over the state of the art on verification tasks derived from standard textbook level hardware designs. Our benchmark suite encompasses word-level designs with safety and liveness properties, unlike the standard HWMCC'24 benchmarks which focus on pure safety properties [19]. Our benchmark is arguably the hardest (as of today) for word-level liveness and combined safety-liveness hardware verification. Yet, our evaluation may not be representative of verifications tasks other than our suite and further research is required to assess the generalisability and the scalability of our approach to other workloads. Future work includes the integration of neural and compositional model checking towards the scalable formal verification of industrial-scale designs [40, 88, 134].

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6 Related Work

Model Checking Linear Temporal Logic Formal hardware verification relies on model checking LTL specifications—codified, e.g., as SystemVerilog Assertions—to guarantee safety and liveness properties [8, 56, 77, 102]. Symbolic engines based on BDD fixed-points [10, 41, 75] or SAT/IC3 reasoning [17, 20, 73, 87, 114] among other methods have evolved over fifty years, with key contributions to formal verification honoured by the ACM Turing Awards of 1996, 2007, and 2013. The automata-theoretic approaches to model checking often reduce model checking to fair-emptiness. This has been tackled via k-liveness bounded model checking [38, 69], IC3 with strongly connected components [23], or BDDs with Emerson–Lei fixed-point computation [52]. Ranking functions were originally devised for program termination [55] and later generalised to liveness certificates [5, 6, 44, 50, 64, 81, 125], may be linear [21, 104], piecewise-defined [76, 123, 124], word-level [32, 47], lexicographic [22, 82], or represented as disjunctive well-founded relations [37, 43, 45, 74, 103]. Traditional algorithms for the automated construction of ranking functions and inductive invariants usually rely on constraint solving (using Farkas' lemma or Positivstellensatz results) or abstract interpretation [31, 43, 45, 74, 103, 105].

Machine Learning for Automated Reasoning Neural methods have permeated every layer of formal reasoning. In theorem proving, they guide clause selection [53, 84], premise selection [13, 68, 89, 127], tactic prediction [100, 132], and even end-to-end proof search [54, 106]. In constraint solving, neural approaches have been integrated into SMT [12, 85, 112] and SAT solving [61, 79, 113, 128], and have been further extended to combinatorial optimisation [83] and MILP [60, 93]. Similar ideas have been applied to program synthesis [15, 33, 72, 122], algorithm selection [80, 86], termination analysis [7], circuit synthesis and repair from temporal logic specifications [46, 111], and generation of satisfying traces for given LTL properties [66]. A large body of work focussed on learning inductive invariants via teacher–learner loops [57], decision trees [58, 76], random search [115], data-driven templates [98], neural networks [109, 133], reinforcement learning [116, 131] and, most recently, large language models [29, 71, 101, 130]. These techniques target safety alone; LTL specifications that encompass both safety *and* liveness are out of scope. Handling properties that combine safety and liveness using machine learning fills a significant gap in the field.

Neural Certificates As opposed to using neural networks to *generate* formal proof certificates, our approach uses neural networks to *represent* them (along with mathematical guarantees), falling within the spectrum of neural certificates. This extends recent work on control [2, 30, 48, 78, 92, 95, 108, 135–137], formal verification of software and probabilistic programs [3, 4, 62], and model checking reactive systems under *pure liveness* LTL properties [63]. Our work has enabled neural certificates to effectively prove *arbitrary* LTL properties, orders of magnitude faster than the state of the art.

7 Conclusion

We have presented a novel and improved neural model checking approach for arbitrary compositions of safety and liveness specifications. By introducing a specialised neural partially-ranking function architecture that (i) simultaneously represents inductive invariants and ranking functions and (ii) is amenable to training with numerically stable MILP solvers in a counterexample-guided procedure, our method yields compact and naturally quantised certificates. We implemented a lightweight Python prototype that combines off-the-shelf MILP (`Gurobi`), SMT (`Bitwuzla`), and BMC (`EBMC`) to train and certify the network in an iterative approach that provides formal guarantees [65, 91, 96]. Our improved technique attains speedups up to $10^5\times$ and $10\,\%$ higher completion (within a $5\,\mathrm{h}$ time limit) over the state-of-the-art symbolic model checkers and prior work on neural model checking [24, 28, 63, 119], on a benchmark suite of 634 hardware model checking tasks encompassing safety, liveness and combined safety-liveness verification tasks written in SystemVerilog.

A complete specification for the functional correctness of reactive systems must capture *both* safety and liveness: the former guarantees the absence of undesired behaviour; the latter guarantees the presence of desired behaviour. Our approach has extended neural model checking to capture both safety and liveness, simultaneously. This paves a path towards the provably safe application of artificial intelligence and machine learning to the design of high-assurance industrial hardware, with impact to avionics [90, 118], automotive [97, 120], medical devices [70, 126], nuclear control [27, 99], rail signalling [34, 35], robotics [110, 129], utility grids [25, 94], and more.

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Model	LTL Specification (Pure-Liveness)
DELAY	$\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{GF}\ \texttt{sig}$
	$\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{GF}\left(\texttt{sig} \wedge \mathsf{X}\ \texttt{!sig}\right)$
LCD Controller	$\mathsf{FG}\ \texttt{lcd\_enable} \rightarrow \mathsf{GF}\ \texttt{ready}$
Blink	$\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{GF}\ \texttt{ledON}$
Thermocouple	$\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{GF}\ \texttt{get\_data}$
7-Segment	$\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{GF}\ \texttt{disp = 1}$
	$\mathsf{FG}\ \texttt{!rst} \rightarrow \left(\mathsf{GF}\ \texttt{disp = 0} \wedge \mathsf{GF}\ \texttt{disp = 1}\right)$
i2c Stretch	$\mathsf{FG}\left(\texttt{!rst} \wedge \texttt{ena}\right) \rightarrow \mathsf{GF}\ \texttt{strc}$
Pulse Width Modulation	$\mathsf{GF}\ \texttt{!pulse}$
VGA Controller	$\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{GF}\ \texttt{disp\_ena}$
UART Transmitter	$\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{GF}\ \texttt{wait}$
Load-Store	$\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{GF}\ \texttt{sig}$
Gray Counter	$\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{GF}\ \texttt{sig}$
	$\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{GF}\left(\texttt{sig} \wedge \mathsf{X}\ \texttt{!sig}\right)$
	$\mathsf{FG}\ \texttt{!rst} \rightarrow \left(\mathsf{GF}\ \texttt{sig} \wedge \mathsf{GF}\ \texttt{!sig}\right)$

Table 2: Model Name and LTL Specification in our Benchmark (Pure-Liveness)

Model	LTL Specification (Pure-Safety)
DELAY	$\mathsf{G}\ \texttt{!err}$
	$\mathsf{G}\left(\texttt{sig} \rightarrow \mathsf{X}\ \texttt{!sig}\right)$
LCD Controller	$\mathsf{G}\left(\left(\texttt{!lcd\_enable} \wedge \texttt{ready}\right) \rightarrow \mathsf{X}\ \texttt{ready}\right)$
	$\mathsf{G}\left(\mathsf{X}\ \texttt{wait} \rightarrow \texttt{busy}\right)$
Blink	$\mathsf{G}\left(\left(\texttt{mode1} \wedge \mathsf{X}\ \texttt{mode1}\right) \rightarrow \mathsf{X}\left(\texttt{cnt!=0}\right)\right)$
Thermocouple	$\mathsf{G}\left(\left(\texttt{ !spi\_busy } \wedge \texttt{ get\_data } \wedge \texttt{ !rst }\right) \rightarrow \mathsf{X}\ \texttt{get\_data}\right)$
7-Segment	$\mathsf{G}\left(\left(\texttt{!sig} \wedge \mathsf{X}\ \texttt{!sig} \wedge \texttt{!rst}\right) \rightarrow \left(\left(\texttt{ds0} \wedge \mathsf{X}\ \texttt{ds0}\right) \vee \left(\texttt{ds1} \wedge \mathsf{X}\ \texttt{ds1}\right)\right)\right)$
i2c Stretch	$\mathsf{G}\left(\left(\texttt{!strc} \wedge \mathsf{X}\ \texttt{strc}\right) \rightarrow \mathsf{X}\ \texttt{switch}\right)$
Pulse Width Modulation	$\mathsf{G}\left(\left(\texttt{pulseLB} \rightarrow \texttt{pulse}\right) \wedge \left(\texttt{!pulseUB} \rightarrow \texttt{!pulse}\right)\right)$
VGA Controller	$\mathsf{G}\left(\left(\texttt{en} \wedge \texttt{!rst}\right) \rightarrow \left(\left(\texttt{hs} \leftrightarrow \mathsf{X}\ \texttt{!hs}\right) \vee \left(\texttt{!hs} \leftrightarrow \mathsf{X}\ \texttt{hs}\right)\right)\right)$
	$\mathsf{G}\left(\left(\texttt{en} \wedge \texttt{!rst}\right) \rightarrow \left(\left(\texttt{vs} \leftrightarrow \mathsf{X}\ \texttt{!vs}\right) \vee \left(\texttt{!vs} \leftrightarrow \mathsf{X}\ \texttt{vs}\right)\right)\right)$
UART Transmitter	$\mathsf{G}\left(\left(\texttt{wait} \rightarrow \texttt{!busy}\right) \wedge \left(\texttt{transmit} \rightarrow \texttt{busy}\right)\right)$
Load-Store	$\mathsf{G}\left(\texttt{sig} \rightarrow \mathsf{X}\,\mathsf{X}\ \texttt{!sig}\right)$
Gray Counter	$\mathsf{G}\left(\left(\texttt{sig} \wedge \texttt{!rst}\right) \rightarrow \mathsf{X}\ \texttt{!sig}\right)$

Table 3: Model Name and LTL Specification in our Benchmark (Pure-Safety)

Model	LTL Specification (Safety-Liveness)
Delay	$\mathsf{G}\ \texttt{!rst} \rightarrow \mathsf{XG}\ (\ cnt < N\ \mathsf{U}\ \texttt{sig}\ )$
	$\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{FG}\ (\ cnt < N\ \mathsf{U}\ \texttt{sig}\ )$
LCD Controller	$\mathsf{G}\ \Big(\ \texttt{receive} \rightarrow\ (\ \texttt{receive}\ \mathsf{U}\ \texttt{ready}\ )\Big)$
Blink	$\mathsf{G}\ \texttt{!rst} \rightarrow\ \mathsf{G}\ \Big(\ \texttt{ledON} \rightarrow\ (\ \texttt{ledON}\ \mathsf{U}\ \texttt{mode0}\ )\Big)$
Thermocouple	$\mathsf{G}\ \texttt{!rst} \rightarrow\ \mathsf{G}\ \Big(\ \texttt{pause} \rightarrow\ (\ \texttt{pause}\ \mathsf{U}\ \texttt{get\_data}\ )\Big)$
7-Segment	$\mathsf{G}\ \texttt{!rst} \rightarrow\ \mathsf{G}\ \Big(\big((\ \texttt{ds0}\ \wedge\ \mathsf{X}\ \texttt{ds0})\ \vee\ (\ \texttt{ds1}\ \wedge\ \mathsf{X}\ \texttt{ds1})\big)\ \mathsf{U}\ \texttt{sig}\Big)$
i2c Stretch	$\mathsf{G}\ \texttt{!rst}\ \rightarrow\ \mathsf{G}\ \Big(\ \texttt{!strc} \rightarrow\ (\ \texttt{!strc}\ \mathsf{U}\ \texttt{switch}\ )\Big)$
Pulse Width Modulation	$\mathsf{GF}\ \texttt{!pulseUB}\ \wedge\ \mathsf{XG}\ \Big(\ \texttt{!pulseUB} \rightarrow\ \texttt{!pulse}\ \Big)$
VGA Controller	$\mathsf{G}\ \Big(\big(\ \texttt{Vcnt == 0}\ \big) \rightarrow\ \big((\ \texttt{Vcnt == 0}\ )\ \mathsf{U}\ (\ \texttt{Hcnt == 0}\ )\big)\Big)$
UART Transmitter	$\mathsf{G}\ \texttt{!rst} \rightarrow\ \mathsf{G}\ \Big(\ \texttt{busy} \rightarrow\ (\ \texttt{busy}\ \mathsf{U}\ \texttt{wait}\ )\Big)$
Load-Store	$\mathsf{G}\ \texttt{!rst} \rightarrow\ \mathsf{G}\ \Big(\ \texttt{modeUP} \rightarrow\ (\ \texttt{modeUP}\ \mathsf{U}\ \texttt{sig}\ )\Big)$
	$\mathsf{G}\ \texttt{!rst} \rightarrow\ \mathsf{X}\,\mathsf{G}\ \Big(\ \texttt{modeUP} \rightarrow\ (\ \texttt{!sig}\ \mathsf{U}\ \texttt{modeDOWN}\ )\Big)$
Gray Counter	$\mathsf{G}\ \texttt{!rst} \rightarrow \mathsf{XG}\ (\ cnt > 0\ \mathsf{U}\ \texttt{sig}\ )$
	$\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{FG}\ (\ cnt > 0\ \mathsf{U}\ \texttt{sig}\ )$

Table 4: Model Name and LTL Specification in our Benchmark (Safety + Liveness)

A Details of the Case Studies

We benchmark our tool on eleven RTL designs. Ten are adopted from the neural model-checking study of [63], which provided *only* pure-liveness properties. We extend every design with semantically natural pure safety and safety plus liveness specifications. Table 2 lists all pure-liveness formulas, Table 3 the pure-safety formulas, and Table 4 the safety-liveness formulas, all in Linear Temporal Logic (LTL). Below we discuss each design together with its full specification suite.

Delay (DELAY). A counter cnt raises a pulse sig after a fixed delay and is reset by rst. Liveness requires $\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{GF}\ \texttt{sig}$ and, to prevent sig from sticking, $\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{GF}\ (\texttt{sig} \wedge \mathsf{X}\ \texttt{!sig})$. Safety bounds the counter, $\mathsf{G}\ \texttt{cnt} <= N$, and clears sig in the next cycle, $\mathsf{G}\ (\texttt{sig} \rightarrow \mathsf{X}\ \texttt{!sig})$. Safety-Liveness formulas constrain cnt until sig occurs, $\mathsf{G}\ \texttt{!rst} \rightarrow \mathsf{XG}\ \big(\texttt{cnt} < N\ \mathsf{U}\ \texttt{sig}\big)$ and its eventually variant $\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{FG}\ \big(\texttt{cnt} < N\ \mathsf{U}\ \texttt{sig}\big)$.

LCD Controller (LCD). After initialisation the controller waits for lcd_enable, switches from ready to send, and returns to ready. Liveness demands $\mathsf{FG}\ \texttt{lcd\_enable} \rightarrow \mathsf{GF}\ \texttt{ready}$. Safety preserves ready when lcd_enable is low, $\mathsf{G}\big((\texttt{!lcd\_enable} \wedge \texttt{ready}) \rightarrow \mathsf{X}\ \texttt{ready}\big)$, and asserts busy in wait, $\mathsf{G}\big(\mathsf{X}\ \texttt{wait} \rightarrow\ \texttt{busy}\big)$; for safety-liveness a receive phase persists until ready, $\mathsf{G}\big(\texttt{receive} \rightarrow (\texttt{receive}\ \mathsf{U}\ \texttt{ready})\big)$.

Blink (BLINK). A counter toggles led on every wrap and raises a one-cycle flag flg. Liveness asserts $\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{GF}\ \texttt{ledON}$, while safety enforces staying in mode1 if cnt has not wrapped: $\mathsf{G}\big((\texttt{mode1} \wedge \mathsf{X}\ \texttt{mode1}) \rightarrow \mathsf{X}(\texttt{cnt} \neq 0)\big)$. The safety–liveness specification ensures that led remains on until mode0 is reached: $\mathsf{G}\ \texttt{!rst} \rightarrow \mathsf{G}\big(\texttt{ledON} \rightarrow (\texttt{ledON}\ \mathsf{U}\ \texttt{mode0})\big)$.

Thermocouple (Tmcp.). The FSM cycles through start, get_data, pause. Liveness requires $\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{GF}\ \texttt{get\_data}$. Safety keeps get_data active on an idle bus and safety-liveness keeps pause active until get_data becomes reachable: $\mathsf{G}\big(\texttt{!spi\_busy} \wedge \texttt{get\_data} \wedge \texttt{!rst} \rightarrow \mathsf{X}\ \texttt{get\_data}\big)$ and $\mathsf{G}\ \texttt{!rst} \rightarrow \mathsf{G}\big(\texttt{pause} \rightarrow (\texttt{pause}\ \mathsf{U}\ \texttt{get\_data})\big)$.

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7-Segment (7-Seg). Two displays alternate unless reset. Liveness enforces $\mathsf{FG}\ \texttt{!rst} \rightarrow (\mathsf{GF}\ \texttt{disp = 0} \wedge \mathsf{GF}\ \texttt{disp = 1})$ and the single-display variant $\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{GF}\ \texttt{disp = 1}$. Safety freezes the display in the absence of sig: $\mathsf{G}\big(\texttt{!sig}\wedge\mathsf{X}\texttt{!sig}\wedge\texttt{!rst} \rightarrow ((\texttt{ds0}\wedge\mathsf{X}\texttt{ds0})\vee(\texttt{ds1}\wedge\mathsf{X}\texttt{ds1}))\big)$ while safety-liveness holds the display until sig, $\mathsf{G}\ \texttt{!rst} \rightarrow \mathsf{G}\big(((\texttt{ds0} \wedge \mathsf{X}\texttt{ds0}) \vee (\texttt{ds1} \wedge \mathsf{X}\texttt{ds1}))\ \mathsf{U}\ \texttt{sig}\big)$.

i2c Stretch (i2cS). Timing signals scl_clk and data_clk are generated according to bus frequency; stretch handles clock stretching. Liveness states $\mathsf{FG}\ (\texttt{!rst} \wedge \texttt{ena}) \rightarrow \mathsf{GF}\ \texttt{strc}$. Safety links a rising stretch to switch: $\mathsf{G}\big(\texttt{!strc} \wedge \mathsf{X}\texttt{strc} \rightarrow \mathsf{X}\texttt{switch}\big)$ meanwhile safety-liveness, under permanent reset-low, keeps stretch low until switch, $\mathsf{G}\ \texttt{!rst} \rightarrow \mathsf{G}\big(\texttt{!strc} \rightarrow (\texttt{!strc}\ \mathsf{U}\ \texttt{switch})\big)$.

Pulse Width Modulation (PWM). An N-bit counter drives pulse; the design must regularly unset the pulse. Accordingly, liveness requires $\mathsf{GF}\ \texttt{!pulse}$. Two guard signals bound the duty-cycle window: pulseLB (minimum width) and pulseUB (maximum width). Safety enforces these bounds at every cycle, $\mathsf{G}\big((\texttt{pulseLB}\rightarrow\texttt{pulse}) \wedge (\texttt{!pulseUB}\rightarrow\texttt{!pulse})\big)$, and safety-liveness strengthens them with a fairness clause that forces the upper bound to be violated—and thus pulse to be low—infinitely often: $\mathsf{GF}\ \texttt{!pulseUB} \wedge \mathsf{XG}\big(\texttt{!pulseUB}\rightarrow\texttt{!pulse}\big)$.

VGA Controller (VGA). Horizontal and vertical counters drive disp_ena. Liveness: $\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{GF}\ \texttt{disp\_ena}$. Safety flips hs and vs under disp_ena: $\mathsf{G}\big((\texttt{en} \wedge \texttt{!rst}) \rightarrow ((\texttt{hs} \leftrightarrow \mathsf{X}\texttt{!hs}) \vee (\texttt{!hs} \leftrightarrow \mathsf{X}\texttt{hs}))\big)$, $\mathsf{G}\big((\texttt{en} \wedge \texttt{!rst}) \rightarrow ((\texttt{vs} \leftrightarrow \mathsf{X}\texttt{!vs}) \vee (\texttt{!vs} \leftrightarrow \mathsf{X}\texttt{vs}))\big)$, and safety-liveness asserts a vertical–horizontal counter relationship $\mathsf{G}\big(\texttt{Vcnt==0} \rightarrow (\texttt{Vcnt==0}\ \mathsf{U}\ \texttt{Hcnt==0})\big)$.

UART Transmitter (UARTt). The FSM toggles between wait and transmit. Liveness: $\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{GF}\ \texttt{wait}$. Safety couples busy with required modes: $\mathsf{G}\big((\texttt{wait} \rightarrow \texttt{!busy}) \wedge (\texttt{transmit} \rightarrow \texttt{busy})\big)$, and safety-liveness under permanent reset-low holds busy until wait, $\mathsf{G}\ \texttt{!rst} \rightarrow \mathsf{G}\big(\texttt{busy} \rightarrow (\texttt{busy}\ \mathsf{U}\ \texttt{wait})\big)$.

Load–Store (LS). A counter counts up in load, down in store; sig triggers the switch. Liveness: $\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{GF}\ \texttt{sig}$. Safety clears sig after two cycles: $\mathsf{G}\big(\texttt{sig} \rightarrow \mathsf{XX}\texttt{!sig}\big)$. The safety-liveness formulas hold modeUP until sig and, symmetrically, !sig until modeDOWN: $\mathsf{G}\ \texttt{!rst} \rightarrow \mathsf{G}\big(\texttt{modeUP} \rightarrow (\texttt{modeUP}\ \mathsf{U}\ \texttt{sig})\big)$ and $\mathsf{G}\ \texttt{!rst} \rightarrow \mathsf{XG}\big(\texttt{modeUP} \rightarrow (\texttt{!sig}\ \mathsf{U}\ \texttt{modeDOWN})\big)$.

Gray Counter (Gray). Counts in Gray code to minimise bit flips. Liveness: $\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{GF}\ \texttt{sig}$, $\mathsf{FG}\texttt{!rst} \rightarrow \mathsf{GF}(\texttt{sig} \wedge \mathsf{X}\texttt{!sig})$, and $\mathsf{FG}\texttt{!rst} \rightarrow (\mathsf{GF}\texttt{sig} \wedge \mathsf{GF}\texttt{!sig})$. Safety clears sig one step later: $\mathsf{G}\big(\texttt{sig} \wedge \texttt{!rst} \rightarrow \mathsf{X}\texttt{!sig}\big)$. Safety-liveness bind the counter until sig: $\mathsf{G}\ \texttt{!rst} \rightarrow \mathsf{XG}(cnt > 0\ \mathsf{U}\ \texttt{sig})$ and its eventually counterpart $\mathsf{FG}\ \texttt{!rst} \rightarrow \mathsf{FG}(cnt > 0\ \mathsf{U}\ \texttt{sig})$.

Collectively, these benchmarks exercise handshake logic, clock stretching, display timing, PWM generation, UART serialisation, counter bounds, and Gray-code sequencing. Each property appears in pure-liveness, pure-safety, and safety-liveness form, enabling a comprehensive assessment across the complete verification spectrum.

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